SMPTE ENGINEERING GUIDELINE

EG 33-2004
Revision of EG 33-1998

Jitter Characteristics and Measurements

Introduction

Transferring digital signals from one location to another involves converting the signals into an analog physical representation at the sending end and then interpreting that representation to extract the data at the receiving end. This is necessary because any signals that are physically represented inherently have analog properties. These properties include the levels and timing of the data intervals and the transitions between them, the spectral distribution that results, and any signal distortions that occur in the transmission system. This is true whether the signals are modulated onto an RF carrier or transmitted directly as data using an appropriate form of encoding.

Analog effects that can alter digital signals are attenuation, spectral roll-offs and anomalies, overshoots, undershoots, time dispersion, and jitter. The first several are frequency- and amplitude-related effects while jitter is the sole timing-related disturbance.

1 Scope

This guideline examines the types of jitter in directly transmitted data signals, the methods for measuring each one, and some of the impacts they can have on system operation. Additionally, some of the system design approaches that can minimize or mitigate the impact of jitter are presented.

2 Jitter definition

In this guideline, the 270 Mbits/s (Mb/s) serial digital interface (SDI) signals of SMPTE 259M will be used as an example, but the same concepts apply to serially transmitting everything from 3.1 Mb/s AES3 audio data streams through 1.5 Gb/s HDTV versions of the SDI. Only the numerical values used for equipment specifications and measurements change when covering this large range of digital signals.

To send digital data streams from one place to another over a single wire or fiber, data is encoded using one of several self-clocking methods. These include such schemes as NRZ, NRZI, bi-phase mark, and others which typically trade-off the resulting data signal bandwidth and spectral shaping for ease of clock extraction, error detection ability, or other performance features. The important thing about all of these designs is that they allow the clock to be extracted from the data stream so it can be used to recover the data.

Clocking information is usually extracted using phase lock loop circuits. The transition locations in a data stream are instantaneously compared with transitions of a synthesized clocking signal coming from a local oscillator (typically an RC- or LC-type voltage controlled oscillator) at the receiver. The local clock's frequency is then adjusted up or down until the extracted clock's edges agree with the incoming data edges. This process is straightforward as long as the data transitions occur at the expected intervals; that is, integer multiples of the serial clock period. In real systems, however, the data transitions will deviate somewhat from their ideal position; that is, the pulse positions vary with respect to a high stability frequency-locked clock. This unwanted pulse position variation is jitter.

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Jitter is defined as the variation of a digital signal's significant instants (such as transition points) from their ideal positions in time. Jitter can cause the recovered clock and the data to become momentarily misaligned in time. Data may be misinterpreted (latched at the wrong time) when this misalignment becomes great enough. Jitter is measured in terms of the unit interval (UI), which represents the period of one clock cycle and, for NRZ or NRZI encoded data, corresponds to the nominal minimum time between transitions of the serial data. This can be seen in figure 1a, where the data of an NRZI signal and the related clock ticks are shown. Figure 1b shows the effect of jitter on the midpoint crossings of the data transitions, as would be seen on an eye-pattern presentation (repetitive display of transition points overlaid upon one another). Increasing jitter closes the eye in the time dimension and makes decisions between data states correspondingly more difficult, just as signal voltage noise does in the amplitude dimension.

Jitter, then, can be thought of as the phase variation (or modulation) of the serial data stream. This phase modulation has a spectrum that corresponds to the frequency with which the data's clock is modulated. Thus, it is possible to plot an amplitude versus frequency characteristic of the jitter. For example, in figure 2, a single spike at 6144 Hz indicates the presence of sinusoidal phase variation (jitter) at a rate of 6144 Hz. The amplitude of the spike would indicate how much of the data eye was closed.

3 Classes of jitter

Absolute jitter is the aggregate of all jitter frequency components found in a signal, from very low to very high frequency. Measuring exact absolute jitter is practically impossible because it is difficult to generate an absolute reference defining where data edges should be. The practical study of jitter divides it into three classes, based on the frequency content of the jitter modulation.

The very lowest frequency variations in the positions of a signal's transitions are termed wander. Wander typically has no effect on the capability of the clock extraction and decoding electronics to accurately recover the digital data stream because this low-frequency variation can be followed by the PLL (unless the wander causes the data rate to go outside the range of the controlled reference oscillator).

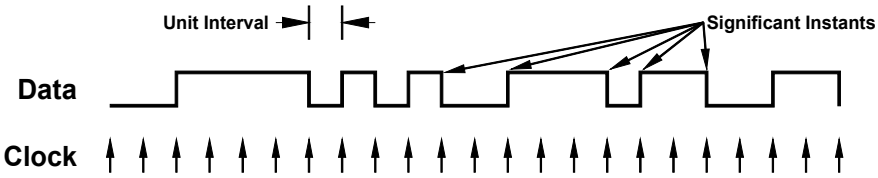
Wander may, however, cause problems in later downstream processing. Wander is generally defined as jitter with frequency components below a particular frequency. In SDI applications, this assigned cutoff is 10 Hz. Measuring wander and absolute jitter implies that the clocking reference used to identify edge jitter be extremely stable with no jitter component of its own. Typical PLL-extracted clocks are unsuitable for this measurement. The source of such an accurate reference signal might be a high-Q crystal oscillator; however, access to this type of signal is not common in SDI applications. This limitation typically causes wander to be excluded in jitter measurements.

Jitter that occurs above the highest frequency defined as wander is termed timing jitter. Jitter that is measured relative to a recovered clock with a loop bandwidth defined by f3 (figure 3) is called alignment jitter. The difference between timing jitter and alignment jitter is the low-frequency jitter.

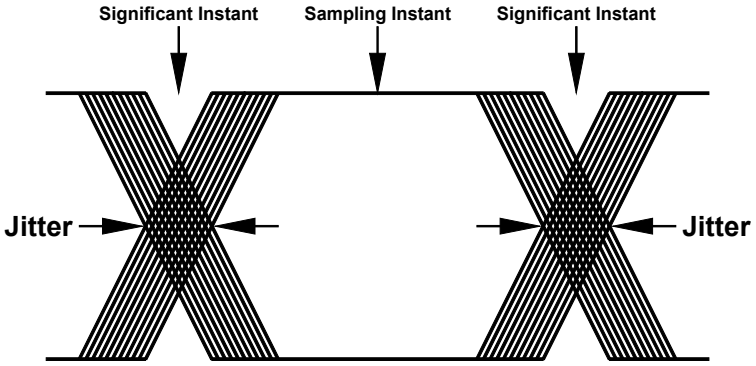
The timing jitter measurement is used to provide an idea of how the overall system is performing. It can be measured by setting the loop filter bandwidth of the clock recovery system to f1. The result will include all frequencies of jitter above the loop filter cutoff to the upper limit of the measurement. This broadband measurement will not specifically identify jitter that could cause data recovery errors.

Alignment jitter can provide information on jitter that directly affects the receiver's ability to properly recover data. This type of error occurs because the PLL is not able to track the timing changes of the incoming signal. If the timing errors become large enough, the decoder will "slip" a bit, which will cause an error in the decoded data. This produces a word framing error, which will not be corrected until the next timing reference signal.

Low-frequency jitter generally does not cause problems in the serial link. Large amounts of low-frequency jitter can be tolerated by the serial link, as the PLL follows these timing changes and maintains proper data recovery. However, one must be aware of this band of jitter, as it will be present in the recovered parallel clock. This parameter is important to monitor if the recovered clock is to be used as a reference signal in the parallel domain.



a) Relationship of Data & Clock for SDI Signals
Showing Unit Interval & Significant Instants



b) Eye Pattern Showing Jitter at Significant Instants

Figure 1 – Elements of serial data signals and relationship to jitter

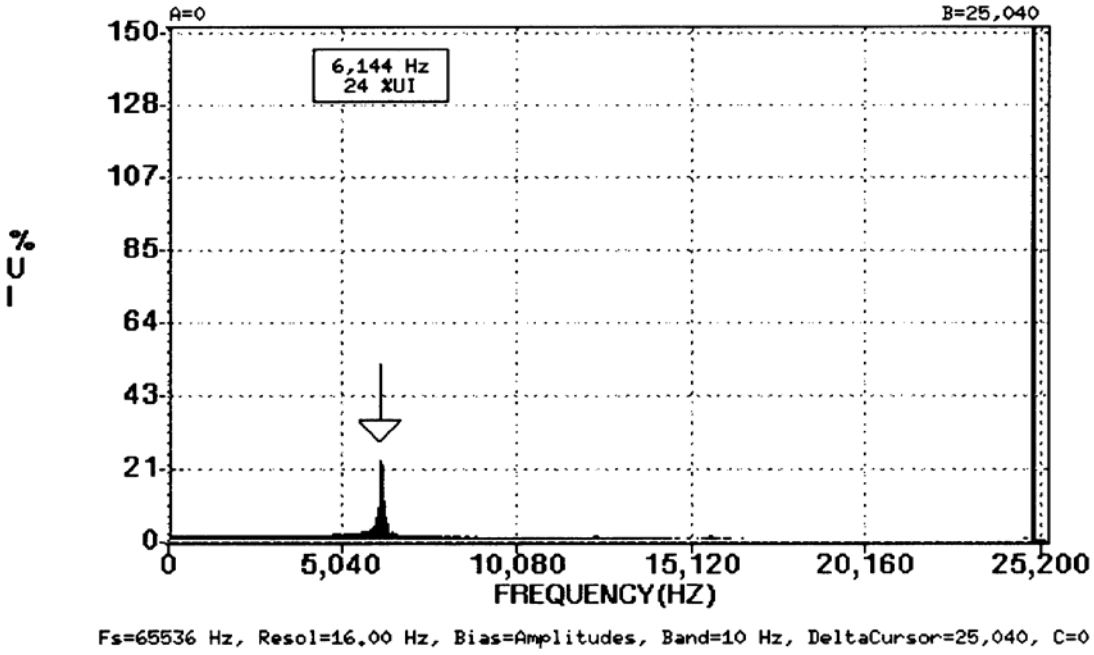


Figure 2 – Jitter frequencies

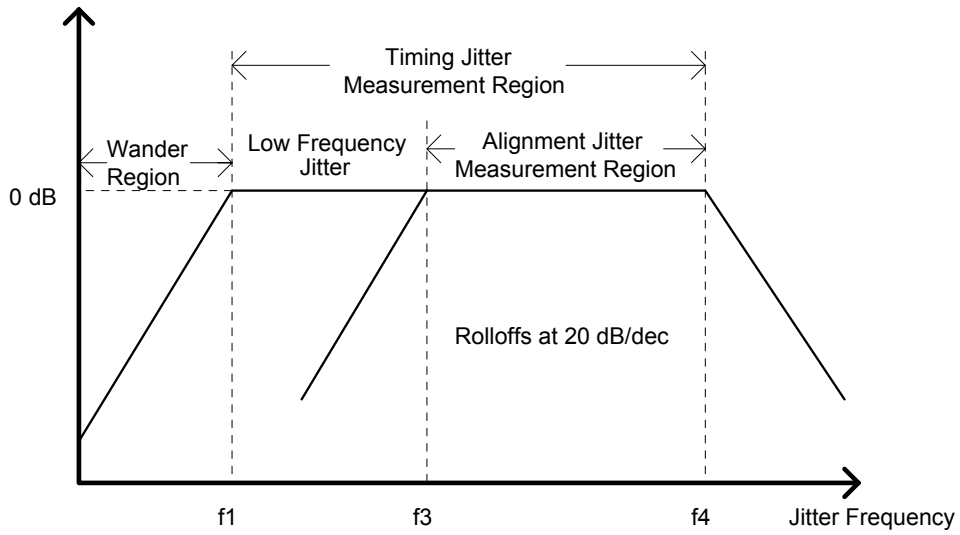


Figure 3 – Jitter measurement regions

The low-frequency jitter can be found by subtracting the alignment jitter from the timing jitter. This will yield accurate results for most types of jitter, such as sinusoidal or random sources of jitter. If the jitter source is a complex waveform, such as a square wave, the frequency and duty cycle will have an effect on this calculation.

In the case of SMPTE 259M serial digital video applications, the frequency roll-off definition for alignment jitter measurements (f3) is 1 kHz. Because there are many popular SDI receivers already in use throughout the industry, this value had to be chosen to be useful for all systems. When choosing this number, a frequency high enough to ignore jitter from typical gen-lock circuits (200 Hz or greater) and low enough to include the clock recovery bandwidths for all popular receiver integrated circuits (10 kHz or less) had to be found.

4 Jitter measurements

Several different instruments and connection arrangements can be used to measure jitter of various types. The more complex techniques will produce more informative results, but the simpler methods can be meaningful as a starting point for understanding the jitter types occurring in a particular system.

The simplest method for observing and measuring jitter is the use of an oscilloscope with an external reference for triggering, as shown in figure 4. The SDI source and the external reference must be locked to a common clock, as any frequency difference (which is not jitter) may interfere with the measurement. The spread of the crossing points of an eye display will reveal the jitter amplitude. If a highly stable external reference, such as a clock derived from black burst, is used, absolute jitter, including wander, will be displayed.

When an external triggering reference is not available, a reference clock must be extracted from the data itself. In this way, greater detail regarding the characteristics of the jitter can be obtained. This can be done by using a clock extractor. A clock extractor is a device that recovers a reference clock from the incoming data stream. The block diagram of a representative clock extractor is shown in figure 5. Clock extractors phase lock to the data stream to synthesize a reference clock and this process inherently has a frequency response to it. A clock extractor that has a phase lock loop natural frequency of 1 kHz will only measure jitter frequencies above 1 kHz because the synthesized reference clock extracted from the data will track the frequency variations at rates below 1 kHz. For this reason, clock extractors typically support multiple-loop filter roll-off frequencies.

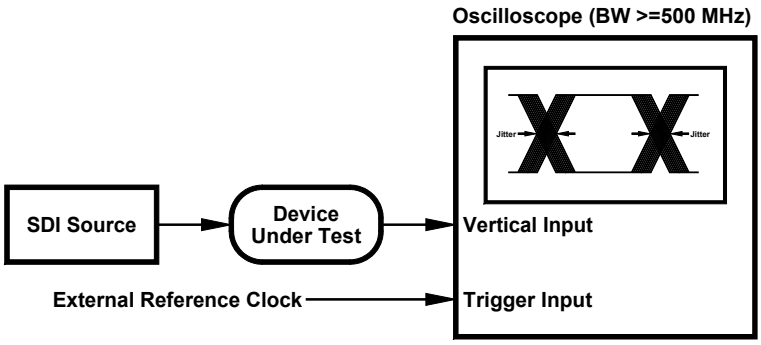


Figure 4 – Jitter measurement with oscilloscope and external reference trigger

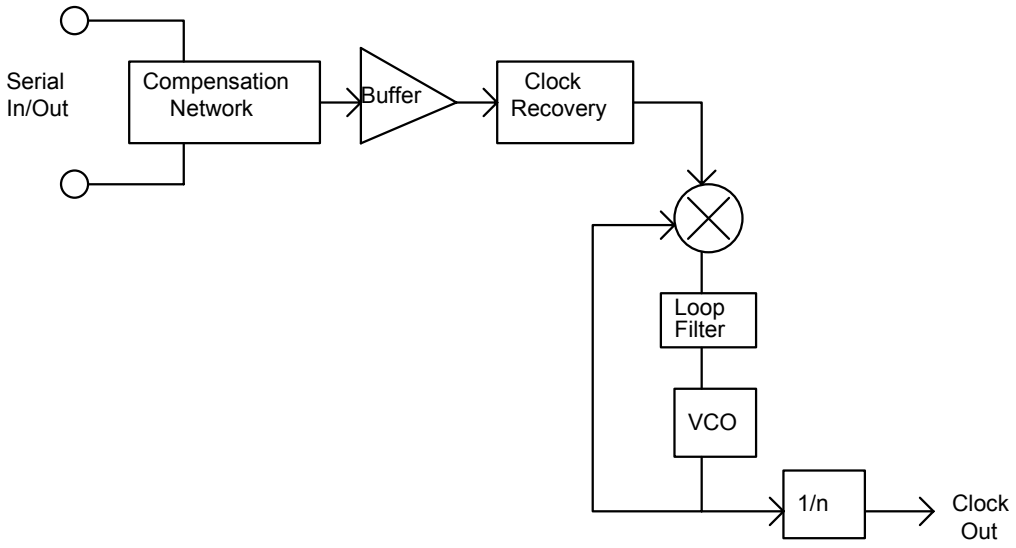


Figure 5 – Block diagram of a clock extractor

An enhanced clock extractor, also called a jitter receiver, includes three sections and provides three outputs (see figure 6). The first section has a passive loop through input (or power splitter), an equalizer, and a high bandwidth phase locked loop (PLL). The high bandwidth of the PLL results in jitter frequencies below the roll-off of the PLL to be passed along in the extracted output clock (output 1). The upper frequency limit of the jitter reproduced by the clock extractor (f4 in figure 3) is set by the loop bandwidth of this PLL. Additionally, a frequency divider with a setable division ratio is provided prior to the clocking output to permit more time between edge transitions. Because the digital divider will pass along perfectly any input clocking jitter as output jitter, an oscilloscope measurement of jitter amplitudes greater than 1 UI is possible. The second section of the enhanced clock extractor includes a second PLL that incorporates a variable bandwidth loop filter and a high quality (high Q) voltage-controlled crystal oscillator. One setting of loop bandwidth in this second PLL determines the upper bound of the wander frequencies (lower bound of jitter measurements — f1 in figure 3). Another setting of loop bandwidth defines the transition frequency between timing jitter and alignment jitter measurements (f3 in figure 3). The output from this section (output 2) also includes a frequency divider similar to that in the output 1 path for oscilloscope measurement of jitter amplitudes larger than 1 UI.

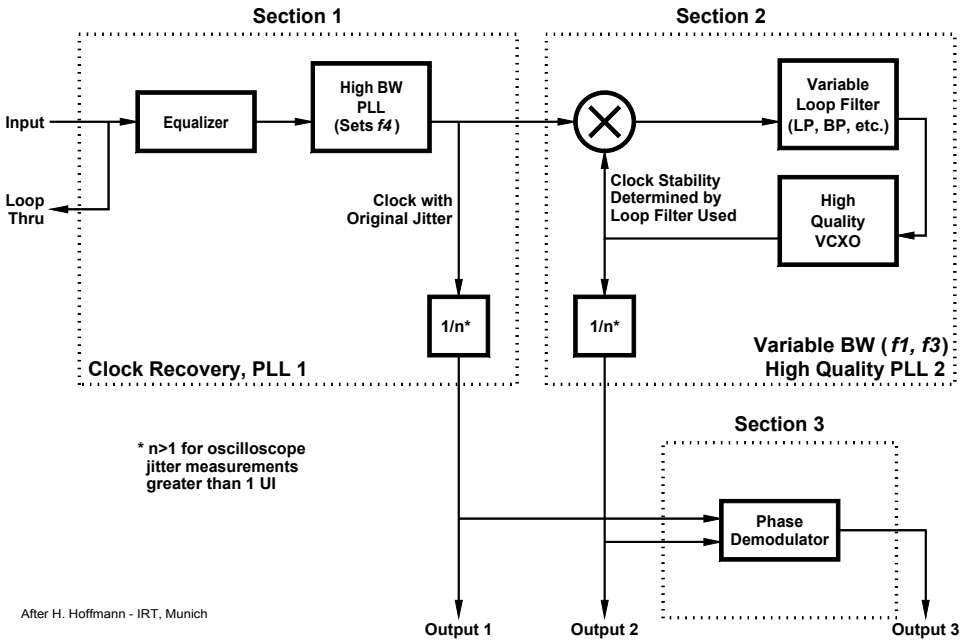


Figure 6 – Jitter receiver block diagram

The third section of a jitter receiver is a phase demodulator. A phase demodulator creates an analog voltage that represents the phase difference of two input signals. In this case, the demodulator uses the clocking outputs of the first two sections as inputs. The demodulator output contains the difference in jitter between PLL 2 and PLL 1, which is the input signal jitter between frequencies f1 (or f3) and f4. This demodulator output (output 3) can then be studied for frequency content. For example, this signal could feed a spectrum analyzer, a selective level voltmeter (effectively a tunable receiver), or a filter and voltmeter arrangement to permit measurement of amplitude versus frequency characteristics. This arrangement is well suited for measuring the peak-to-peak jitter over the frequency bands specified for particular pieces of equipment.

Phase demodulator methods are usually limited in bandwidth to less than 1/10 the clock frequency. Other techniques, such as the eye pattern methods discussed above, may be needed if jitter frequencies above this need investigation. This results from the fact that jitter frequencies as high as 20% of the clock frequency (54 MHz in the case of a 270 Mb/s system, and occurring at twice the 10-bit word rate) have been known to disrupt proper operation of succeeding devices.

Very useful measurements also result from use of a clock extractor in combination with a spectrum analyzer. The exact configuration depends upon the capabilities of the spectrum analyzer used.

If a high-frequency spectrum analyzer with a narrow resolution bandwidth is available, just the first section of the clock extractor can be used in combination with it to display the spectral characteristics of the jitter in terms of amplitude and frequency. This is shown in figure 7, in which the spectrum analyzer has been tuned to the clock frequency (270 MHz in this example) and in which two distinct sidebands are visible. These two sidebands represent a single modulating frequency (at about 40 kHz) that has added jitter to the clock somewhere in the system.

If a low-frequency spectrum analyzer or an oscilloscope with a built-in FFT (fast Fourier transform) analyzer is available, it can be used in conjunction with the complete jitter receiver to create an amplitude versus frequency display similar to that just described. As shown in figure 8, just the demodulated sideband energy is displayed. Depending upon the equipment used, this technique is good for measuring jitter up to about half the clock frequency. This limit comes from the bandwidth of the PLL used in the clock extractor of the jitter receiver. This may not be enough, as will be discussed below. Nevertheless, within its bandpass, it is suitable for discovering specific jitter modulation frequencies and their amplitudes.

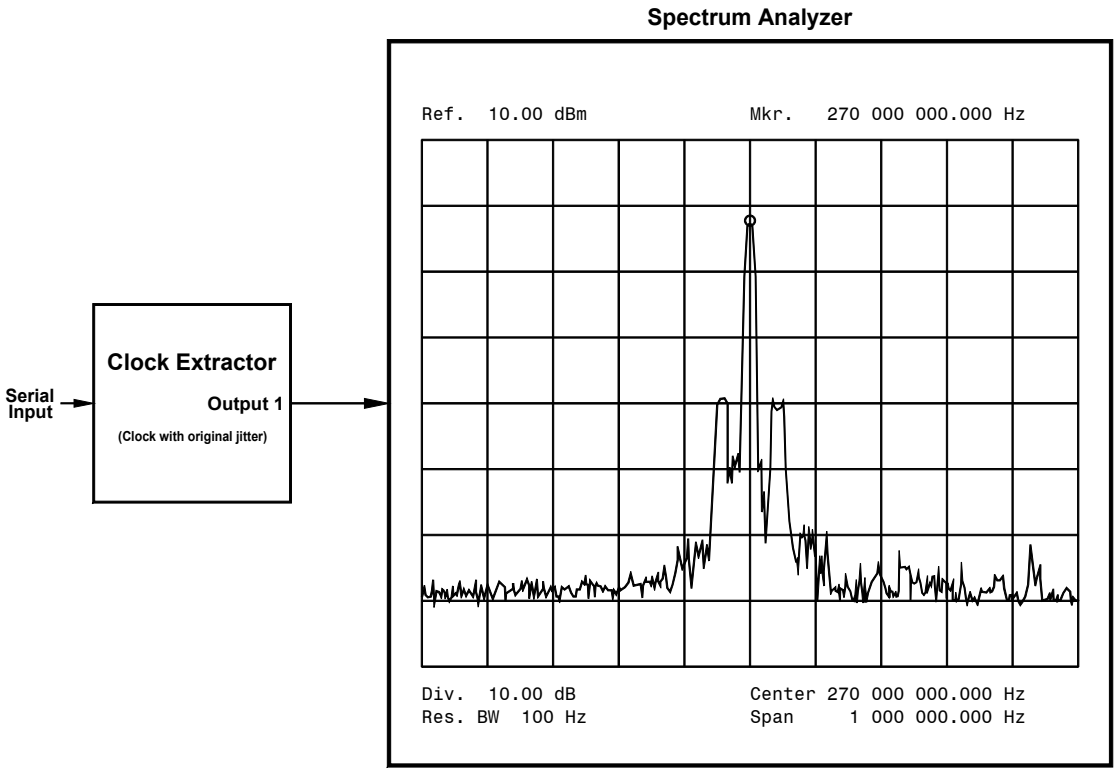


Figure 7 – Jitter measurement using a clock extractor and spectrum analyzer

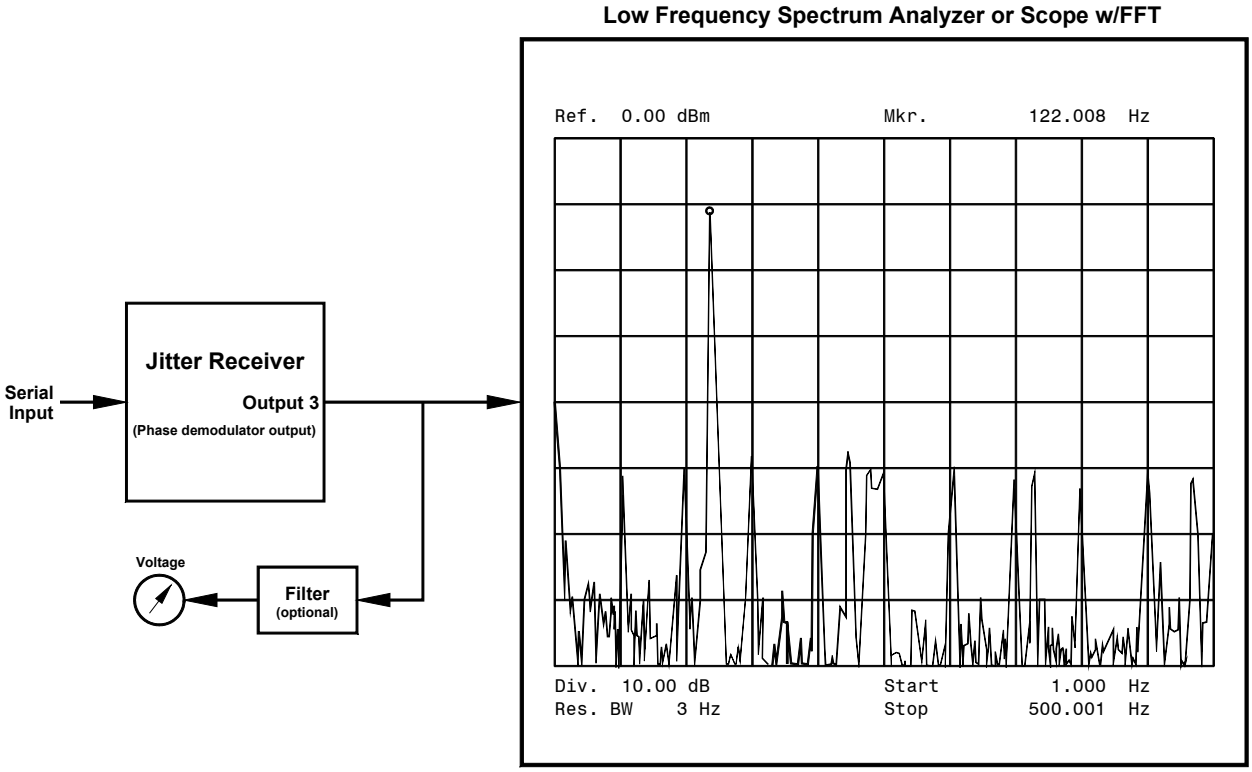


Figure 8 – Jitter measurement using phase demodulator output of jitter receiver

The methods described so far are appropriate for oscilloscope jitter measurements in which the jitter is below 1 UI total deviation. If these methods are used to view greater than l UI of jitter on an oscilloscope, the result would be an image with the entire eye closed, making it impossible to quantify the jitter. When the jitter exceeds 1 UI and a scope is to be used, the dividers in jitter receiver outputs 1 and 2 can be set to a division ratio higher than 1. This has the effect of reducing the frequency of the carrier by the division ratio used and of reducing the modulation deviation by a proportionate amount.

With proper selection of the division ratio, the result is that the phase rotation of the carrier does not exceed 360°, and the eye does not close as it otherwise would at 1 UI. This setup is shown in figure 9, wherein output 2 is used for triggering a wideband oscilloscope and output 1 drives the vertical channel. It is important to keep the division ratio as low as possible when making these measurements so as not to mask any word-related jitter effects, as might occur at a ratio of 10 and its submultiples.

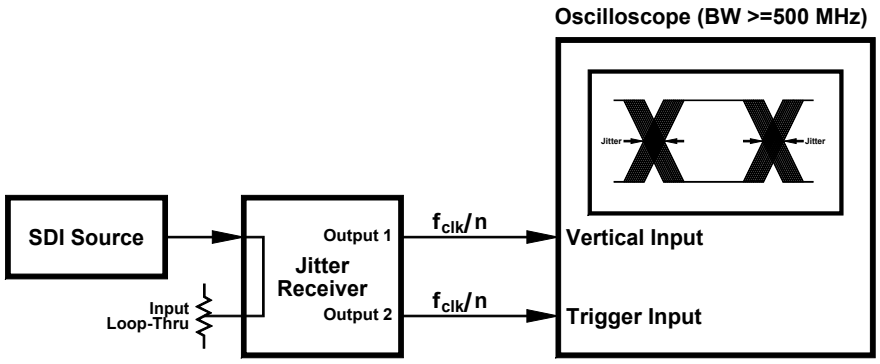


Figure 9 – Jitter measurement of UI > 1 with oscilloscope and jitter receiver using output frequency division

5 Equipment specification

The measurement methods available are used for characterizing equipment with respect to jitter performance. They are also used to determine that system implementations do not permit accumulation of jitter sufficient to cause data errors or degraded performance during digital-to-analog conversion.

The jitter performance of equipment is characterized in several ways. Input jitter tolerance is the peak-to-peak amplitude of sinusoidal jitter that, when applied to an equipment input, causes a specified degradation of error performance. The input jitter tolerance of a piece of equipment can be specified through use of a template, as shown in figure 10. The template specifies the minimum input jitter tolerance expected from the equipment. The actual input jitter tolerance measured (also shown in figure 10) will be higher than the template for properly operating units.

Jitter transfer is jitter that occurs on the output of equipment resulting from jitter applied to the input of that equipment. The jitter transfer function is the ratio of the output jitter to the applied input jitter as a function of frequency. A template is used to specify the jitter transfer function in terms of jitter gain versus frequency. This is shown in figure 11, where a compliant jitter transfer function is shown as falling below the template specification. The template is specified and measurements are made from f1 (the low-frequency specification limit) to fc (the upper band edge of the jitter transfer bandpass).

Jitter at equipment outputs is broken into two categories. Intrinsic jitter is the amount of jitter at the equipment output when the input to the equipment is jitter-free. It is essentially the jitter that is generated by the equipment. Output jitter is the amount of jitter measured at the equipment output when the equipment is embedded in a system. It comprises the sum of the jitter transfer of the jitter appearing at the equipment input and the intrinsic jitter of the equipment.

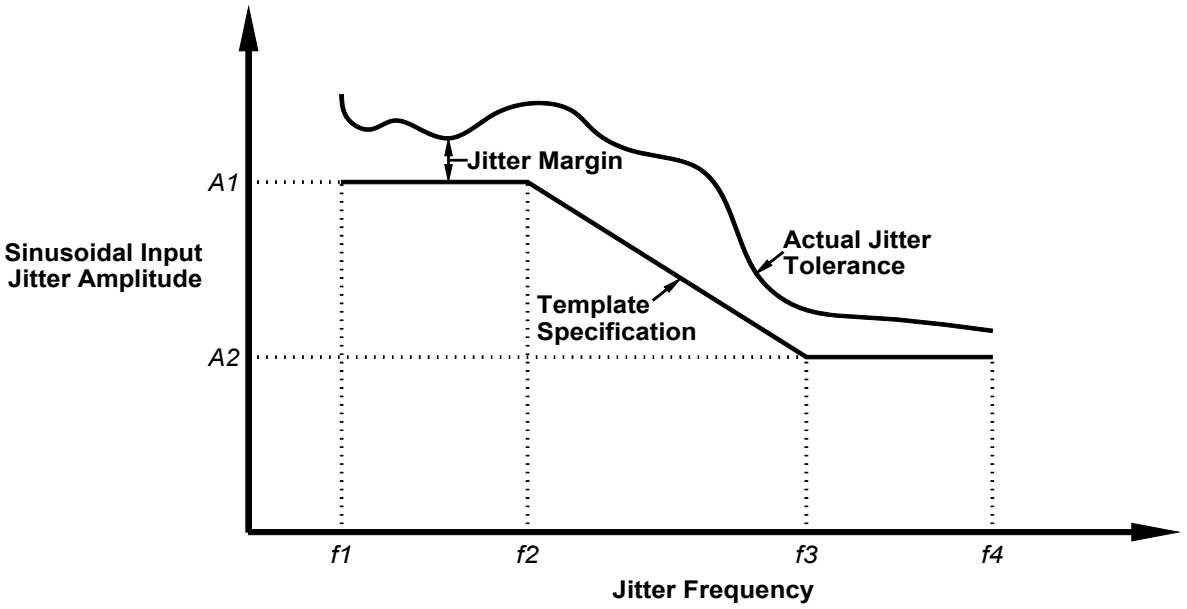


Figure 10 – Input jitter tolerance template and a compliant input jitter tolerance

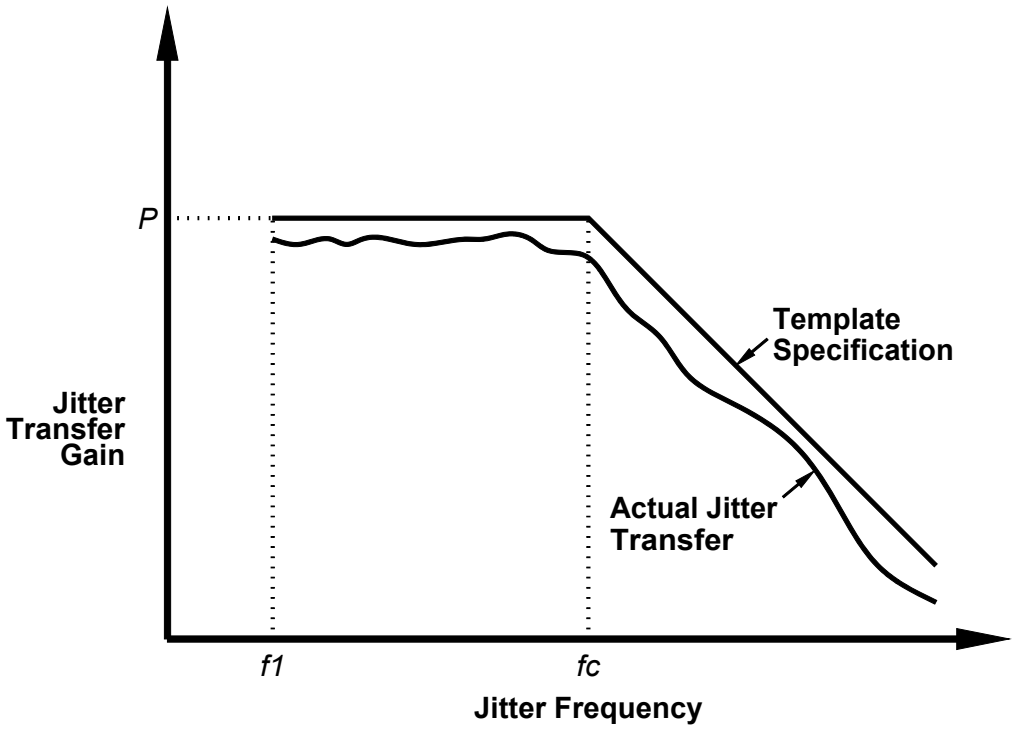


Figure 11 – Jitter transfer template and a compliant jitter transfer function

6 System considerations

Jitter usually accumulates as signals pass through a system. Error-free operation requires that the output jitter at one piece of equipment does not exceed the input jitter tolerance of the succeeding equipment item. Jitter specifications allow estimating the jitter accumulation in a cascade of digital equipment.

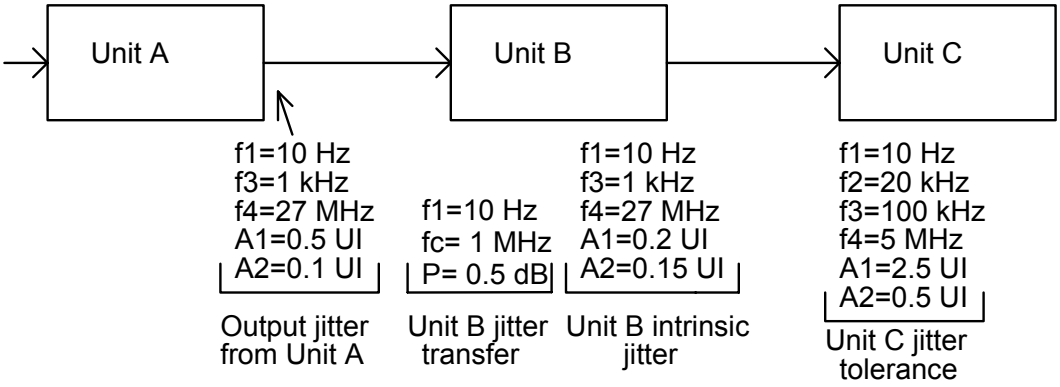
Models for jitter accumulation separate jitter into two categories: random and systematic. Random jitter is defined as jitter that is uncorrelated with other jitter generated in the system. Edge jitter caused by thermal noise in a slicing circuit is an example of random jitter. Since it is uncorrelated, random jitter adds on a power basis: the amplitude increases root-sum-square. Systematic jitter is jitter that is completely correlated with other jitter in the system. Timing variations caused by specific data sequences are an example of systematic jitter, since in a cascade of identical regenerators the same behavior occursat each one. Since it is correlated, systematic jitter accumulates arithmetically.

Most jitter is a combination of random and systematic. After passing through several regenerators, however, systematic jitter usually dominates because of the arithmetic accumulation. Accordingly, simple accumulation models treat all jitter as systematic.

Jitter accumulation is estimated as follows:

1) Jitter at an equipment input is multiplied by the equipment's jitter transfer function;
2) This scaled jitter is added to the equipment's intrinsic jitter to get output jitter;
3) This output jitter becomes the input jitter for the next stage, and the process repeated;
4) At no point can the output jitter exceed the input jitter tolerance of the next stage.

Example:



Step 1: Multiply output jitter from unit A by unit B's jitter transfer function

Unit B's jitter transfer function shows 0.5 dB peaking over 10 Hz to 1 MHz, rolling off beyond 1 MHz. 0.5 dB corresponds to a gain of 1.06.

f1 to fc (10 Hz to 1 MHz): $(A1)\log^{-1}(P/20) = (0.5\ UI)\ (1.06) = 0.53\ U1$
f3 to fc (1 kHz to 1 MHz): $(A2)\log^{-1}(P/20) = (0.1\ UI)\ (1.06) = 0.11\ UI$

Note that the jitter calculation was limited to 1 MHz (fc), even though the input jitter (output jitter from unit A) was specified to 27 MHz (f4). This is because unit B's jitter transfer function low pass filters the input jitter to 1 MHz. Even if higher frequency terms are present, they are not propagated by unit B and hence do not figure into the accumulation calculation.

Step 2: Add unit B intrinsic jitter to jitter transferred by unit B to get unit B output jitter

Above f1 (10 Hz): Output jitter = 0.53 UI + 0.2 UI = 0.73 UI
Above f3 (1 kHz): Output jitter = 0.11 UI + 0.15 UI = 0.26 UI
Above fc (1 MHz): Output jitter = 0.15 UI

The third entry results because there is no jitter transfer above fc (1 MHz). Thus, the only output jitter above this frequency is unit B's intrinsic jitter. Although it is unknown if the 0.15 UI occurs between 1 kHz and 1 MHz, or above 1 MHz, the practice is to assume a constant magnitude over the entire f3 to f4 range.

Step 3: Compare unit B output jitter with unit C input jitter tolerance

Unit C jitter tolerance requires that jitter above f3 (100 kHz) must be less than 0.5 UI, and jitter between f1 (10 Hz) and f2 (20 kHz) must be less than 2.5 UI. Unit B output jitter is 0.15 UI above fc (1 MHz), 0.26 UI above f3 (1 kHz), and 0.73 UI above f1 (10 Hz). A pessimistic but convenient assumption is that all 0.73 UI occurs between f1 and f3 (10 Hz and 1 kHz). Note that unit B's output jitter is less than unit C's input jitter tolerance (see figure 12).

Thus, this cascade of equipment would work.

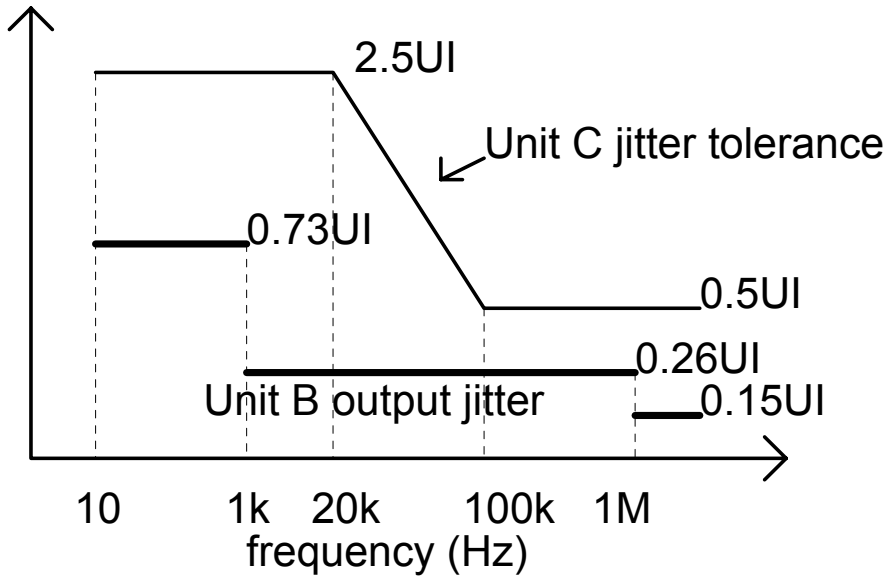


Figure 12 – Unit B output jitter compared with unit C jitter tolerance

The simple method described above allows paper calculations of a proposed cascade of equipment. This requires obtaining jitter tolerance, jitter transfer, and intrinsic jitter specifications from the equipment manufacturer. If unavailable, these parameters can be measured.

Jitter failures result when output jitter exceeds the following equipment's input jitter tolerance. Common causes of this in a system are:

1) Excessive intrinsic jitter, normally the result of poor equipment design or equipment failure;

2) After a cascade of equipment having jitter transfer up to fc, adding a device whose jitter tolerance breakpoint f3 is much lower than frequency fc. Jitter will accumulate arithmetically below fc, and will eventually exceed the high-frequency jitter tolerance A2. There is essentially no jitter accumulation above fc;

3) Peaking in the jitter transfer function, usually near fc (see figure 13). A cascade of equipment with this characteristic can show pronounced jitter growth.

Items 2 and 3 are good examples of why published specifications on jitter transfer and jitter tolerance are important. Item 2 can be avoided by suitable equipment choice, by suitably ordering a cascade of equipment, or by installing a jitter remover prior to the device with the low f3 jitter tolerance breakpoint. Item 3 can be avoided with suitable equipment choice (small jitter peaking), or designed around jitter removers, or by limiting the length of the cascade. All of these solutions require knowing the jitter transfer and tolerance of components in the system.

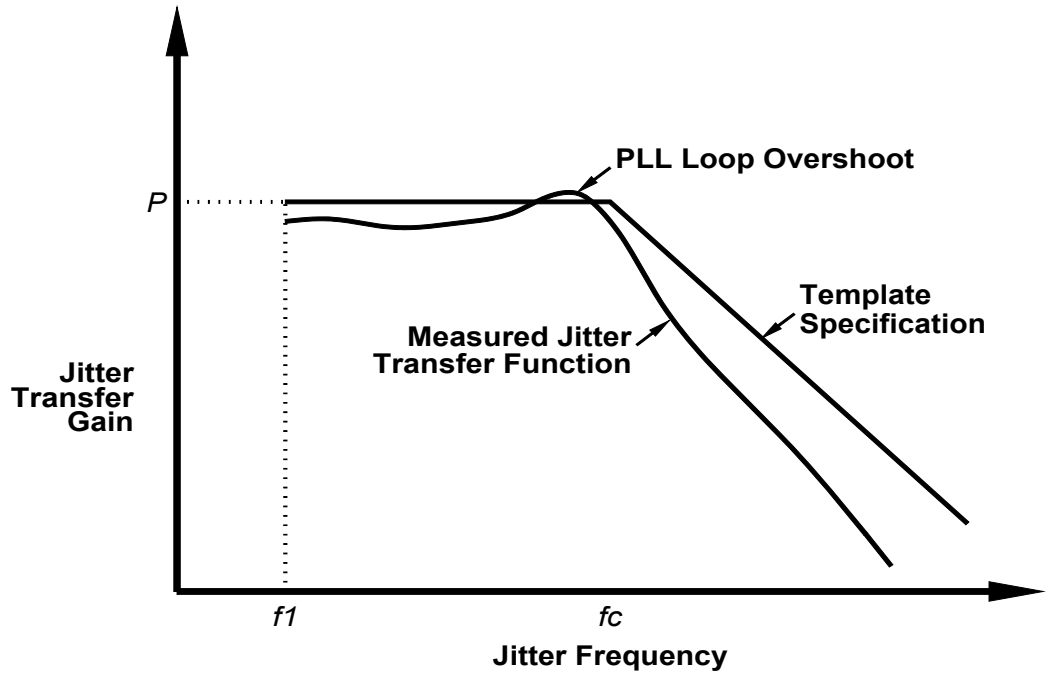


Figure 13 – Jitter transfer function showing jitter peaking

7 Mitigating jitter

It may be necessary to eliminate jitter at various points in a system. This could be for reasons of jitter accumulation sufficient to exceed the input jitter tolerance of a succeeding device, as just discussed, or it could be to permit a high-quality conversion to analog form. Jitter causes non-linearity in digital-to-analog (D/A) converters. High quality D/A conversion, therefore, requires removal of any jitter accompanying a signal if the conversion clock is derived from the signal.

A jitter remover works by converting serial digital signals back to parallel form, passing them through a first-in-first-out (FIFO) register, and then re-serializing them using a highly stable clock. Usually this highly stable

clock is referenced to a synchronization signal like black burst. As shown in figure 14, the input to the jitter remover is structured very much like the input to any equipment with an SDI input. This is followed by a relatively small FIFO with sufficient length to accommodate the longest time variations caused by the highest jitter amplitudes expected to be encountered. Finally, the high quality clock source drives either a serializer or a D/A converter to provide a virtually jitter-free output. Devices of this sort can be applied in a system as often as necessary to control jitter accumulation or to ensure linear analog outputs. Care must be taken in implementing jitter removers to account for the additional delay they cause and to ensure that the delay is predictable.

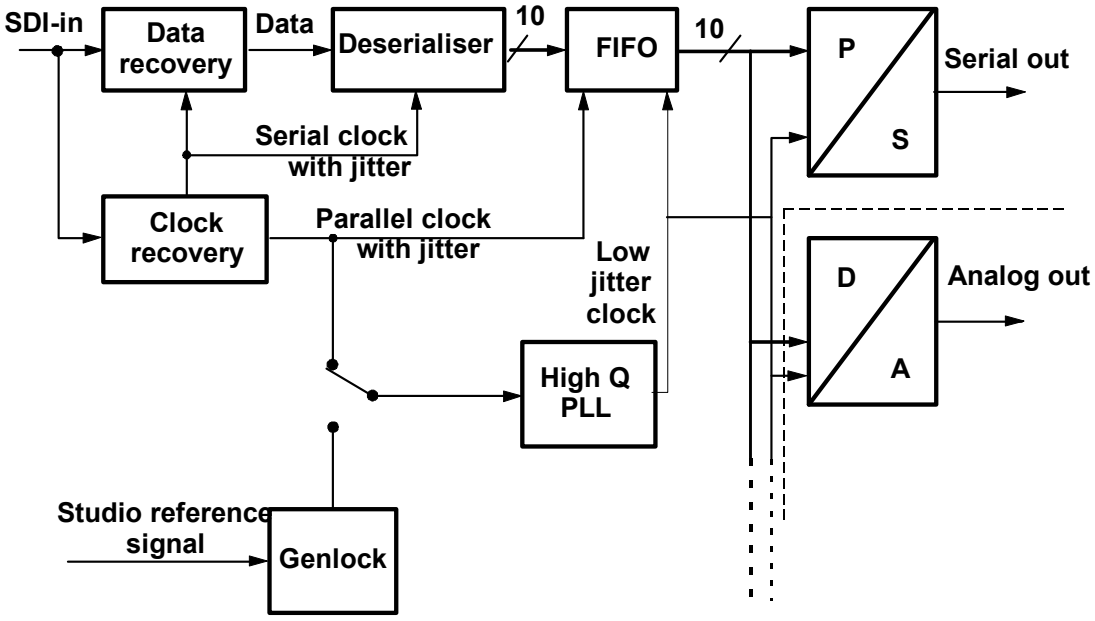


Figure 14 – Block diagram of a "jitter remover"

Annex A (informative)
Bibliography

AES3-2003, Digital Audio Engineering — Serial Transmission Format for Two-Channel Linearly Represented Digital Audio Data

SMPTE 259M, Television — SDTV Digital Signal Data — Serial Digital Interface