SMPTE REGISTERED DISCLOSURE DOCUMENT

Film Transfer — 2048x1556 Image Container and Signal Interface

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Proponent contact information:

Tadashi Okano,
Sony Corporation,
4-14-1 Asahi-cho, Atsugi
Kanagawa, 243-0014
Japan

Email: tadashi.okano@jp.sony.com

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Introduction

The intended application of this RDD is for the transfer of full frame film images to electronic media.

This RDD defines an image pixel array and interface container to transport a maximum pixel array of 2048 x 1556, over a real time serial digital interface of 1650 lines. The source image is a 4:4:4 image, transported by a dual link interface.The 2048 x 1556 source image is mapped into 2 serial Interface containers, 2 x 1536 x 778 pixels (dual channel) per link. The Y/G image samples are interleaved between the Y and C channels of link A. The Red image samples are interleaved between the Y and C channels of link B. The Blue samples are interleaved between the C channels of link A and the Y channel of link B

This RDD serial interface data structure, sampling frequencies, and synchronizing signals have a lot in common to other SMPTE defined HDTV Serial interfaces. These commonalities should allow for the use of HDTV distribution equipment currently in use to transport these images. Because of the mapping format, processing and storage of the serial interface data will be required to display the 2048 x 1556 images.

1 General

Throughout this document reference is made to Ancillary Data Packets (ANC).These data packets are formatted in conformance with SMPTE ST 291.

In the Audio section of the document reference is made to AES-3. Readers may obtain a copy of AES-3 from the Audio Engineering Society.

The time code defined in this RDD is based on SMPTE ST 12M-1, SMPTE ST 12M-2 and Recommendation ITU-R BR.780-2. Details concerning typical physical interfaces, time code data structure, and other implementation issues may be found in these references. This RDD does not use all the user defined binary group data contained within the time code structure.

2 Source Image Format

The source image format is a progressive capture with a maximum 2048 x 1556 pixel array.

The frame rate of the source image array shall be 24, 24/1.001, or 25 frames per second.

Table 1 – System Numbers

System Number	Frame Rate – Frames per second
1	24
2	24/1.001
3	25

The pixel array defined above shall be placed within an image container, however the image may not fill the container.

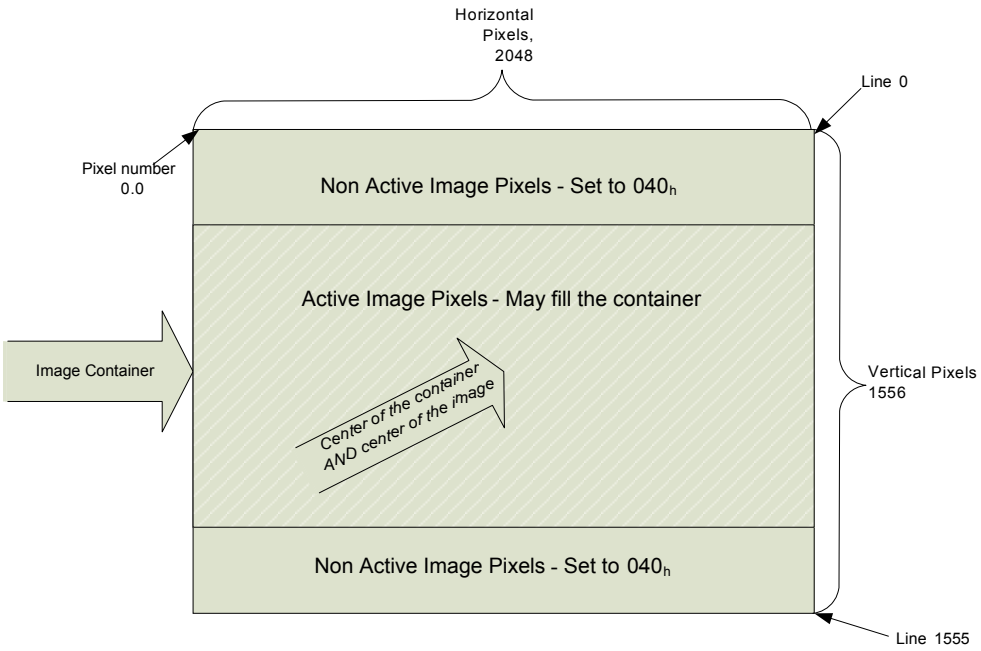

Figure 1 – Image Container

When the source image contains non active pixels, these non-active pixels shall be set to 40h.

The bit depth of each pixel shall be 10 bits.

Image pixel digital values shall not exceed the following values:

Signal level of 100 %	$3AC_h$ $(940_{(10)})$
Signal level of 0 %	040_h $(64_{(10)})$
Head room for Over shoot	$3AD_h$-$3FB_h$ $(941_{(10)}$-$1019_{(10)})$
Foot room for Under shoot	$004h$-$03F_h$ $(4_{(10)}$-$63_{(10)})$

2.1 F-S Colorimetry

2.1.1 Encoding Primaries Free Scale Gamut (FS-Gamut)

The FS colorimetry shall use the CIE XYZ tristimulus values defined in CIE S 014-2/E: 2006 [ISO 11664-2:2007] ranging from –2.00000 to +2.00000. Default values of the primaries and reference white shall be as

defined in Table 2 and is defined as FS-Gamut. — FS-Gamut and FS-Log are identifying names of the defined color space and the Log curve in this RDD.

Table 2 – Default values of FS-Gamut

	CIE *x*	CIE y
R_{FS} primary	0.73470	0.26530
G_{FS} primary	0.14000	0.86000
B_{FS} primary	0.10000	– 0.02985
Reference white D65	0.31272	0.32903

2.1.2 FS-Log curve

From the R_{FS}, G_{FS}, B_{FS} or user defined R_{user}, G_{user}, B_{user} tristimulus values, three nonlinear primary components R'_{FS}, G'_{FS}, B'_{FS} or R', G', B' shall be calculated according to the following FS-Log curve (Equation 1) — and if necessary — the upper and lower three coordinates defined in Table 3. Where nonlinear primary components L' shall be $0 \le L' \le 1$.

Table 3 – Definition of FS-Log curve

Exposure Range	Definition
$L_{C1} \le L \le L_{C3}$	Upper three coordinates (L_{C1}, L'_{C1}), (L_{C2}, L'_{C2}), (L_{C3}, L'_{C3})
$L_{B1} \le L \le L_{C1}$	$L' = \alpha \, Log_{10} (\beta L + \delta) + \varepsilon$ (Equation 1)
$L_{B3} \le L \le L_{B1}$	Lower three coordinates (L_{B3}, L'_{B3}), (L_{B2}, L'_{B2}), (L_{B1}, L'_{B1})

Where, L shall be a linear tristimulus value multiplied by a k_{exp} factor as shown in Equation 2.

$$L = \text{Linear value} \times k_{exp} \; ; \quad k_{exp} \text{ denotes the exposure value} \qquad \text{(Equation 2)}$$

"a linear value" shall mean that each value be linear relative to the amount of light. For example, G_{FS} = 0.18000 denotes an 18% Gray and G_{FS} = 1.00000 denotes light coming from a 100% reflector. The k_{exp} value shall denote the overexposure and the underexposure, i.e., the k_{exp} value of greater than 1 indicates the overexposure and the k_{exp} value of between 0 and 1 indicates the underexposure. The default value of the k_{exp} shall be 1.00000.

The FS-Log curve shall use the Equation 1 with L from L_{B1} to L_{C1} — and if necessary — in combination with two nonlinear curves connecting the upper three coordinates of (L_{C1}, L'_{C1}), (L_{C2}, L'_{C2}), (L_{C3}, L'_{C3}) with L from L_{C1} to L_{C3} and lower three coordinates of (L_{B1}, L'_{B1}), (L_{B2}, L'_{B2}), (L_{B3}, L'_{B3}) with L from L_{B3} to L_{B1} as shown in Figure 3. L_{B1}, L_{B2}, L_{B3} ($L_{B1} > L_{B2} > L_{B3}$) and L_{C1}, L_{C2}, L_{C3} ($L_{C1} < L_{C2} < L_{C3}$) shall indicate the linear values and L'_{B1}, L'_{B2}, L'_{B3} and L'_{C1}, L'_{C2}, L'_{C3} shall indicate the transformed nonlinear values, respectively.

Each of the two nonlinear curves shall be applied only when Equation 1 can not specify the nonlinear characteristics of primary components and shall be a smooth function connecting each of the upper and lower three coordinates as shown in Figure 3 and Figure 4.

Parameter values of α, β, δ, ε as well as the upper three coordinates of (L_{C1}, L'_{C1}), (L_{C2}, L'_{C2}), (L_{C3}, L'_{C3}) and lower three coordinates of (L_{B1}, L'_{B1}), (L_{B2}, L'_{B2}), (L_{B3}, L'_{B3}) shall be defined within the limitation of having the value of L' ranging from 0 to 1 and shall be carried within the Color ANC defined in Section 11.

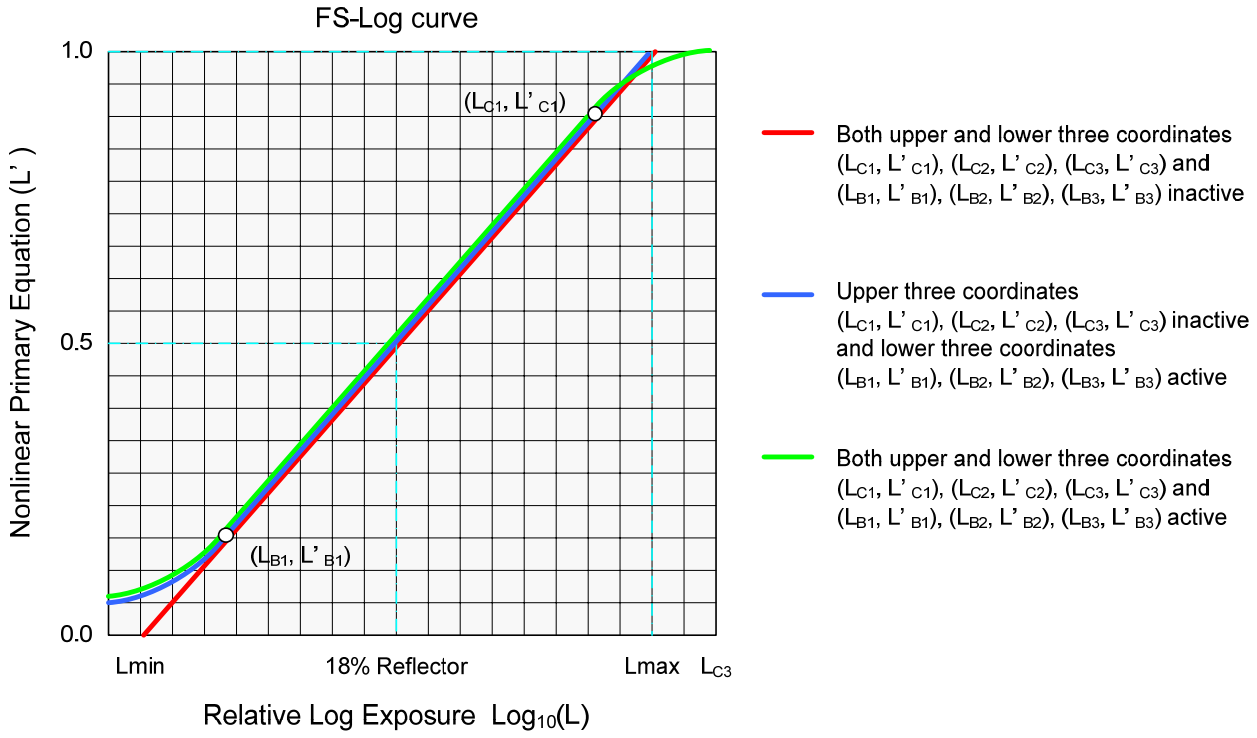

Figure 2 – FS-Log curve

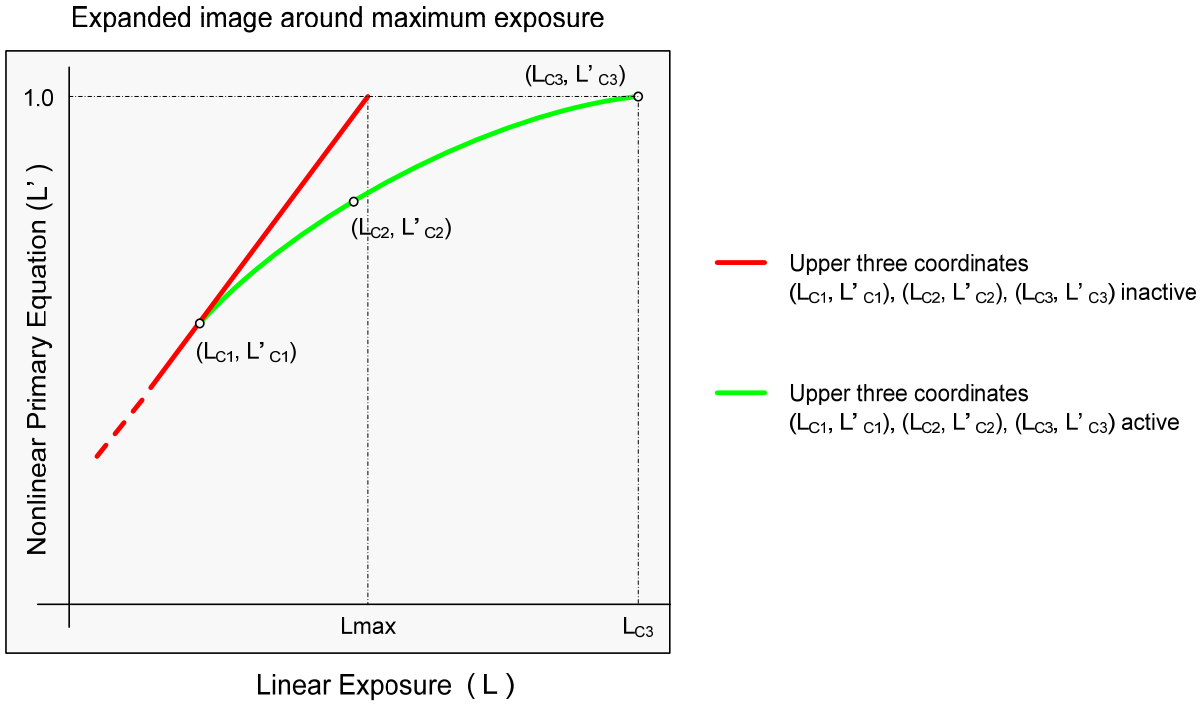

Figure 3 – Three coordinates to define FS-Log curve above LC1

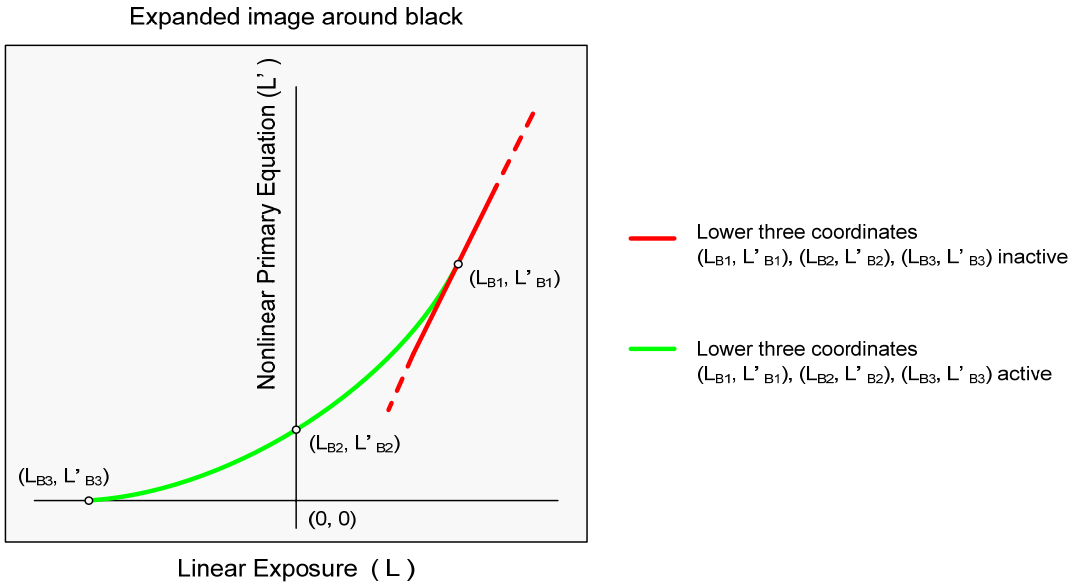

Figure 4 – Three coordinates to define FS-Log curve below LB1

2.1.3 Notation of parameter values

Parameter values which shall be mapped into the Color ANC defined in §11 and shall be denoted by the 32-bit single-precision Binary Floating-Point Arithmetic defined in IEEE 754-2008 as shown in Figure 5, and Equation 3.

In Figure 5 and Equation 3, the most significant bit is the sign bit, the exponent is biased by 127(exponent - 127 in the range -126 to +127 are representable), and fraction is significand without the most significant bit. The detail is defined in IEEE 754-2008.

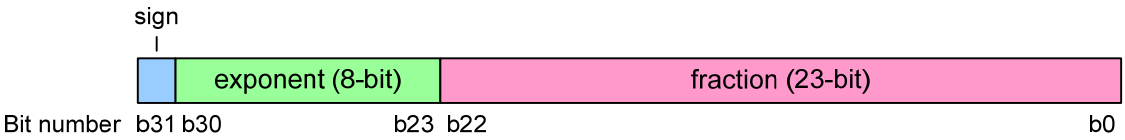

Figure 5 – 32-bit Binary Floating-Point Arithmetic

$$v = s \times 2^{e} \times m$$

or

$$v = (-1)^{sign} \times 2^{(exponent - 127)} \times 1.fraction \qquad \text{(Equation 3)}$$

Where

s = +1 (positive numbers and +0) when the sign bit is 0
s = -1 (negative numbers and -0) when the sign bit is 1
e = *exponent* - 127 (in other words the exponent is stored with 127 added to it, also called "biased with 127")
m = 1.*fraction* in binary (that is, the significand is the binary number 1 followed by the radix point followed by the bits of the *fraction*). Therefore, 1 < m < 2.

2.1.4 Color Ancillary Data

A Color Ancillary Data packet as defined in Section 11 shall be used to carry user defined parameters of color primaries and FS-Log curve. ACT1 and ACT2 of the Color ANC indicate active color primaries, active nonlinear curve, active parameters of the FS-Log curve, etc.

2.2 R'G'B'/Y',C'$_R$,C'$_B$Colorimetry

The default value of R', G', B' opto-electric conversion including encoding primaries, reference white, opto-electric transfer characteristics as well as Y', C'$_R$, C'$_B$ computation shall be in conformance with Recommendation ITU-R BT.709-5.

2.3 Image Pixel Array Representation

2.3.1 FS-Log Pixel Array Representation

The FS-Gamut primary components shall be computed according to Equation 4:

$$L'_D = \text{floor}\{(4095/16)DL'\}; \quad 0 \le L' \le 1, D = 2^{n-8}\ n=10, 12 \quad \text{(Equation 4)}$$

Where L' shall be the component value in abstract terms from 0 to 1, n takes the value 10 or 12 corresponding to the number of bits to be represented, and L'D is the resulting digital code. The function floor(x) returns the largest integer less than or equal to x.

2.3.2 R'G'B' Pixel Array Representation

The R', G', B', R_{fs},G_{fs},B_{fs}, and Y', C'$_R$, C'$_B$ pixel array representation shall be in conformance with Section 2.

3 Transport Image Container Parameters

The transport image container shall be 1536 samples carried on 778 lines per field. See Figures 7 and 9.

The pixel numbering of the container shall begin with a value of 0.0 thru 1535.777.

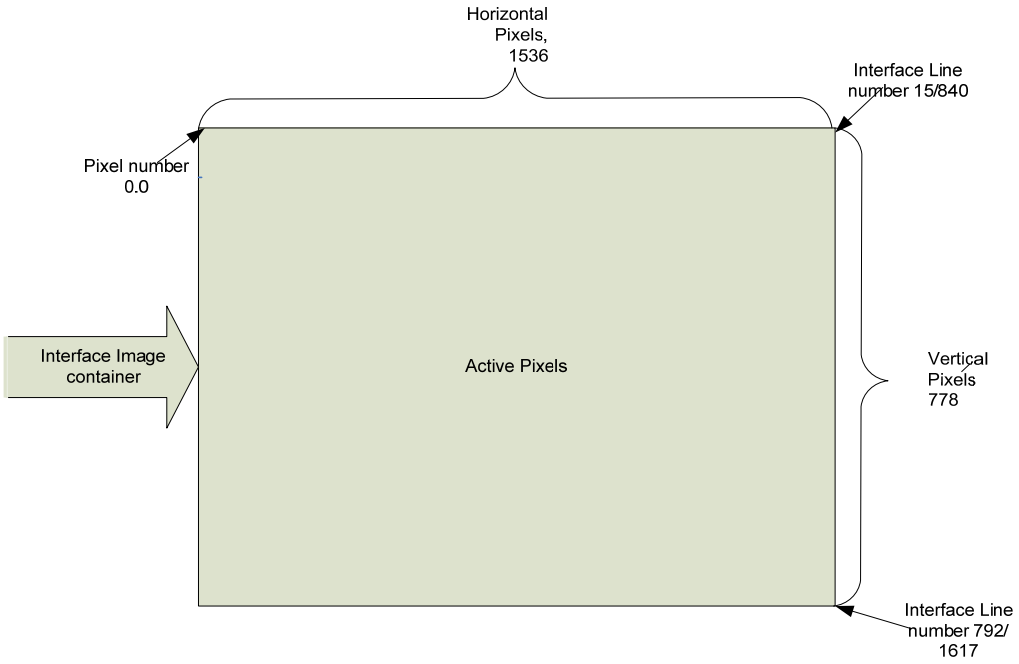

Figure 6 – Interface Image Container

4 Virtual Interface Data Values and Structure

There shall be 3 data channels represented on the virtual interface, R.G.B, Y´,$C'_{R.}C'_{B,}$ or $R'_{FS}G'_{FS}B'_{FS}$.

The data format at the virtual interface of each channel shall consist of synchronizing signals (EAV andSAV), the serial digital interface container, and ancillary data space. See Figure 7.

SAV (start of active video) and EAV (end of active video) digital synchronizing sequences shall provide synchronization across the serial digital interface.

5 Serial Interface Characteristics

The total number of lines carried on the interface shall be 1650. See Figure 8.

The three data streams of the source Image interface shall be mapped into the two channels, of link A and B for dual link implementations or the Y and C channel of a single 3 Gb/s link.

The channels of the links are commonly referred to as the Y channel and C channel. For consistency this RDD will use the same terminology, although the signals carried may not be Y or color difference signals.

The data structure of the Serial Interface shall be as shown in Figures 7 and 8.

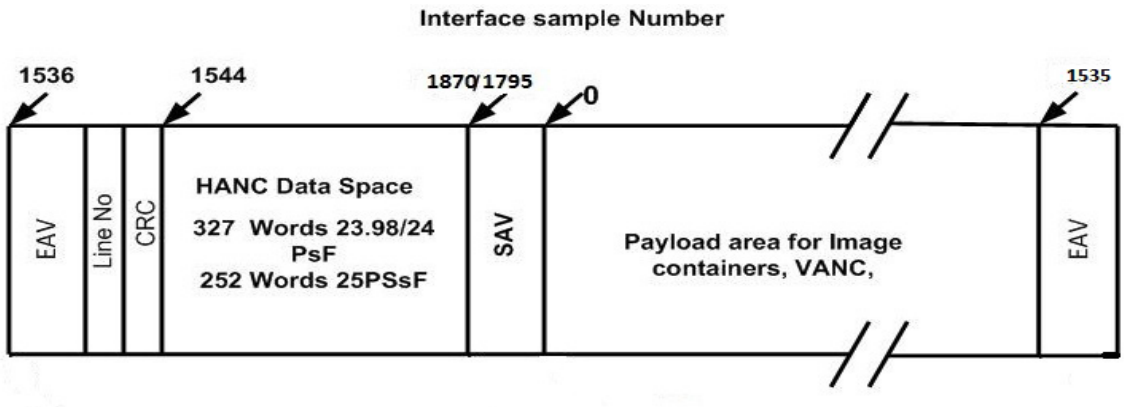

Figure 7 – Interface Sample Number Details

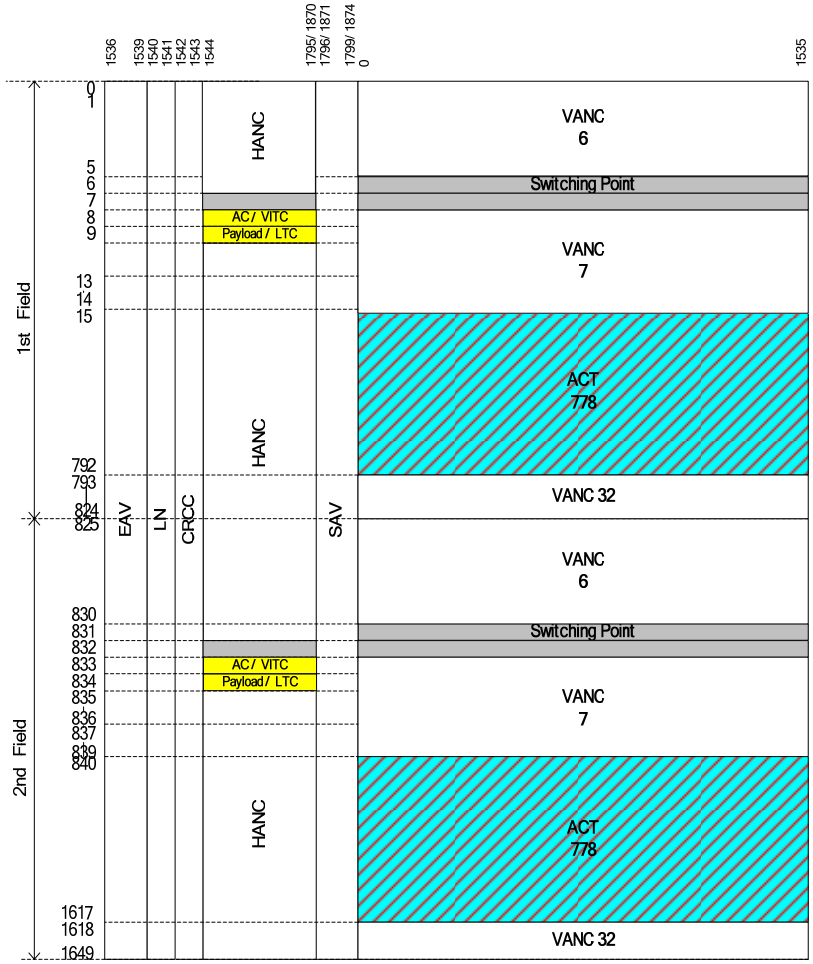

Figure not to scale

Figure 8 – Serial Interface Structure

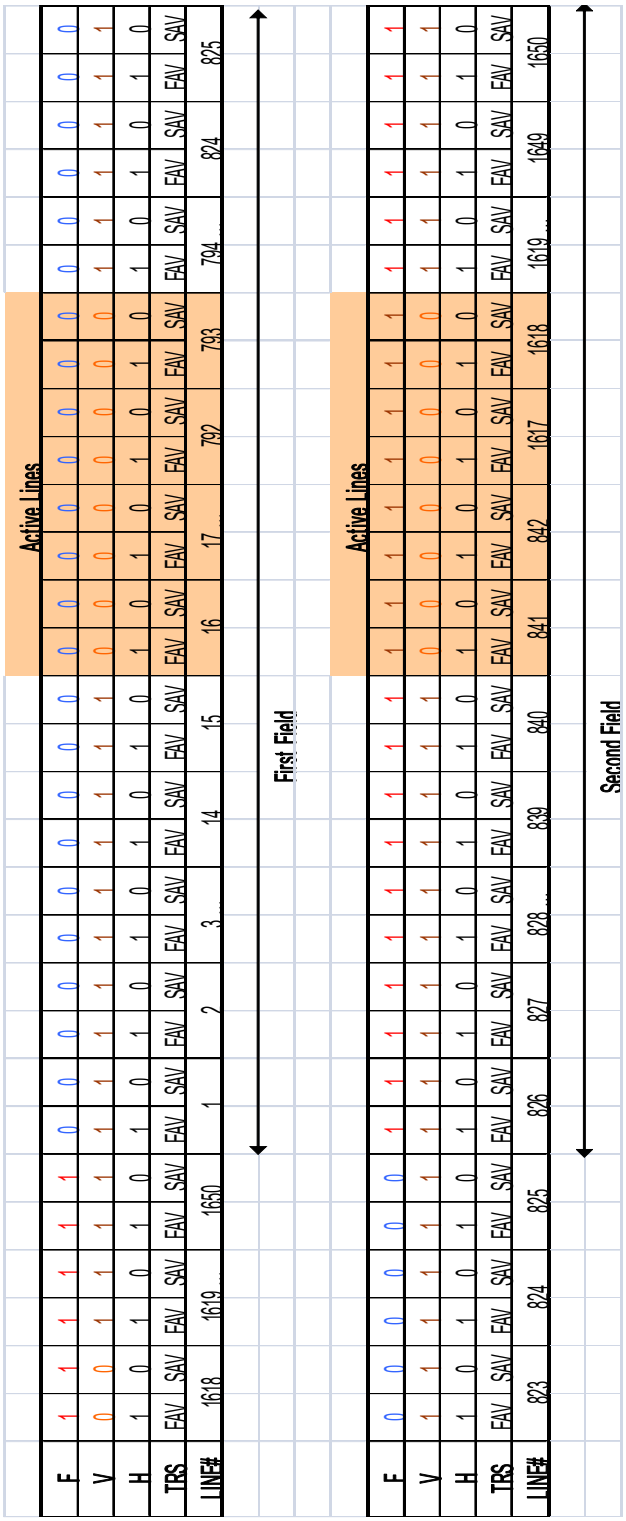

Figure 9 – Interface F, H, V

Note= Line # is the interface line number

Data values 000h to 003h and 3FCh to 3FFh shall be used exclusively for interface synchronization.

Timing references SAV, EAV, line number, and CRCs for each of the two parallel data streams shall be formatted as shown in Figure 8 and 10.

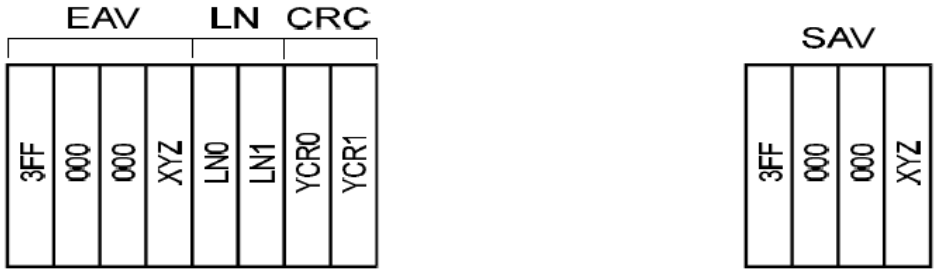

Figure 10 – Timing reference format (Y channel shown)

5.1 Timing Reference Signal Data Structure

An SAV or EAV sequence shall comprise four consecutive code words: a code word of all ones, a code word of all zeros, another code word of all zeros, and a code word including F (field/frame), V (vertical), H (horizontal), P3, P2, P1, and P0 (parity) bits. An SAV sequence shall be identified by having H = 0; EAV shall have H = 1 (Tables 4 and 5 show details of the coding).

Table 4 – Video timing reference codes

	Bit number	9 (MSB)	8	7	6	5	4	3	2	1	0 (LSB)
Word	Value										
0	$3FF_h$ ($1023_{(10)}$)	1	1	1	1	1	1	1	1	1	1
1	0	0	0	0	0	0	0	0	0	0	0
2	0	0	0	0	0	0	0	0	0	0	0
3		1	F	V	H	P3	P2	P1	P0	0	0

Table 5 – Protection bits for SAV and EAV

Bit number	9	8	7	6	5	4	3	2	1	0
Function	1 Fixed	F	V	H	P3	P2	P1	P0	0 Fixed	0 Fixed
0	1	0	0	0	0	0	0	0	0	0
1	1	0	0	1	1	1	0	1	0	0
2	1	0	1	0	1	0	1	1	0	0
3	1	0	1	1	0	1	1	0	0	0
4	1	1	0	0	0	1	1	1	0	0
5	1	1	0	1	1	0	1	0	0	0
6	1	1	1	0	1	1	0	0	0	0
7	1	1	1	1	0	0	0	1	0	0

Interface line number data are composed of two words and shall be as shown in Table 6.

Table 6 – Line number data

Word	9 (MSB)	8	7	6	5	4	3	2	1	0 (LSB)
LN0	$\overline{B8}$	L6	L5	L4	L3	L2	L1	L0	R	R
LN1	$\overline{B8}$	R	R	R	L10	L9	L8	L7	R	R

Notes: 1 L0 – L10 = line number in binary code.
2 R = reserved, set to “0”.

CRC (cyclic redundancy check codes) are used to detect errors in the active digital line and the EAV which follows it. The error detection code consists of two words determined by the polynomial generator equation:

$$CRC(X) = X^{18} + X^5 + X^4 + 1$$

The initial value of the CRC is set to zero. The calculation starts at the first active line word and ends at the final word of the line number, LN1. Two CRCs are calculated, one for the Y data channel and one for the C data channel of the interface, as shown in Table 7.

Table 7 – CRC data

Word	9 (MSB)	8	7	6	5	4	3	2	1	0 (LSB)
YCR0	$\overline{B8}$	CRC8	CRC7	CRC6	CRC5	CRC4	CRC3	CRC2	CRC1	CRC0
YCR1	$\overline{B8}$	CRC17	CRC16	CRC15	CRC14	CRC13	CRC12	CRC11	CRC10	CRC9
CCR0	$\overline{B8}$	CRC8	CRC7	CRC6	CRC5	CRC4	CRC3	CRC2	CRC1	CRC0
CCR1	$\overline{B8}$	CRC17	CRC16	CRC15	CRC14	CRC13	CRC12	CRC11	CRC10	CRC9

5.2 Channel Coding

The channel coding scheme shall be scrambled NRZI (non-return to zero inverted).

The generator polynomial for the scrambled NRZ shall be G1(X) = X9 + X4 + 1. Polarity-free scrambled NRZI sequence data shall be produced by the generator polynomial G2(X) = X + 1. The input signal to the scrambler shall be positive logic. (The highest voltage represents data 1 and the lowest voltage represents data 0.). Example of a possible implementation is shown in Figure 11.

The serial interface data word length shall be 10 bits.

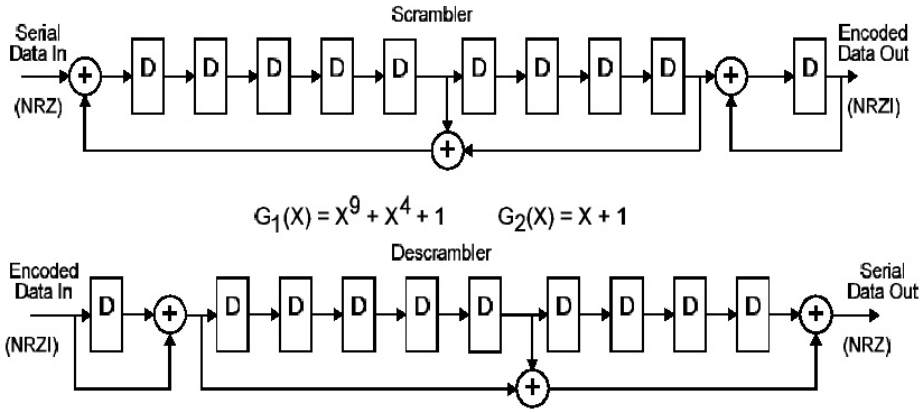

Figure 11 – Example of a possible Scrambler Descrambler

5.3 Coaxial Cable Interface

5.3.1 Signal Levels and Specifications

The output of the generator shall be measured across a 75-ohm resistive load connected through a 1-m coaxial cable. Figure 12 depicts the measurement dimensions for amplitude, rise-time and overshoot.

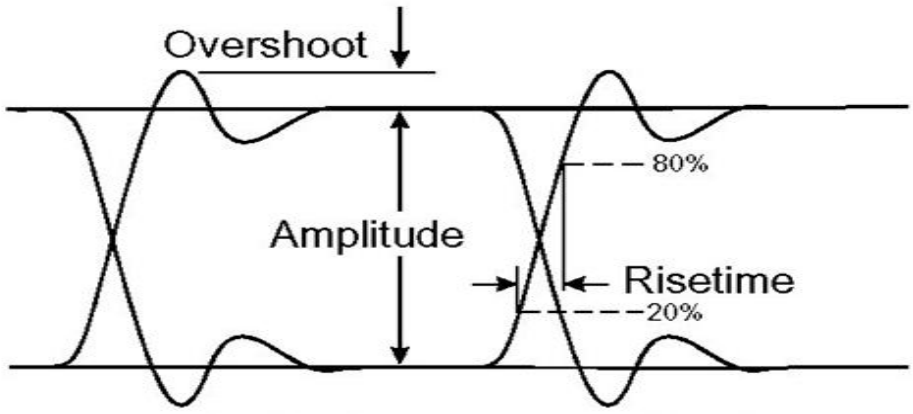

Figure 12 – Waveform measurement dimensions

The generator shall have an unbalanced output circuit with a source impedance of 75 ohms and a return loss of at least 15 dB over a frequency range of 5 MHz to the clock frequency of the signal being transmitted.

The peak-to-peak signal amplitude shall be 800 mV ± 10%.

The dc offset, as defined by the mid-amplitude point of the signal, shall be nominally 0.0 V ± 0.5 V.

The rise and fall times, determined between the 20% and 80% amplitude points shall be no greater than 270 ps and shall not differ by more than 100 ps.

Overshoot of the rising and falling edges of the waveform shall not exceed 10% of the amplitude.

Output amplitude excursions due to signals with a significant dc component occurring for a horizontal line (pathological signals) shall not exceed 50 mV above or below the average peak-to-peak signal envelope. Note this specification defines a minimum output coupling time constant.

The jitter in the timing of the transitions of the data signal shall be measured in accordance with SMPTE RP 184. Measurement parameters are defined in SMPTE RP 184 and shall have the values shown in Table 8 for compliance with this RDD.

The receiver of the serial interface signal shall present an impedance of 75 ohms with a return loss of at least 15 dB over a frequency range of 5 MHz to the clock frequency of the signal being transmitted.

Receivers shall as a minimum operate with input cable loss of up to 20 dB at one-half the clock frequency.

When connected to a line driver operating at the lower limit of voltage permitted the receiver must sense correctly the binary data in the presence of the superimposed interfering signal at the following levels:

dc	± 2.5V
Below 5 kHz	<2.5V p-p
5 kHz to 27 MHz	<100 mV p-p
Above 27 MHz	<40 mV p-p

Table 8 – Jitter specifications

B1	10 Hz	Timing jitter lower band edge	
B2	100 kHz	Alignment jitter lower band edge	
B3	> 1/10 the clock rate	Upper band edge	
A1	2 UI(3Gb/s)/1UI(1.5Gb/s)	Timing jitter	(Note 1)
A2	0.2 UI(3Gb/s)/0.2 UI(1,5Gb/s)	Intrinsic jitter (UI = unit interval)	
Test signal	Color bar test signal		(Note 2)
n	≠10 (preferred)	Serial clock divided	(Note 3)

Notes:

1 Color bars are chosen as a nonstressing test signal for jitter measurements. Use of a stressing signal with long runs of zeros may give misleading results.

2 Use of a serial clock divider value of 10 may mask word correlated jitter components.

3 See SMPTE RP 184 for definition of terms.

5.4 Connector and Cable Types

The male and female connectors shall be 75-ohm BNC as defined in IEC 61169-8, Part 8, Annex A.

Application of this RDD does not require a particular type of coaxial cable. It is necessary for the frequency response of the coaxial cable loss, in decibels, to be approximately proportional to $1/\sqrt{f}$ from 1 MHz to the clock frequency of the signal being transmitted to ensure correct operation of automatic cable equalizers over moderate to maximum lengths.

Return loss of the correctly terminated transmission line shall be greater than 15 dB over a frequency range of 5 MHz to the clock frequency of the signal being transmitted.

6 Dual Link Image Data Mapping

The source image format is a 2048 x 1556 pixel array this pixel array shall be mapped into two 1536 x 778 interface containers per each link. See Figure 8.

Audio = 16ch :
31word/ Group x 4Group x 2sample(max)/ line
= 248Word(max) / Line

48kHz 1-16ch MUX / 96kHz 1-8ch MUX

sampling rate = 74.25MHz

1.5G Link A	Y Chn	G2040	G2041	G2042	G2044	G2045	G2046	EAV (3FFh)	EAV (000h)	EAV (000h)	EAV (XYZh)	LN0	LN1	CRC0	CRC1	ANC/ Audio Data = 327 Words(23.98PsF) = 252 Words(25PsF)				SAV (3FFh)	SAV (000h)	SAV (000h)	SAV (XYZh)	G0	G1	G2	G4			
	C Chn	B2040	B2041	G2043	B2044	B2045	G2047	EAV (3FFh)	EAV (000h)	EAV (000h)	EAV (XYZh)	LN0	LN1	CRC0	CRC1					SAV (3FFh)	SAV (000h)	SAV (000h)	SAV (XYZh)	B0	B1	G3	B4			
1.5G Link B	Y Chn	R2040	B2042	B2043	R2044	B2046	B2047	EAV (3FFh)	EAV (000h)	EAV (000h)	EAV (XYZh)	LN0	LN1	CRC0	CRC1	Reserved				SAV (3FFh)	SAV (000h)	SAV (000h)	SAV (XYZh)	R0	B2	B3	R4			
	C Chn	R2041	R2042	R2043	R2045	R2046	R2047	EAV (3FFh)	EAV (000h)	EAV (000h)	EAV (XYZh)	LN0	LN1	CRC0	CRC1	48kHZ Blank / 96kHz Audio 9-16ch				SAV (3FFh)	SAV (000h)	SAV (000h)	SAV (XYZh)	R1	R2	R3	R5			
23.98PsF WORD#	23.98PsF WORD#	1870	1871	1872	1873	1874	1875	1	2	3	4	5	6	7	8	9	...	...	335	336	337	338	339	340	341	342	343			
25PsF WORD#	25PsF WORD#	1795	1796	1797	1798	1799	1800	1	2	3	4	5	6	7	8	9	...	...	260	261	262	263	264	265	266	267	267			

Figure 13 – Dual Link Image Sample Mapping of the Y and C Channels

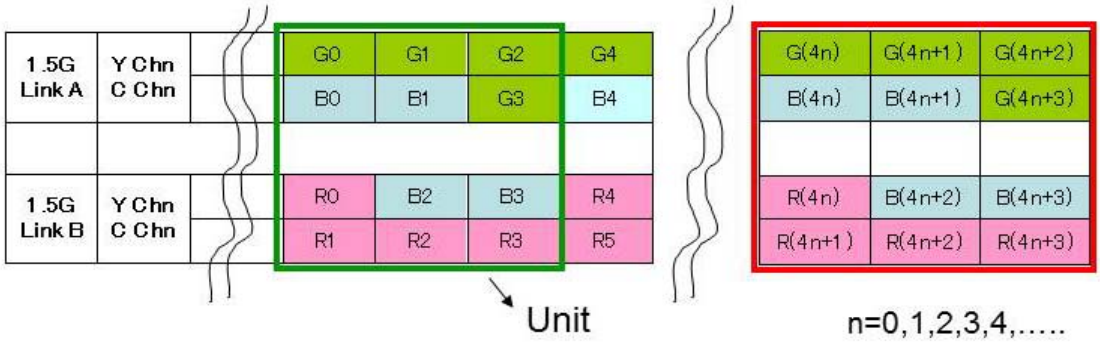

Figure 14 – Dual Link Mapping Rule

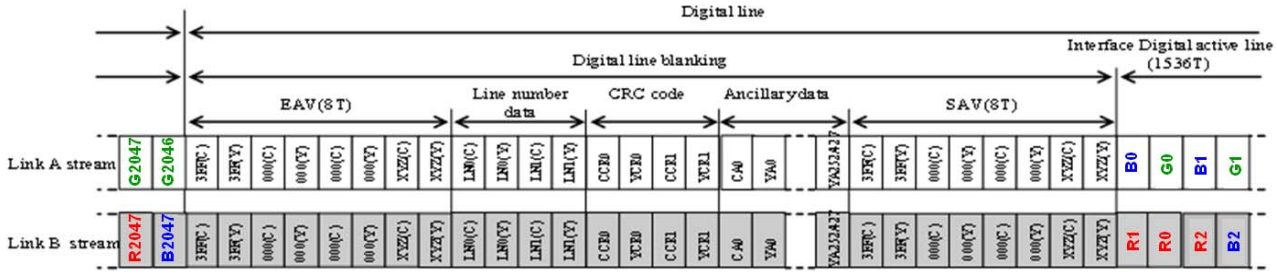

Figure 15 – Dual Link Data Stream

The interface sampling frequency shall be 74.25 MHz or 74.25/1.001 MHz. for Link A and Link B.

The image source line numbers1-778 shall be mapped to interface line numbers 16 thru 793inclusive (Field 1). Image source line numbers779 thru 1556 shall be mapped to interface line numbers 841-1618 inclusive (Field 2). See Figure 8.

The Y channel of link A shall contain all G image samples except where the sample number modulo 4 =3. For example, 0,1,2,4,5,6,8...2046. G Samples 3,7,11,...2047..shall be carried in the C Channel. See Figures 13 and 14.

The C channel of link A shall carry the B image samples as sample pairs 0-1, 4-5, 8-9...2046-2047. See Figures 13 and 14.

The Y channel of Link B shall carry single R samples interleaved with B sample pairs. R samples, 0,4,8,12...2040,2044. The B image sample pairs 2-3,6-7,10-11...2042-2043, 2046-2047. See Figures 13 and 14.

The C channel of link B shall carry R samples 1,2,3,5,6,7,9....2045, 2046, 2047. See Figures 13 and 14.

The PsF word number as indicated in Figure 13 is the word count for one complete horizontal line. Figure 6 represents the sample count of a horizontal line.

7 3 Gb/s Single-Link Mapping

The interface sampling Frequency shall be 148.5 MHz or 148.5/1.001 MHz.

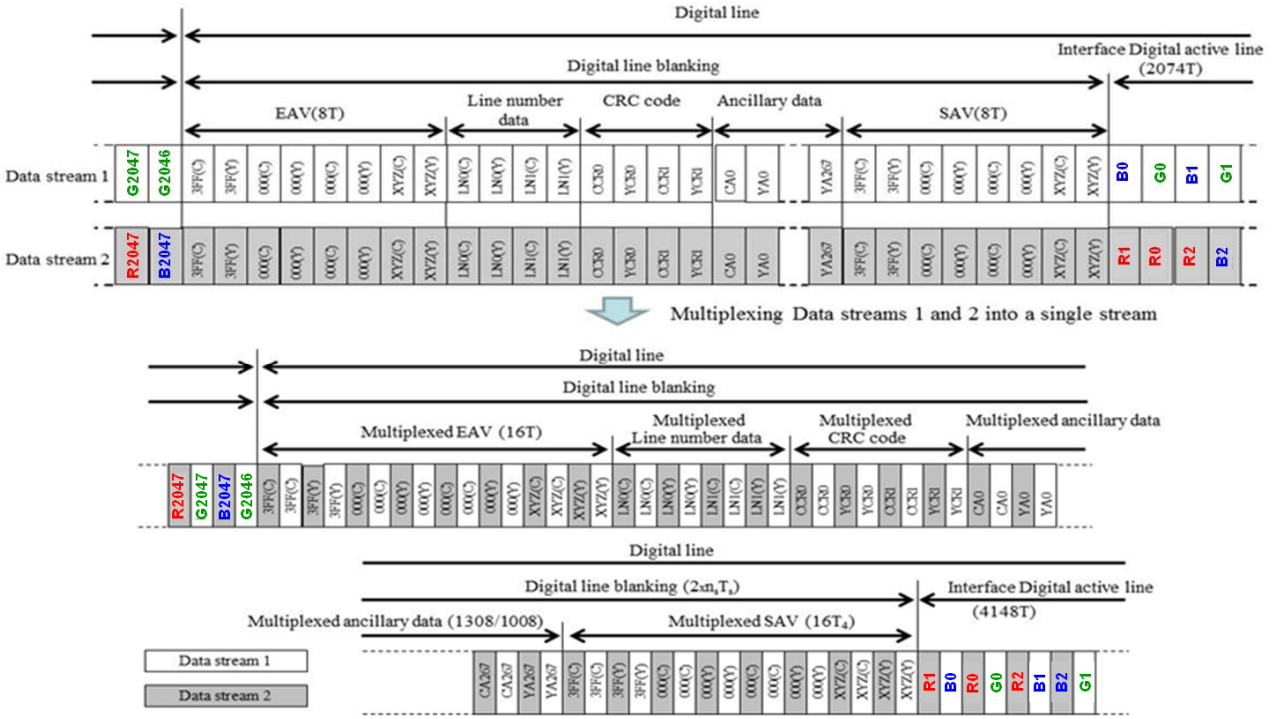

Figure 16 – 3 Gb/s Serial Data Stream

Two parallel 10-bit interfaces of the same line and frame structure having bit synchronization shall be mapped into a 20-bit Virtual Interface, consisting of two data streams — data stream one and data stream two. The image samples from data stream one and data stream two shall alternate, with the samples from data stream 2 appearing first. See Figure 16.

8 Audio

This RDD defines the mapping of 24-bit AES digital audio data and associated control information into the horizontal ancillary data space of the serial digital video interface defined in this RDD. The audio data are derived from AES3, hereafter referred to as AES audio. This RDD constrains the content carried by the AES3 interface to linear coded samples.

Audio sampled at a clock frequency of either 48 kHz or 96 kHz locked (synchronous) to video.

Audio channels are transmitted in groups of four, up to a maximum of 16 audio channels in the case of 48-kHz sampling, and up to a maximum of 8 audio channels in case of 96-kHz sampling. Each group is identified by a unique ancillary data ID.

Audio data packets are multiplexed (embedded) into the horizontal ancillary data space of the C data stream, and audio control packets are multiplexed into the horizontal ancillary data space of the Y data stream.

The modes of transmission carried in an audio data packet shall be the TWO-CHANNEL MODE at a sampling frequency of 48 kHz, and the SINGLE CHANNEL DOUBLE SAMPLING FREQUENCY MODE at the sampling

frequency of 96 kHz as defined in AES3. Audio data channels 1~4 (CH1~ CH4) carry two AES audio channel pairs (AES1 channel 1 and 2 and AES2 channel 1 and 2) in the case of 48 kHz sampling. For 96 kHz sampling, two successive samples of two AES audio channels (AES1 channel 1 1st and 2nd sample and AES2 channel 1 1st and 2nd sample) shall be carried.

The 48-kHz sampling audio data derived from two channel pairs shall be configured in an audio data packet as shown in Figure 17. Both channels of a channel pair are derived from the same AES audio source. The number of samples per channel used for one audio data packet shall be constant and is equal to one. The number of audio data packets in a given group shall be less than or equal to Na in a horizontal ancillary data block.

Figure 18 shows the audio data packet at the sampling rate of 96 kHz. AES sub frames 1 and 2 carry successive samples of the same AES audio signal. Both channels shall be derived from the same AES audio source. The number of samples per channel used for one audio data packet shall be constant and equal to two. The number of audio data packets in a given group is less than or equal to Na/2 in a horizontal ancillary data block.

Two types of ancillary data packets carrying AES audio information are defined. Each audio data packet shall carry all of the information in the AES bit stream as defined by AES3. The audio data packet shall be located in the horizontal ancillary data space of the C data stream. An audio control packet shall be transmitted once per field on interface lines 9 and 834. See Figure 8.

Data ID shall be defined for four separate packets of each packet type. This allows for up to eight channel pairs. In this RDD, the audio groups are numbered 1 through 4 and the channels are numbered 1 through 16. Channels 1 through 4 are in group 1, channels 5 through 8 are in group 2, and so on. Table 9 defines the relationship between CH1~CH4 (UDW2~UDW17) in the audio data packet and the channel/sample number for 48-kHz sampling and 96-kHz sampling, respectively.

The audio data packet and audio control packet shall be located in horizontal ancillary data space.

Audio data packets shall only be placed on interface line numbers 16 thru 795 inclusive and interface line numbers 841 thru 1620.

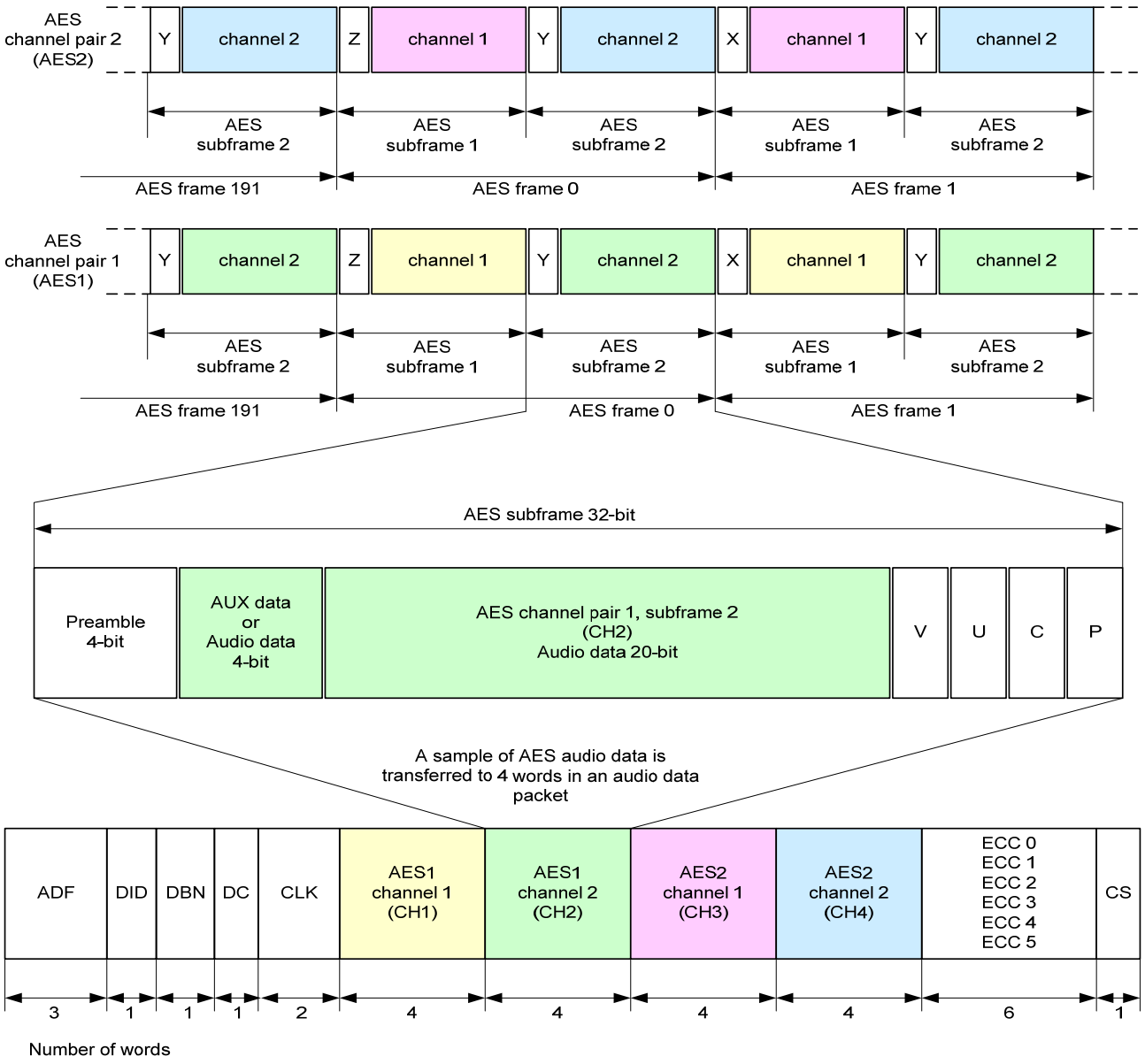

Figure 17 – Relationship between AES audio and audio data packets at sampling rate of 48 kHz

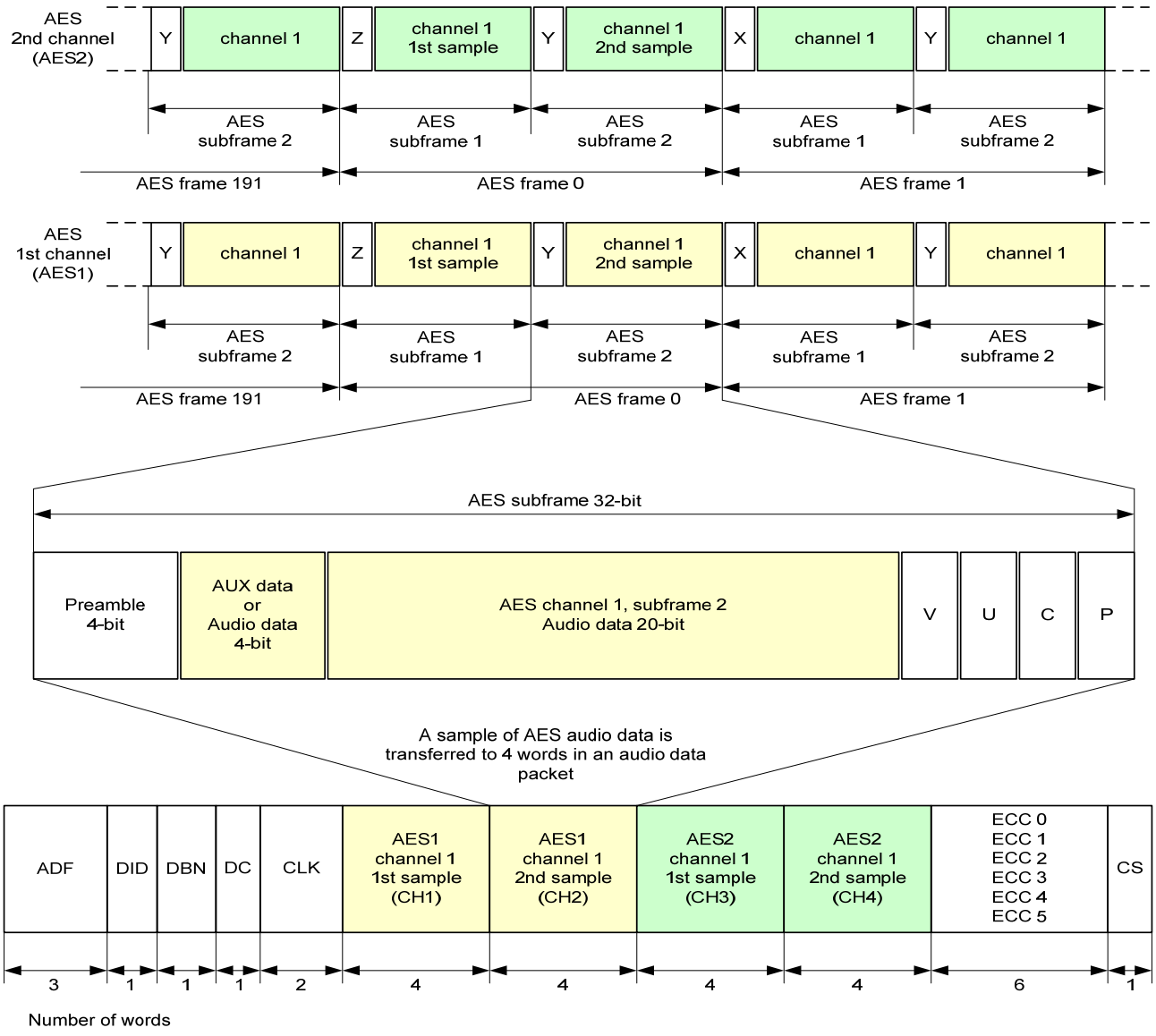

Figure 18 – Relationship between AES audio and audio data packets at a sampling rate of 96 kHz

Table 9 – Relationship between audio data packets and the channel/sample number of 48 kHz and 96 kHz sampling

	Audio Group 1			
Audio sampling rate	UDW2~UDW5 CH1	UDW6~UDW9 CH2	UDW10~UDW13 CH3	UDW14~UDW17 CH4
48.0 kHz	AES1 channel 1	AES1 channel 2	AES2 channel 1	AES2 channel 2
96.0 kHz	AES1 channel 1 1st sample	AES1 channel 1 2nd sample	AES2 channel 1 1st sample	AES2 channel 1 2nd sample

8.1 Structure of Audio Data Packet

The structure of the audio data packet shall be as shown in Figure 19. Audio data packets shall include ancillary data flag (ADF), data identification (DID), data block number (DBN), data count (DC), user data words (UDW) and checksum (CS) fields. DC is always 218h.

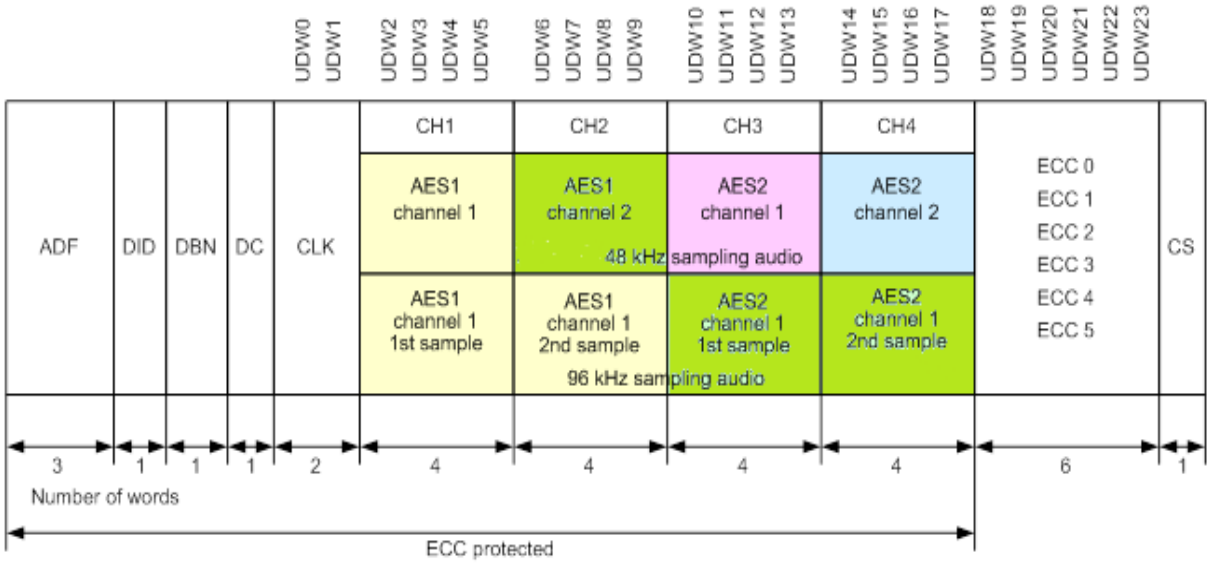

Figure 19 – Structure of audio data packets

The DID value shall be defined as 2E7h for audio group 1 (channel 1~4), 1E6h for audio group 2 (channel 5~8), 1E5h for audio group 3 (channel 9-12) and 2E4h for audio group 4 (channel 13~16), respectively.

In this RDD, UDWx means the xth user data word. There shall always be 24 words in the UDW of an audio data packet; i.e., UDW0, UDW1 … UDW22, UDW23.

All audio channels in a given audio group shall have identical sampling rate, identical sampling phase and identical synchronous/asynchronous status.

For a given audio data packet, one sample of the audio data of each channel (CH1~CH4) shall be transmitted. Even when only one of the four channels (CH1~CH4) is active, all audio data of the 4 channels shall be transmitted. In such case, the value of audio data, V, U, C and P bits of all inactive channels shall be set to zero.

8.2 Structure of User Data Words (UDW)

The description in this section covers only audio group 1. The description for audio groups 2, 3 and 4 is similar to that for audio group 1 where channels 5, 9 and 13 correspond to channel 1; channels 6, 10 and 14 correspond to channel 2; channels 7, 11 and 15 correspond to channel 3; and channels 8, 12 and 16 correspond to channel 4, respectively.

8.2.1 CLK (audio clock phase data)

Bit assignment of CLK shall be as shown in Table 10. Valid CLK data is required.

Table 10 – Bit assignment of CLK

Bit number	UDW0	UDW1
b9 (MSB)	Not b8	Not b8
b8	Even parity [1)]	Even parity [1)]
b7	ck7 audio clock phase data	Reserved (set to 0)
b6	ck6 audio clock phase data	Reserved (set to 0)
b5	ck5 audio clock phase data	ck12 audio clock phase data (MSB)
b4	ck4 audio clock phase data	mpf multiplex position flag
b3	ck3 audio clock phase data	ck11 audio clock phase data
b2	ck2 audio clock phase data	ck10 audio clock phase data
b1	ck1 audio clock phase data	ck9 audio clock phase data
b0 (LSB)	ck0 audio clock phase data (LSB)	ck8 audio clock phase data

[1)] Even parity for b0 through b7.

The bits of ck0 to ck12 shall indicate the number of video clocks between the first word of EAV and the video sample at the same time that audio sample appears at the input of the formatter. For example, the value of ck0~12 is in the range of 0 to 8191 for systems that use 74.25-MHz or 74.25/1.001-MHz clocks.

In the case of 96-kHz sampling, CLK (the audio clock phase data) indicates the number of video clocks between the first word of EAV and the video sample at the same time that the second audio sample of the successive two samples of the same AES audio signal appears at the input of the formatter.

The formatter shall place the audio data packet in the horizontal ancillary data space following the video line during which the audio sample occurred.

Flag bit *mpf* defines the audio data packet position in the multiplexed output stream relative to the associated video data.

When bit mpf = 0, it shall indicate that the audio data packet is located immediately after the video line during which the audio sample occurred.

When bit mpf = 1, it shall indicate that the audio data packet is located in the second line following the video line during which the audio sample occurred.

The relationship between the multiplex position flag (mpf) and the multiplex position of the audio data packet is shown in Figure 20 and Figure 8.

In the case of 96-kHz sampling, mpf shall be defined according to the position of the second sample of the successive two samples of the same AES audio signal.

8.2.1.1 CHn (audio data)

The bit assignment of CHn (n = 1~4) shall be as shown in Table 11. All bits of an AES sub frame shall be transparently transferred to four consecutive UDW words (UDW4n-2, UDW4n-1, UDW4n, UDW4n+1). UDW2 through UDW17 are always used for CHn in audio data packets.

Bit 3 of UDW2 and UDW10 indicates the status of the Z flag which corresponds to the AES block sync. The Z flag bit in UDW2 shall be associated with CH1 and CH2, and the Z flag bit in UDW10 shall be associated with CH3 and CH4,

Bits b0 through b2 in UDW2, UDW6, UDW10 and UDW14, and bit b3 in UDW6 and UDW14 shall be set to zero.

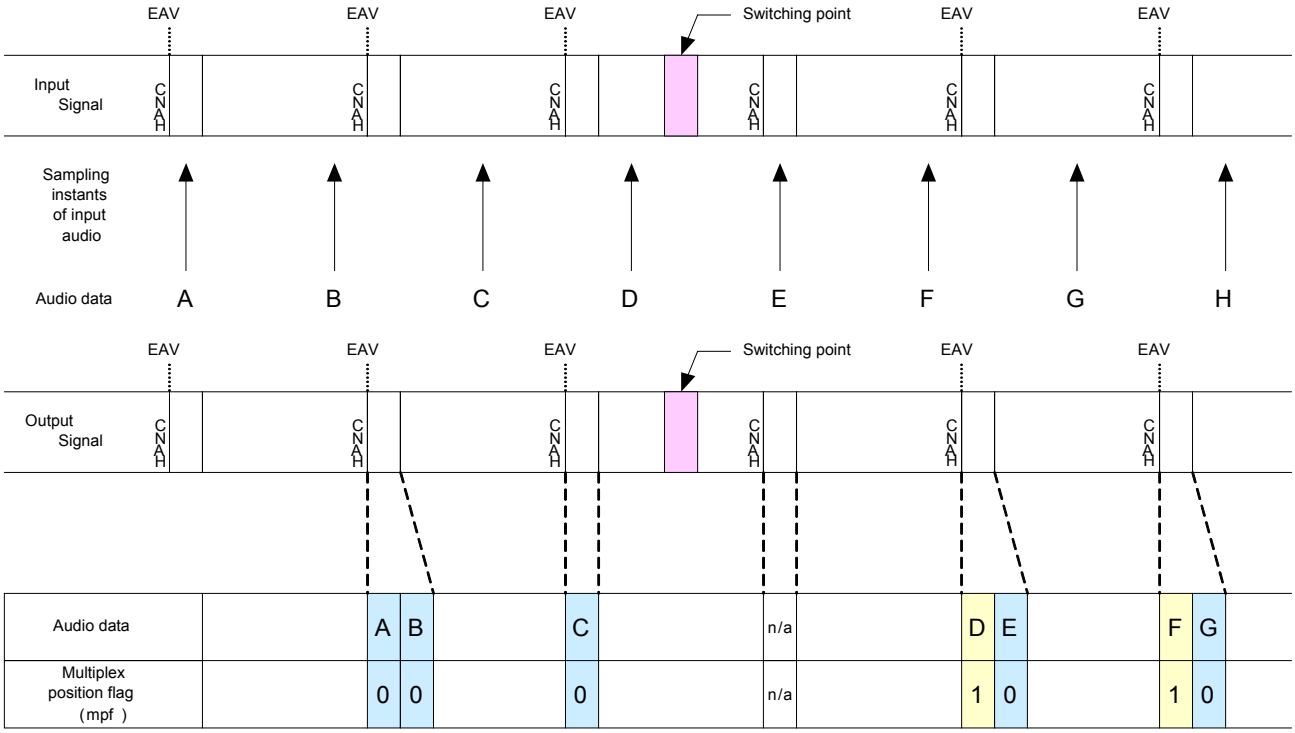

Figure 20 – Relationship between the multiplex position flag (mpf) and the multiplex position of 48 kHz sampling audio data packets

Notes:

1. For example, for samples A, B, C, E and G, mpf = 0 because the ancillary data packet is multiplexed in the horizontal ancillary data space of the next line relative to the input timing of the audio sample.

2. N/A shows that the line subsequent to the switching point precludes the insertion of ancillary data packets.

3. For example, for samples D and F, mpf = 1 because the ancillary data packet is multiplexed in the horizontal ancillary data space of the second line relative to the input timing of the audio sample.

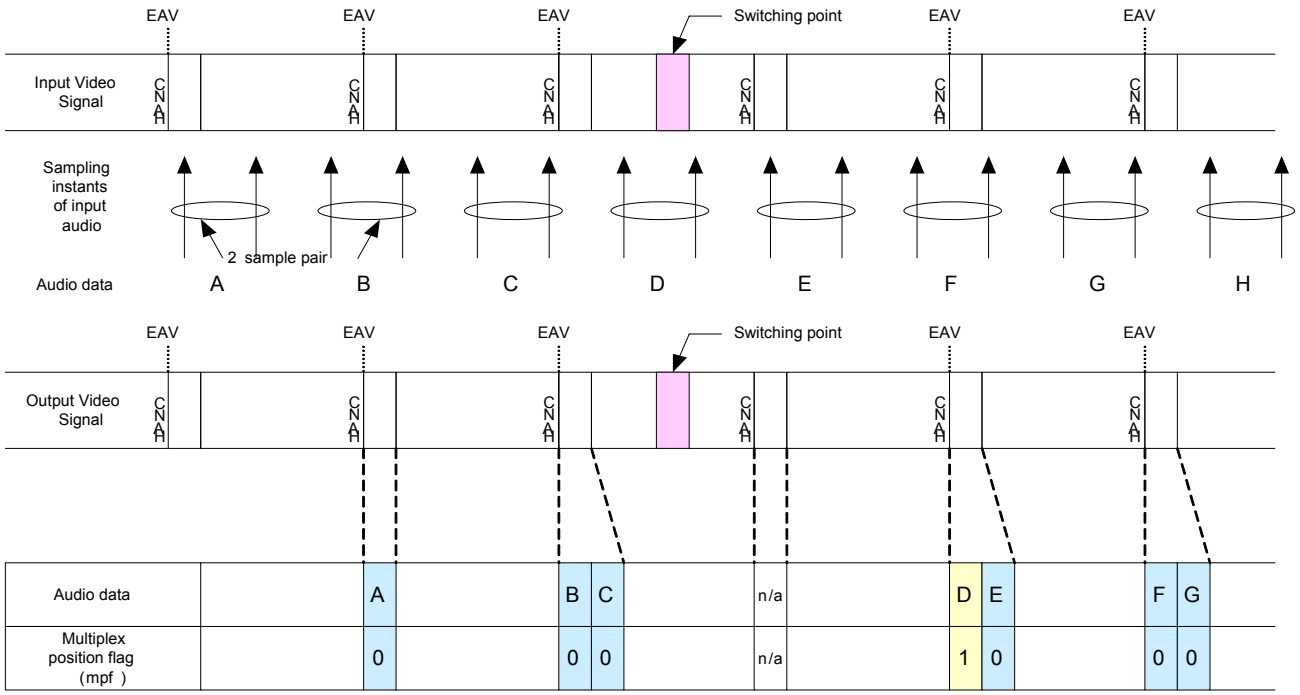

Figure 21 – Relationship between the multiplex position flag (mpf) and the multiplex position of 96 kHz sampling audio data packets

Notes:

1. For example, for samples A, B, C, E, F and G, mpf = 0 because the ancillary data packet is multiplexed in the horizontal ancillary data space of the next line relative to the input timing of the audio sample.

2. N/A shows that the line subsequent to the switching point precludes the insertion of ancillary data packets.

3. For example, for samples D, mpf = 1 because the ancillary data packet is multiplexed in the horizontal ancillary data space of the second line relative to the input timing of the audio sample

Table 11 – Bit-assignment of audio data (CHn)

CH1	Bit number	UDW2	UDW3	UDW4	UDW5
	b9 (MSB)	Not b8	Not b8	Not b8	Not b8
	b8	Even parity [1]	Even parity [1]	Even parity [1]	Even parity [1]
	b7	aud_1 3	aud_1 11	aud_1 19	P_1
	b6	aud_1 2	aud_1 10	aud_1 18	C_1
	b5	aud_1 1	aud_1 9	aud_1 17	U_1
	b4	aud_1 0 (LSB)	aud_1 8	aud_1 16	V_1
	b3	Z	aud_1 7	aud_1 15	aud_1 23(MSB)
	b2	0	aud_1 6	aud_1 14	aud_1 22
	b1	0	aud_1 5	aud_1 13	aud_1 21
	b0 (LSB)	0	aud_1 4	aud_1 12	aud_1 20
CH2	Bit number	UDW6	UDW7	UDW8	UDW9
	b9 (MSB)	Not b8	Not b8	Not b8	Not b8
	b8	Even parity [1]	Even parity [1]	Even parity [1]	Even parity [1]
	b7	aud_2 3	aud_2 11	aud_2 19	P_2
	b6	aud_2 2	aud_2 10	aud_2 18	C_2
	b5	aud_2 1	aud_2 9	aud_2 17	U_2
	b4	aud_2 0 (LSB)	aud_2 8	aud_2 16	V_2
	b3	0	aud_2 7	aud_2 15	aud_2 23(MSB)
	b2	0	aud_2 6	aud_2 14	aud_2 22
	b1	0	aud_2 5	aud_2 13	aud_2 21
	b0 (LSB)	0	aud_2 4	aud_2 12	aud_2 20
CH3	Bit number	UDW10	UDW11	UDW12	UDW13
	b9 (MSB)	Not b8	Not b8	Not b8	Not b8
	b8	Even parity [1]	Even parity [1]	Even parity [1]	Even parity [1]
	b7	aud_3 3	aud_3 11	aud_3 19	P_3
	b6	aud_3 2	aud_3 10	aud_3 18	C_3
	b5	aud_3 1	aud_3 9	aud_3 17	U_3
	b4	aud_3 0 (LSB)	aud_3 8	aud_3 16	V_3
	b3	Z	aud_3 7	aud_3 15	aud_3 23(MSB)
	b2	0	aud_3 6	aud_3 14	aud_3 22
	b1	0	aud_3 5	aud_3 13	aud_3 21
	b0 (LSB)	0	aud_3 4	aud_3 12	aud_3 20
CH4	Bit number	UDW14	UDW15	UDW16	UDW17
	b9 (MSB)	Not b8	Not b8	Not b8	Not b8
	b8	Even parity [1]	Even parity [1]	Even parity [1]	Even parity [1]
	b7	aud_4 3	aud_4 11	aud_4 19	P_4
	b6	aud_4 2	aud_4 10	aud_4 18	C_4
	b5	aud_4 1	aud_4 9	aud_4 17	U_4
	b4	aud_4 0 (LSB)	aud_4 8	aud_4 16	V_4
	b3	0	aud_4 7	aud_4 15	aud_4 23(MSB)
	b2	0	aud_4 6	aud_4 14	aud_4 22
	b1	0	aud_4 5	aud_4 13	aud_4 21
	b0 (LSB)	0	aud_4 4	aud_4 12	aud_4 20

Notes:

1 Even parity for b0 through b7.
2 Z = AES block sync.
3 Un = AES user bit of CHn.
4 Pn = AES parity bit of CHn.
5 aud (0-23) =24-bit AES audio data of CHn.
6 Vn = AES sample validity bit of CHn.
7 Cn = AES channel status bit of CHn.
8 Value of Vn, Un, Cn and Pn is equal to that of AES subframe, respectively.

8.2.2 ECC (Error correction codes)

ECC shall be used to correct or detect errors in 24 words from the first word of ADF through UDW17. The error correction code is BCH (31, 25) code. The BCH code shall be formed for each bit sequence of b0 – b7. The ECC shall consist of six words determined by the polynomial generator equation:

$$ECC(X) = (X+1)(X^5+X^2+1) = X^6+X^5+X^3+X^2+X+1$$

The initial value of all FFn shall be set to zero. The calculation shall start at the first word of ADF and shall end at the final word of CH4 (UDW17) for each bit of b0 to b7, respectively. The remaining data in the FFn shall be ECCn (n = 0~5).

Note: FFn is the flip flop number. For example, the data of FF0 is ECC0; and the data of FF5 is ECC5.

Bit assignment of ECC shall be as shown in Table 12. An example of the block diagram of the BCH-code information circuit is shown in Figure 22.

Table 12 – Bit assignment of ECC

	UDW18	UDW19	UDW20	UDW21	UDW22	UDW23
Bit number	ECC0	ECC1	ECC2	ECC3	ECC4	ECC5
b9 (MSB)	Not b8	Not b8	Not b8	Not b8	Not b8	Not b8
b8	Even parity [1)]	Even parity [1)]	Even parity [1)]	Even parity [1)]	Even parity [1)]	Even parity [1)]
b7	ecc0 7	ecc1 7	ecc2 7	ecc3 7	ecc4 7	ecc5 7
b6	ecc0 6	ecc1 6	ecc2 6	ecc3 6	ecc4 6	ecc5 6
b5	ecc0 5	ecc1 5	ecc2 5	ecc3 5	ecc4 5	ecc5 5
b4	ecc0 4	ecc1 4	ecc2 4	ecc3 4	ecc4 4	ecc5 4
b3	ecc0 3	ecc1 3	ecc2 3	ecc3 3	ecc4 3	ecc5 3
b2	ecc0 2	ecc1 2	ecc2 2	ecc3 2	ecc4 2	ecc5 2
b1	ecc0 1	ecc1 1	ecc2 1	ecc3 1	ecc4 1	ecc5 1
b0 (LSB)	ecc0 0	ecc1 0	ecc2 0	ecc3 0	ecc4 0	ecc5 0

[1)] Even parity for b0 through b7.

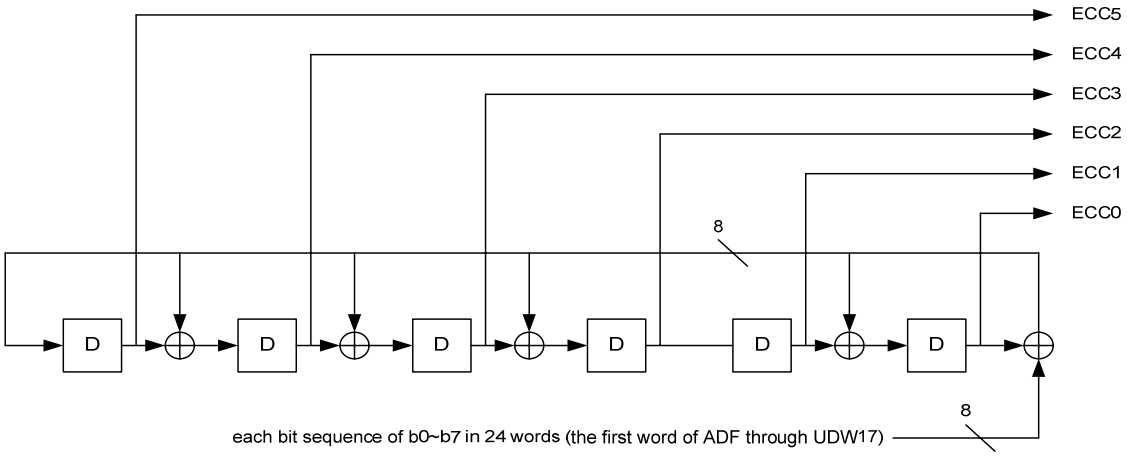

Figure 22 – Block diagram of the BCH-code formation circuitry (informative example)

8.3 Multiplexing of Audio Data Packet

Only the horizontal ancillary data space of the C channel data stream shall be used for transmission of the audio data packet.

The number of samples per audio channel which can be multiplexed in one horizontal ancillary data space shall be less than or equal to Na (Number of audio samples), where Na is defined in the following pseudo code:

```
No = Int (audio sample rate/line frequency) + 1
if (( No × (the number of total lines per video frame – the number of switching line per video frame)
   < (the number of audio samples per video frame)
then  Na = No + 1
else  Na = No
if (audio sampling rate == 96 kHz)  Na = Even (Na)
```

The function Even (n) returns the smallest even number that is greater than or equal to n. For example, Even (123) =124, Even (98) =98.

When two or more samples of the audio data are transmitted in one horizontal ancillary data block, the packet of the audio sample which appears earlier at the input of the formatter shall be transmitted first.

An audio data packet shall be multiplexed in the horizontal ancillary data space of the first or second line following the line during which the audio sample occurred at the input of the formatter.

Audio phase shall be maintained across the audio groups carrying multiple-channel audio.

The audio data packet shall be inserted following the CRC.

When more than two audio data packets are transmitted in one horizontal ancillary data block, the audio data packets shall be contiguous with each other.

8.3.1 Audio Control Packet

8.3.1.1 Structure of Audio Control Packet

The structure of the audio control packet shall be as shown in Figure 23. Audio control packets shall include ancillary data flag (ADF), data identification (DID), data block number (DBN), data count (DC), user data words (UDW) and checksum (CS) fields. DC is always $10B_h$ and DBN is always 200_h.

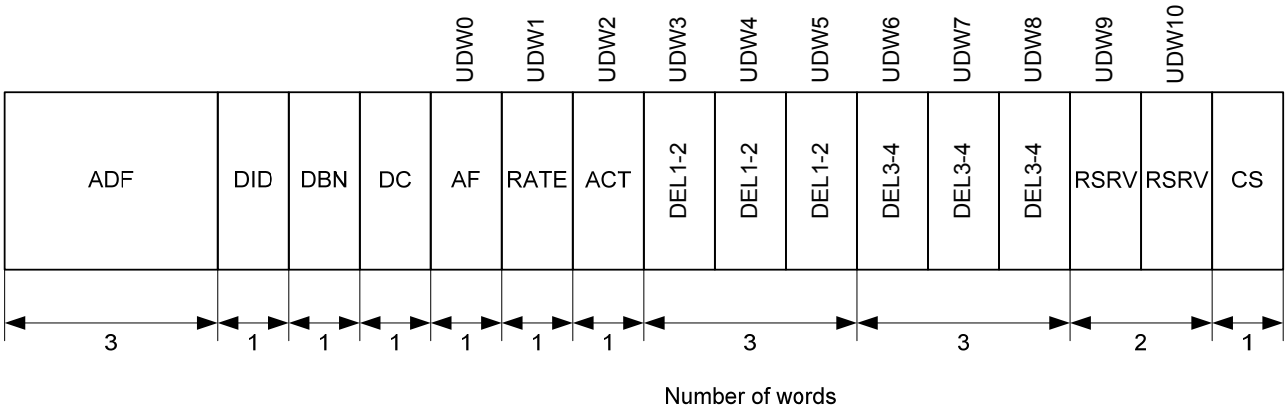

Figure 23 – Structure of audio control packet

The DID shall be defined as 1E3h for audio group 1 (channels 1~4), 2E2h for audio group 2 (channels 5~8), 2E1h for audio group 3 (channel 9~12) and 1E0h for audio group 4 (channel 13~16), respectively.

In this RDD, UDWx means the xth user data word. There shall be always 11 words in the UDW of an audio control packet; i.e., UDW0, UDW1 … UDW9, UDW10.

8.3.2 Structure of User Data Words (UDW)

The UDW consists of five types of data defined in Section 8.2.2.1 through Section 8.2.2.4. The description in this section covers only audio group 1. The description for audio groups 2, 3 and 4 is similar to audio group 1 where channels 5, 9 and 13 correspond to channel 1; channels 6, 10 and 14 correspond to channel 2; channels 7, 11 and 15 correspond to channel 3; channels 8, 12 and 16 correspond to channel 4, respectively.

8.3.2.1 AF (audio frame number data)

The Audio frame number data (AF) provides a sequential numbering of audio frames to indicate where they fall in the progression of non-integer number of samples per video frame (audio frame sequence). The first number of the sequence shall be always 1 and the final number shall be equal to the length of the audio frame sequence. A value of AF equal to all zeros shall indicate that frame numbering is not available.

The bit-assignment of the AF shall be as shown in Table 13. The AF shall be a common value for all channels in a given audio group.

Table 13 – Bit-assignment of AF

Bit number	UDW0
	AF
b9 (MSB)	not b8
b8	f8 audio frame number (MSB)
b7	f7 audio frame number
b6	f6 audio frame number
b5	f5 audio frame number
b4	f4 audio frame number
b3	f3 audio frame number
b2	f2 audio frame number
b1	f1 audio frame number
b0 (LSB)	f0 audio frame number (LSB)

For correct use of the audio frame number, the audio frame sequence shall be defined. Two synchronous sampling rates are defined in this RDD All audio frame sequences shall be based on two integer numbers of samples per frame (m and m+1) with audio frame numbers starting at 1 and proceeding to the end of the sequence. Odd-numbered audio frame (1, 3, 5, etc.) have the larger integer number of samples and even-numbered audio frames (2, 4, 6, etc.) have the smaller integer number of samples with the exception tabulated in Table 14.

Table 14 – Exceptions to audio frame sequences

Image Frame Rate	Audio Sampling rate (kHz)	Frame sequence	Basic numbering		Exceptions	
			Samples per odd audio frame (m)	Samples per even audio frame (m+1)	Frame number	Number of samples
25Hz	96.0	1	3840		none	
	48.0	1	1920		none	
24Hz	96.0	1	4000		none	
	48.0	1	2000		none	
24/1.001 frame/s	96.0	5	4004	4002 [1)]	none	
	48.0	5	2002	2001	none	

[1)] Successive samples are carried in audio data packet.

8.3.2.2 RATE (Sampling rate)

The sampling rate for all channel pairs is defined by the word RATE. The bit assignment of RATE shall be as shown in Table15.

Table 15 – Bit assignment of RATE

Bit number	UDW1
	RATE
b9 (MSB) b8 b7 b6 b5 b4 b3 b2 b1 b0 (LSB)	not b8 Reserved (set to 0) Reserved (set to 0) Reserved (set to 0) Reserved (set to 0) Reserved (set to 0) X2 (MSB) X1 Rate code X0 (LSB) asx 0 = synchronous audio 1 = Reserved

For this RDD the sync mode bit asx, shall be set to 0, and shall indicate that the channel pairs in a given audio group are operating synchronously

The rate code shall be as defined in Table 16.

Table 16 – Assignment of rate code

X2	X1	X0	Sample rate
0	0	0	48.0 kHz
0	0	1	Reserved
0	1	0	Reserved
1	0	0	96.0 kHz
0	1	1	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

8.3.2.3 ACT (Active Channels)

The word ACT shall indicate the active channels. Bits a1 to a4 shall be set to one for each active channel in a given audio group; otherwise, they shall be set to zero. The bit assignment of ACT shall be as defined in Table 17.

Table 17 – Bit assignment of ACT

Bit number	UDW2
	ACT
b9 (MSB)	Not b8
b8	Even parity [1)]
b7	Reserved (set to 0)
b6	Reserved (set to 0)
b5	Reserved (set to 0)
b4	Reserved (set to 0)
b3	a4 active: 1, inactive: 0 (CH4)
b2	a3 active: 1, inactive: 0 (CH3)
b1	a2 active: 1, inactive: 0 (CH2)
b0 (LSB)	a1 active: 1, inactive: 0 (CH1)

1) Even parity for b0 through b7.

8.3.2.4 DELm-n (Audio Delay Data)

The words DELm-n shall indicate the amount of accumulated audio processing delay relative to video, measured in audio sample intervals, for each channel pair of CHm and CHn.

In the case of 96 kHz sampling, DELm-n shall indicate the amount of accumulated audio processing delay relative to video measured in audio sample intervals for the successive two samples of the same AES audio signal carried in CH1, CH2 and CH3, CH4.

The bit assignment of DELm-n shall be as shown in Table 18. The e bit shall be set to one to indicate valid audio delay data otherwise it shall be zero. The delay words are referenced to the point where the AES-3 data are input to the formatter. The delay words shall represent the average delay value, inherent in the formatting process, over a period no less than the length of the audio frame sequence plus any preexisting audio delay.

Table 18 – Bit assignment of DELm-n

Bit number	UDW3	UDW4	UDW5	UDW6	UDW7	UDW8
	DEL1-2			DEL3-4		
b9 (MSB)	Not b8	Not b8	Not b8	Not b8	Not b8	Not b8
b8	del 7	del 16	del 25 (±)	del 7	del 16	del 25 (±)
b7	del 6	del 15	del 24 (MSB)	del 6	del 15	del 24 (MSB)
b6	del 5	del 14	del 23	del 5	del 14	del 23
b5	del 4	del 13	del 22	del 4	del 13	del 22
b4	del 3	del 12	del 21	del 3	del 12	del 21
b3	del 2	del 11	del 20	del 2	del 11	del 20
b2	del 1	del 10	del 19	del 1	del 10	del 19
b1	del 0 (LSB)	del 9	del 18	del 0 (LSB)	del 9	del 18
b0 (LSB)	*e*	del 8	del 17	*e*	del 8	del 17

The audio delay data (del 0 – del 25) shall be represented in the format of 26-bit two's complement. Positive values shall indicate that the video leads the audio.

8.3.3 Multiplexing of the Audio Control Packets

The audio control packets shall be transmitted once every interface field.

The audio control packets shall be transmitted in the horizontal ancillary data space of line 15 and 840 of the Y data stream.

9 Time Code

In this RDD the acronym ATC refers to the time code data carried within an ANC packet in Horizontal Ancillary space of the serial bit stream, and is used to convey time code data formatted as LTC, and VITC.

The time code data is encapsulated into an ATC packet. Time code may be carried as either LTC or VITC as shown in Figure 8. This RDD does not define any system physical interfaces; it only describes the data to be encapsulated, and the data format and location of the ANC packet within the serial interface.

9.1 25 Frame Operation

Each frame shall be identified by a unique and complete address consisting of an hour, minute, second and frame number. The hours, minutes, and seconds follow the ascending progression of a 24 h clock beginning with 0 h 0 min 0 s to 23 h 59 min 59 s. The frames shall be numbered successively 0 through 24. In addition where VITC is used the field flag shall be set once every field of the serial interface. A logical zero shall represent field 1, a logical one shall represent field 2.

9.2 24, 24/1.001 Frame Operation

Each frame shall be identified by a unique and complete address consisting of an hour, minute, second and frame number. The hours, minutes, and seconds follow the ascending progression of a 24 h clock beginning with 0 h 0 min 0 s to 23 h 59 min 59 s. The frames shall be numbered successively 0 through 23. In addition where VITC is used the field flag shall be set once every field of the serial interface.

9.3 Linear Time Code (LTC) Structure

9.3.1 Codeword format

Each LTC codeword consists of 80 bits numbered 0 through 79. The bits are generated serially beginning with bit 0. Bit 79 of the codeword is followed by bit 0 of the next codeword. Each codeword is associated with a frame. The digital code consists of sixteen 4-bit groups, eight groups containing time address and flag bits, and eight 4-bit binary groups for user-defined data and control codes. This RDD does not use user defined data and control codes, these bits shall be set to 0.

9.3.2 Codeword data content

Each LTC codeword contains the time address of the frame, flag bits, binary groups, biphase mark polarity correction bit and a synchronization word. See Table 19

9.3.3 Flag bits

This RDD makes no uses of the Flag bits other than the interface field flag identifier. Flag bits shall be set to 0.

9.3.4 Timing of the codeword relative to the image

The insertion of the data packet into the Serial interface of the LTC value shall have a latency of one frame.

9.4 Vertical Interval Timecode (VITC)

9.4.1 Codeword format

Each codeword shall consist of 90 bits numbered 0 through 89, organized as 9 groups of 10 bits. Each 10-bit group starts with a synchronization bit pair, which is a bit 1 followed by a bit 0. The synchronization bit pair is followed by 8 data bits.

The first eight groups contain the 64 time and control code data bits; the ninth contains a cyclic redundancy check (CRC) code used to detect errors in the data. The boundaries of the word are defined as the leading edge of the first bit (bit 0) and the trailing edge of the last bit (bit 89). Since bit 0 is the first synchronization bit of the codeword, it shall always have the value of one.

9.4.2 Codeword data content

Each VITC codeword consists of a time address, flag bits, binary groups, field mark flag, CRC code and synchronization bits.

9.4.3 Time address

The lowest numbered bit of each group corresponds to the least significant bit of each BCD digit.

9.4.4 Flag bits

The positions of these are shown in table 19.This RDD does not make any use of these flag bits. The flag bits shall be set to zero.

9.4.5 Binary groups

The positions of these bits are shown in Table 19.

9.4.6 Interface-Field flag

The Interface field identification shall be indicated as follows: A zero shall represent field 1 of the interface. A one shall represent field 2 of the interface. Field 1 contains image lines 1 through 778 inclusive; field 2 contains lines 779 through 1556.

Table 19 – VITC and LTC codeword bit definitions

VITC BIT NO.	VALUE (WEIGHT)	COMMON ASSIGNMENT	LTC BIT NO.	25-FRAME/	24-FRAME/
0	1	VITC SYNC BITS			
1	0				
2	(1)	FRAME UNITS	0		
3	(2)		1		
4	(4)		2		
5	(8)		3		
6	(LSB)	FIRST BINARY GROUP	4		
7	|		5		
8	|		6		
9	(MSB)		7		
10	1	VITC SYNC BITS			
11	0				
12	(10)	FRAME TENS	8		
13	(20)		9		
14	FLAG	FLAG	10	UNUSED BIT	UNUSED BIT
15	FLAG	FLAG	11	Unused Bit	UNUSED BIT
16	(LSB)	SECOND BINARY GROUP	12		
17	|		13		
18	|		14		
19	(MSB)		15		
20	1	VITC SYNC BITS			
21	0				

22	(1)	SECOND UNITS	16		
23	(2)		17		
24	(4)		18		
25	(8)		19		
26	(LSB)	THIRD BINARY GROUP	20		
27	|		21		
28	|		22		
29	(MSB)		23		
30	1	VITC SYNC BITS			
31	0				
32	(10)	SECOND TENS	24		
33	(20)		25		
34	(40)		26		
35	FLAG	FLAG	27	BINARY GROUP FLAG 0 Not Used Set to zero	Not Used set to Zero
36	(LSB)	FOURTH BINARY GROUP	28		
37	|		29		
38	|		30		
39	(MSB)		31		
40	1	VITC SYNC BITS			
41	0				
42	(1)	MINUTE UNITS	32		
43	(2)		33		
44	(4)		34		
45	(8)		35		
46	(LSB)	FIFTH BINARY GROUP	36		
47	|		37		
48	|		38		
49	(MSB)		39		
50	1	VITC SYNC BITS			
51	0				
52	(10)	MINUTE TENS	40		
53	(20)		41		
54	(40)		42		
55	FLAG	FLAG	43	BINARY GROUP FLAG 2	BINARY GROUP FLAG 0
56	(LSB)	SIXTH BINARY GROUP	44		
57	|		45		
58	|		46		
59	(MSB)		47		
60	1	VITC SYNC BITS			
61	0				
62	(1)	HOUR UNITS	48		
63	(2)		49		
64	(4)		50		
65	(8)		51		
66	(LSB)	SEVENTH BINARY GROUP	52		
67	|		53		
68	|		54		
69	(MSB)		55		
70	1	VITC SYNC BITS			
71	0				
72	(10)	HOUR TENS	56		
73	(20)		57		
74	FLAG	FLAG	58	BINARY GROUP FLAG 1	BINARY GROUP FLAG 1
75	FLAG	FLAG	59	FIELD BIT/LTC POLARITY	BINARY GROUP FLAG 2
76	(LSB)	EIGHTH BINARY GROUP	60		
77	|		61		
78	|		62		
79	(MSB)		63		
80	1	VITC SYNC BITS			
81	0				
82-89		VITC CRC CODE			
		LTC SYNC WORD	64-79		

Note: For this RDD, there is no color frame flag used.

9.5 Format of Ancillary Time Code Packets

The ANC packet consists of the ancillary data flag (ADF), the data ID (DID), the secondary data ID (SDID), the data count (DC), the user data words (UDW), and the checksum (CS). The UDW consists of the data payload.

The DID and SDID shall be set to:

DID 60_h
SDID 60_h

The data count word for ancillary time code shall be set to:

DC 10_h

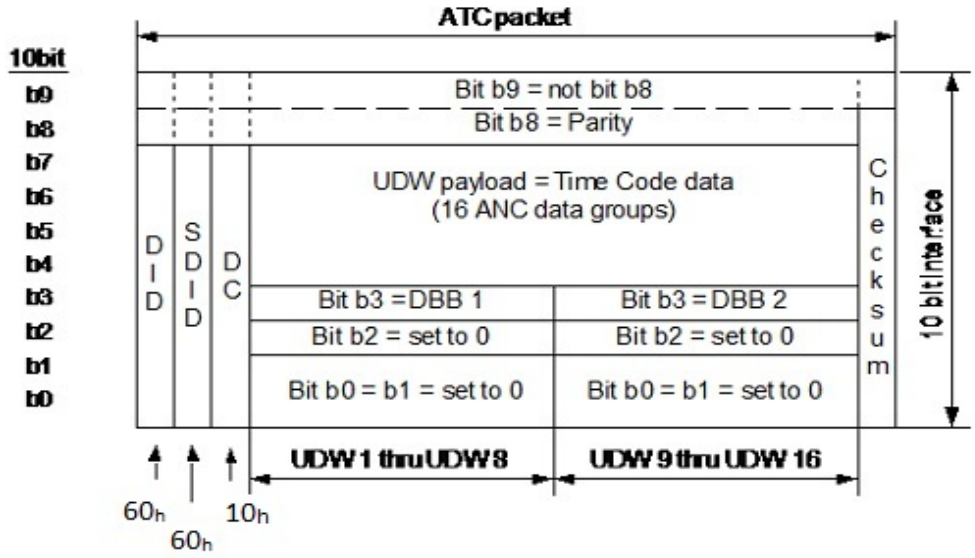

Figure 24 – Ancillary Time Code Packet format

9.6 Ancillary Time Code Packet Layout

One ancillary data packet shall fully represent an ancillary time code (ATC) codeword. See Figure 24.

All User Data Words of the Ancillary Time Code packets are formatted as shown in Table 20.

Table 20 – User Data Word (UDW) format

UDW bit (10-bit words)	Assignment
b0 (LSB)	Set to 0
b1	Set to 0
b2	Set to 0
b3	Distributed binary bit (DBB)
b4	ANC binary group LSB
b5	ANC binary group
b6	ANC binary group
b7	ANC binary group MSB
b8	10-bit - Even parity for data contained in UDW bit 7 through bit 0
b9 (MSB)	10-bit - Not bit 8

9.7 Format of User Data Words in Ancillary Time Code Packet

9.7.1 Bit Assignments within the UDW

9.7.1.1 UDW Bits b9 and b8

Bits b9 shall equal not b8, and b8 shall be the even parity for bits b7 through b0.

9.7.1.2 UDW Bits b7 through b4

Bits b7 through b4 of UDW-1 through UDW-16 shall form an array of ancillary data groups into which the time code code-words shall be mapped. Bit b4 of each UDW represents the LSB of each group. See Table 22.

9.7.1.3 UDW Bit b3

Two groups of control bits shall be distributed across Bit b3 of UDW-1 through UDW-16. See Figure 24.

9.7.1.4 UDW Bits b2 through b0

Bits b2 through b0 shall be set to zero.

9.8 Distributed Binary Bits (DBB)

Bit b3 of UDW-1 through UDW-16 shall form two groups of distributed binary bits known as DBB1 and DBB2. Information coded in the DBB1 is defined in Table 21 and is illustrated in Figure 24.

9.8.1 DBB1 – Payload Type

The first group of distributed binary bits (DBB1) shall be formed by bit 3 of UDW-1 through UDW-8, where UDW-1 (b3) represents the LSB and UDW-8 (b3) represents the MSB. The DBB1 bits shall define what type of data is being carried in the time code bits (b7 to b4) of the UDW as defined in Table 21.

9.8.1.1 Ancillary Time Code Linear Code Payload Type

The acronym “ATC_LTC” refers to ATC packets that carry linear time code (LTC) code-words and have the distributed binary bit group 1 (DBB1) value of 00h. See Table 21.

9.8.1.2 Ancillary Time Code Vertical Interval Code

The acronym “ATC_VITC1” refers to ATC packets that carry vertical interval time code (VITC) and have the distributed binary bit group 1 (DBB1) value of 01h. See Table 21. The code-word contents shall be as shown in Table 22.

Table 21 – DBB1 (payload type) Distributed binary bit group coding

Bit 3 of UDW	Distributed binary bit (DBB1) MSB LSB	Definition
UDW-8 through UDW-1	0 0 0 0 0 0 0 0	Linear time code (ATC_LTC)
	0 0 0 0 0 0 0 1	Vertical interval time code (ATC_VITC)
	0 0 0 0 0 0 1 0	Not used in this RDD
	0 0 0 0 0 0 1 1 through 0 0 0 0 0 1 0 1	Reserved
	0 0 0 0 0 1 1 0	Reserved
	0 0 0 0 0 1 1 1	Reserved
	0 0 0 0 1 0 0 0 through 0 1 1 1 1 1 0 0	Reserved
	0 1 1 1 1 1 0 1	Reserved
	0 1 1 1 1 1 1 0	Reserved
	0 1 1 1 1 1 1 1	Reserved
	1 0 0 0 0 0 0 0 through 1 1 1 1 1 1 1 1	Reserved

9.8.1.3 DBB2

The second group of distributed binary bits (DBB2) is formed by bit 3 of UDW-9 through UDW-16, where UDW-9 (b3) represents the LSB and UDW-16 (b3) represents the MSB. DBB2 is not used by this RDD.

This RDD does not use DBB2, bits b7 through b0. These bits shall be set to 0.

9.8.2 Mapping of the Time Code Data into Ancillary Data Packets

Mapping of the time code data into the UDW-1 through UDW-16 of the ancillary time code data packet shall be as shown in Table 22.

Only the 64 information bits of the time code data shall be transferred to the ATC. The LTC sync word (bits 64-79) and the VITC (1/0) sync bit pairs and the CRC word shall be omitted from the ancillary time code packets.

Table 22 – Mapping of Time code Data into UDW

ATC		Time Code Data		
UDW	**Bit**	**LTC bit**	**VITC bit**	**Time code bit definitions**
1	4	0	2	Units of frames 1
	5	1	3	Units of frames 2
	6	2	4	Units of frames 4
	7	3	5	Units of frames 8
2	4	4	6	LSB binary group 1
	5	5	7	Not Used
	6	6	8	Not Used
	7	7	9	MSB binary group 1
3	4	8	12	Tens of frames 10
	5	9	13	Tens of frames 20
	6	10	14	Flag
	7	11	15	Flag
4	4	12	16	LSB binary group 2
	5	13	17	Not Used
	6	14	18	Not Used
	7	15	19	MSB binary group 2
5	4	16	22	Units of seconds 1
	5	17	23	Units of seconds 2
	6	18	24	Units of seconds 4
	7	19	25	Units of seconds 8
6	4	20	26	LSB binary group 3
	5	21	27	Not Used
	6	22	28	Not Used
	7	23	29	MSB binary group 3
7	4	24	32	Tens of seconds 10
	5	25	33	Tens of seconds 20
	6	26	34	Tens of seconds 40
	7	27	35	Flag

ATC		Time Code Data		
UDW	Bit	LTC bit	VITC bit	Time code bit definitions
8	4	28	36	LSB binary group 4
	5	29	37	Not Used
	6	30	38	Not used
	7	31	39	MSB binary group 4
9	4	32	42	Units of minutes 1
	5	33	43	Units of minutes 2
	6	34	44	Units of minutes 4
	7	35	45	Units of minutes 8
10	4	36	46	LSB binary group 5
	5	37	47	Not Used
	6	38	48	Not Used
	7	39	49	MSB binary group 5
11	4	40	52	Tens of minutes 10
	5	41	53	Tens of minutes 20
	6	42	54	Tens of minutes 40
	7	43	55	Flag
12	4	44	56	LSB binary group 6
	5	45	57	Not Used
	6	46	58	Not Used
	7	47	59	MSB binary group 6
13	4	48	62	Units of hours 1
	5	49	63	Units of hours 2
	6	50	64	Units of hours 4
	7	51	65	Units of hours 8
14	4	52	66	LSB binary group 7
	5	53	67	Not used
	6	54	68	Not used
	7	55	69	MSB binary group 7
15	4	56	72	Tens of hours 10
	5	57	73	Tens of hours 20
	6	58	74	Flag
	7	59	75	Flag
16	4	60	76	LSB binary group 8
	5	61	77	Not used
	6	62	78	Not used
	7	63	79	MSB binary group 8

9.8.3 Transmission of ancillary time code packets

Multiple transmissions of ancillary time code packets per interface field are permissible under the provisions of this RDD. See Figure 8.

9.8.4 ATC Packet Transmission Rate

Transmission of ancillary time code packets shall be at least once per Interface frame for a packet containing LTC code-words and once per interface field for a packet containing VITC code-words.

9.8.5 Ancillary Time Code Packet Location

Insertion of ancillary time code (ATC) packets shall be constrained to horizontal Ancillary data space of interface line numbers 9,10 and 834,835. The data shall be carried in the Y channel.

10 Payload Identifier

A payload identifier shall be placed on Line 10 and 835 of the Y channel in the Horizontal Ancillary data space as shown in Figure 7 and shall be present on every field of the interface. The payload Identifier shall be present on both links.

10.1 Ancillary Data Specification

The ancillary data packet used by the video payload identifier shall use a first data identification (DID) word followed by a secondary data identification (SDID) word. The DID word value shall be 41h, the SDID shall have a value of 01h. See Table 23.

Table 23 – Ancillary data packet structure for the video payload identifier

Name	Acronym	Value
Ancillary data flag (10-bit words)	ADF	000_h, $3FF_h$, $3FF_h$
Data identification	DID	41_h
Secondary data identification	SDID	01_h
Data count	DC	04_h
SDI video payload identifier	4 words	See table 24
Checksum	CS	—

The Video Payload Identified shall have the following data format. See Table 24.

Table 24 – Video payload identifier ancillary packet format

	10-bit data									
	b9 (MSB)	b8	b7	b6	b5	b4	b3	b2	b1	b0 (LSB)
Ancillary data flag (ADF)	0	0	0	0	0	0	0	0	0	0
	1	1	1	1	1	1	1	1	1	1
	1	1	1	1	1	1	1	1	1	1
Data ID (DID)	not b8	EP	0	1	0	0	0	0	0	1
Secondary data ID (SDID)	not b8	EP	0	0	0	0	0	0	0	1
Data count (DC)	not b8	EP	0	0	0	0	0	1	0	0
Video payload (byte 1)	not b8	EP	Version ID	Payload identifier						
Picture rate and scanning (byte 2)	not b8	EP	I/P transport	I/P picture	0	0	Picture rate			
Sampling structure (byte 3)	not b8	EP	0	0	0	0	Sampling structure			
Special options (byte 4)	not b8	EP	Channel 1/2		0	0	0	0	0	
Checksum	not b8	Sum of b0~b8 of DID through to payload byte 4.								

Table 25 – Payload ID for Dual Link Applications

Bits	Byte 1	Byte 2	Byte 3	Byte 4
Bit 7	1	Interlaced transport=0 1= Reserved	0= Reserved	0=Reserved
Bit 6	0	Progressive picture=1 0=Reserved	Horizontal Pixel Array 1= 2048 0= Reserved	Channel assignment = Ch1(0) or Ch2(1)
Bit 5	1	1=Reserved	0= Reserved	0=Reserved
Bit 4	1	1=Reserved	1=Reserved	1=Reserved
Bit 3	0	Image Frame rate 2h : 24/1.001 3h : 24 5h : 25 Other values Reserved	Sampling structure 1h: Y',C'_{Rr},C'_{B} 2h : RGB 7h : Rfs,Gfs,Bfs [1] Other values Reserved	1=Reserved
Bit 2	1			0= Reserved
Bit 1	0			Bit depth 1_h= 10-bit Other values Reserved
Bit 0	0			

[1] See Section 11 for information carried in the Color Anc data packet.

Byte 1 shall be set to (B4h).

Byte 2 –

The second byte shall be used to identify the picture rate and the picture and transport methods

- Bits 0-3 shall identify the Frame rate

  2h shall identify 24/1.001 Frames/sec

  3h Shall Identify 24 Frames/sec

  5h shall identify 25 Frames/sec

- Bit b7 shall be used to identify whether the digital interface uses a progressive or interlaced transport structure such that:

  0 identifies an interlaced transport

  1 is reserved

- Bit b6 shall be used to identify whether the picture has a progressive or interlaced structure such that.

  0 is reserved

  1 identifies a progressive structure

- Bits b5 and b4 shall be set to 0.

Byte 3 –

Byte 3 shall be used to identify the sampling structure and Horizontal pixel count of the video payload.

- Bit b6 shall be used to identify horizontal Pixel count

  0 reserved

  1 identifies 2048 Pixels

- Bits b4, b5, and b7 are reserved and set to 0.

- Bits b3 to b0 of byte 3 shall be used to identify the horizontal sampling structure

  1h: Y',C'_R,C'_B/4:2:2

  2h : RGB

  7h : Rfs,Gfs,Bfs [1]

  Other values are reserved and set to 0

[1] See Section 11 for information carried in the Color Anc data packet.

Byte 4 −

• The channel assignment in bit b6 of byte 4 shall be set to a value of (0) for channel 1 and to (1) for the channel 2.

• The bit depth of the sample quantization shall be identified by bits b1 and b0 of byte 4 having the following values:

0h reserved

1h identifies quantization using 10 bits per sample;

2h reserved.

3h reserved

Table 26 – Payload ID for 3 Gb/s Applications

Bits	Byte 1	Byte 2	Byte 3	Byte 4
Bit 7	1	Interlaced transport=0 1= Reserved	0= Reserved	0= Reserved
Bit 6	0	Progressive picture=1 0=Reserved	Horizontal Pixel Array 1= 2048 0= Reserved	Channel Assignment Ch1 (0h) or Ch2 (1h)
Bit 5	1	0= Reserved	0= Reserved	0 = Reserved
Bit 4	1	0= Reserved	0=Reserved	0 = Reserved
Bit 3	0	Image Frame rate 2h : 24/1.001 3h : 24 5h : 25 Other values Reserved	Sampling structure 1h: Y',C'$_{Rr}$,C'$_{B}$ 2h : RGB 7h : Rfs,Gfs,Bfs [2] Other values Reserved	0 = Reserved
Bit 2	1			0 = Reserved
Bit 1	0			Bit depth 1$_{h}$= 10-bit Other values Reserved
Bit 0	1			

Byte 1 shall be set to (B5h).

Byte 2 –

• The second byte shall be used to identify the picture rate and the picture and transport methods

Bits 0-3 shall identify the Frame rate

2h shall identify 24/1.001 Frames/sec

3h Shall Identify 24 Frames/sec

5h shall identify 25 Frames/sec

[2] See Section 11 for information carried in the Color Anc data packet

• Bit b7 shall be used to identify whether the digital interface uses a progressive or interlaced transport structure such that:

0 identifies an interlaced transport

1 is reserved

• Bit b6 shall be used to identify whether the picture has a progressive or interlaced structure such that.

0 is reserved

1 identifies a progressive structure

• Bits b5 and b4 shall be set to 0.

Byte 3 –

• Byte 3 shall be used to identify the sampling structure and Horizontal pixel count of the video payload

• Bit b6 shall be used to identify horizontal Pixel count

0 reserved

1 identifies 2048 Pixels

• Bits b4, b5, and b7 are reserved and set to 0.

• Bits b3 to b0 of byte 3 shall be used to identify the horizontal sampling structure

1h: Y',C'_R,C'_B/4:2:2

2h : RGB

7h : Rfs,Gfs,Bfs [1]

Other values are reserved and set to 0

Byte 4 –

• The bit depth of the sample quantization shall be identified by bits b1 and b0 of byte 4 having the following values:

0h reserved

1h identifies quantization using 10 bits per sample;

2h reserved.

3h reserved

• The channel assignment in bit b6 of byte 4 shall be set to a value of (0) for channel 1 and to (1) for channel 2

11 Color ANC Data Packet

The Color ANC data packet shall be carried on every field of the interface and shall be carried in the Horizontal Ancillary data space of line 9 and 834 as shown in Figure 8.

11.1 Structure of Color ANC

The structure of the Color ANC shall be as shown in Figure 25. Color ANC shall include ancillary data flag (ADF), data identification (DID), secondary data identification (SDID), data count (DC), user data words (UDW) and checksum (CS) it is always 266_h.

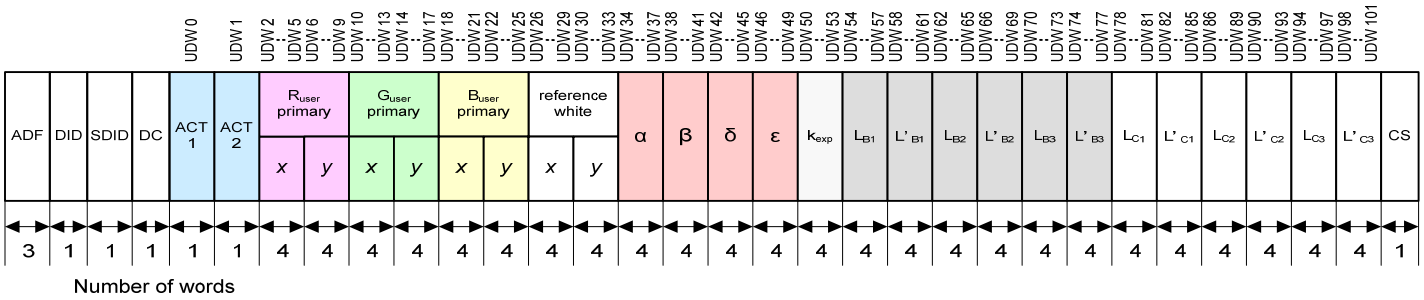

Figure 25 – Structure of Color ANC Packet

The DID value shall be defined as 41_h and the SDID value shall be 02_h.

11.2 Color ANC Packet UDW

In this RDD, UDWx shall mean the xth Color ANC word. There shall be always 102 words in the 0, UDW1…UDW101.

11.2.1 ACT1 Color Primary and Reference White Parameter

The word ACT1 shall indicate, which color primaries and reference white are being defined, i.e., FS-Gamut or the ones defined in Recommendation ITU-R BT.709. The bit assignment of ACT1 shall be as shown in Table 27.

Bits a1.0 or a1.1 shall be set to one for active FS-Gamut or color primaries and reference white defined in Recommendation ITU-R BT.709.

Bits a1.2 through a1.5 shall be set to one, when user defined tristimulus values (Ruser, Guser, Buser) and reference white are assigned, and shall be set to zero when default values of (RFS, GFS, BFS) or (R, G, B) primaries and reference white of FS-Gamut or the ones defined in Recommendation ITU-R BT.709 indicated with a1.0 and a1.1 are assigned.

Table 27 – Bit assignment of ACT1

Bit number	CDW0
	ACT1
b9 (MSB)	Not b8
b8	Even parity [1)]
b7	Reserved (set to 0)
b6	Reserved (set to 0)
b5	a1.5 active: 1, inactive: 0 (user defined reference white)
b4	a1.4 active: 1, inactive: 0 (user defined B_{user} primary)
b3	a1.3 active: 1, inactive: 0 (user defined G_{user} primary)
b2	a1.2 active: 1, inactive: 0 (user defined R_{user} primary)
b1	a1.1 active: 1, inactive: 0 (Color primaries and white defined in ITU-R BT.709)
b0 (LSB)	a1.0 active: 1, inactive: 0 (FS-Gamut defined in Table 2)

[1)] Even parity for b0 through b7

11.2.2 ACT2 Nonlinear Equation Specifier

The word ACT2 shall indicate which nonlinear equation, i.e., FS-Log curve or the gamma curve defined in Recommendation ITU-R BT.709, shall be used, and whether the upper three coordinates, lower three coordinates and the default value of kexp = 1.00000 shall be used or not. The bit assignment of ACT2 shall be as shown in Table 28.

Bit a2.0 or a2.1 shall be set to one for the active FS-Log curve or the gamma curve defined in Recommendation ITU-R BT.709.

Bits a2.2 and a2.3 shall be set to one for active upper and lower three coordinates. Bit a2.4 shall be set to one, when user defined value of kexp (≠ 1.00000) is assigned and shall be set to zero when default value of kexp = 1.00000 is assigned. Bits a2.2 through a2.4 shall be functional only when a2.0 is set to one, i.e., for active FS-Log curve.

If upper or lower three coordinates are not to be assigned, bit a2.2 or a2.3 shall be set to zero and upper or lower three coordinates values in the Color ANC shall be identified as invalid.

Table 28 – Bit assignment of ACT2

Bit number	CDW1
	ACT2
b9 (MSB)	Not b8
b8	Even parity [1)]
b7	Reserved (set to 0)
b6	Reserved (set to 0)
b5	Reserved (set to 0)
b4	a2.4 active: 1, inactive: 0 (user defined k_{esp} (≠ 1.00000))
b3	a2.3 active: 1, inactive: 0 (Lower three coordinates (L_{B1}, L'_{B1}), (L_{B2}, L'_{B2}), (L_{B3}, L'_{B3}))
b2	a2.2 active: 1, inactive: 0 (Upper three coordinates (L_{C1}, L'_{C1}), (L_{C2}, L'_{C2}), (L_{C3}, L'_{C3}))
b1	a2.1 active: 1, inactive: 0 (gamma curve defined in ITU-R BT.709)
b0 (LSB)	a2.0 active: 1, inactive: 0 (FS-Log curve defined in Equation 1 (α, β, δ, ε parameters))

[1)] Even parity for b0 through b7

11.2.2.1 Examples of ACT1 and ACT2 usage

Example.1) FS-Log curve with upper and lower three coordinates and default tristimulus values, default reference white and default k_{exp}:

	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
ACT1	0	1	0	0	0	0	0	0	0	1
ACT2	0	1	0	0	0	0	1	1	0	1

Parameter values of α, β, δ, ε, upper and lower three coordinates of (L_{C1}, L'_{C1}), (L_{C2}, L'_{C2}), (L_{B3}, L'_{C3}) and (L_{B1}, L'_{B1}), (L_{B2}, L'_{B2}), (L_{B3}, L'_{B3}) shall be mapped into the Color ANC. See Figure 23.

Example.2) FS-Log curve with lower three coordinates and default tristimulus values, default reference white and default k_{exp}:

	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
ACT1	0	1	0	0	0	0	0	0	0	1
ACT2	1	0	0	0	0	0	1	0	0	1

Parameter values of α, β, δ, ε and lower three coordinates of (L_{B1}, L'_{B1}), (L_{B2}, L'_{B2}), (L_{B3}, L'_{B3}) shall be mapped into the Color ANC.

Example.3) FS-Log curve without upper and lower three coordinates and with user defined tristimulus values, default reference white and over exposure:

	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
ACT1	1	0	0	0	0	1	1	1	0	1
ACT2	1	0	0	0	0	1	0	0	0	1

User defined parameter values of tristimulus values (R_{user}, G_{user}, B_{user}) and α, β, δ, ε, k_{exp} shall be mapped into the Color ANC.

Example.4) Tristimulus values, reference white and opto-electric conversion defined in Recommendation ITU-R BT.709:

	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
ACT1	0	1	0	0	0	0	0	0	1	0
ACT2	0	1	0	0	0	0	0	0	1	0

Example.5) The gamma curve defined in Recommendation ITU-R BT.709 with user defined tristimulus values and default reference white:

	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
ACT1	1	0	0	0	0	1	1	1	1	0
ACT2	0	1	0	0	0	0	0	0	1	0

User defined tristimulus values of R_{user}, G_{user}, B_{user} shall be mapped into the Color ANC.

11.3 RFS, GFS, BFS, Reference White Primaries, α, β, δ, ε, kexp and LB1, L'B1, LB2, L'B2, LB3, L'B3, LC1, L'C1, LC2, L'C2, LC3 L'C3 Parameters

The CIE *x, y* chromaticity coordinates of R_{user}, G_{user}, B_{user} primaries, reference white primaries, parameter values of α, β, δ, ε, k_{exp} and upper and lower three coordinates of L_{B1}, L'_{B1}, L_{B2}, L'_{B2}, L_{B3}, L'_{B3} and L_{C1}, L'_{C1}, L_{C2}, L'_{C2}, L_{C3} L'_{C3} shall be denoted by the 32-bit Binary Floating-Point Arithmetic defined in IEEE 754-2008 as shown in Figure 5. The values of *x*, *y* chromaticity coordinates shall be defined within the range of -2.00000 to +2.00000 i.e.; $-2.00000 \leq x, y \leq +2.00000$.

The bit assignment of R_{user}, G_{user}, B_{user} and the reference white primaries shall be as shown in Table 29 and Table 30. The bit assignment of α, β, δ, ε, k_{exp} and L_{B1}, L'_{B1}, L_{B2}, L'_{B2}, L_{B3}, L'_{B3}, L_{C1}, L'_{C1}, L_{C2}, L'_{C2}, L_{C3}, L'_{C3} shall be as shown in Table 31, Table 32, Table 33 and Table 34, respectively.

Table 29 – Bit-assignment of R_{user}, G_{user}, B_{user} primaries

	Bit number	UDW2	UDW3	UDW4	UDW5
R_{user} primary *x*	b9 (MSB)	Not b8	Not b8	Not b8	Not b8
	b8	Even parity [1)]	Even parity [1)]	Even parity [1)]	Even parity [1)]
	b7	b31 (sign)	b23 (exponent)	b15 (fraction)	b7 (fraction)
	b6	b30 (exponent)	b22 (fraction)	b14 (fraction)	b6 (fraction)
	b5	b29 (exponent)	b21 (fraction)	b13 (fraction)	b5 (fraction)
	b4	b28 (exponent)	b20 (fraction)	b12 (fraction)	b4 (fraction)
	b3	b27 (exponent)	b19 (fraction)	b11 (fraction)	b3 (fraction)
	b2	b26 (exponent)	b18 (fraction)	b10 (fraction)	b2 (fraction)
	b1	b25 (exponent)	b17 (fraction)	b9 (fraction)	b1 (fraction)
	b0 (LSB)	b24 (exponent)	b16 (fraction)	b8 (fraction)	b0 (fraction)
	Bit number	UDW6	UDW7	UDW8	UDW9
R_{user} primary *y*	b9 (MSB)	Not b8	Not b8	Not b8	Not b8
	b8	Even parity [1)]	Even parity [1)]	Even parity [1)]	Even parity [1)]
	b7	b31 (sign)	b23 (exponent)	b15 (fraction)	b7 (fraction)
	b6	b30 (exponent)	b22 (fraction)	b14 (fraction)	b6 (fraction)
	b5	b29 (exponent)	b21 (fraction)	b13 (fraction)	b5 (fraction)
	b4	b28 (exponent)	b20 (fraction)	b12 (fraction)	b4 (fraction)
	b3	b27 (exponent)	b19 (fraction)	b11 (fraction)	b3 (fraction)
	b2	b26 (exponent)	b18 (fraction)	b10 (fraction)	b2 (fraction)
	b1	b25 (exponent)	b17 (fraction)	b9 (fraction)	b1 (fraction)
	b0 (LSB)	b24 (exponent)	b16 (fraction)	b8 (fraction)	b0 (fraction)
	Bit number	UDW10	UDW11	UDW12	UDW13
G_{user} primary *x*	b9 (MSB)	Not b8	Not b8	Not b8	Not b8
	b8	Even parity [1)]	Even parity [1)]	Even parity [1)]	Even parity [1)]
	b7	b31 (sign)	b23 (exponent)	b15 (fraction)	b7 (fraction)
	b6	b30 (exponent)	b22 (fraction)	b14 (fraction)	b6 (fraction)
	b5	b29 (exponent)	b21 (fraction)	b13 (fraction)	b5 (fraction)
	b4	b28 (exponent)	b20 (fraction)	b12 (fraction)	b4 (fraction)
	b3	b27 (exponent)	b19 (fraction)	b11 (fraction)	b3 (fraction)
	b2	b26 (exponent)	b18 (fraction)	b10 (fraction)	b2 (fraction)
	b1	b25 (exponent)	b17 (fraction)	b9 (fraction)	b1 (fraction)
	b0 (LSB)	b24 (exponent)	b16 (fraction)	b8 (fraction)	b0 (fraction)
	Bit number	UDW14	UDW15	UDW16	UDW17
G_{user} primary *y*	b9 (MSB)	Not b8	Not b8	Not b8	Not b8
	b8	Even parity [1)]	Even parity [1)]	Even parity [1)]	Even parity [1)]
	b7	b31 (sign)	b23 (exponent)	b15 (fraction)	b7 (fraction)
	b6	b30 (exponent)	b22 (fraction)	b14 (fraction)	b6 (fraction)
	b5	b29 (exponent)	b21 (fraction)	b13 (fraction)	b5 (fraction)
	b4	b28 (exponent)	b20 (fraction)	b12 (fraction)	b4 (fraction)
	b3	b27 (exponent)	b19 (fraction)	b11 (fraction)	b3 (fraction)
	b2	b26 (exponent)	b18 (fraction)	b10 (fraction)	b2 (fraction)
	b1	b25 (exponent)	b17 (fraction)	b9 (fraction)	b1 (fraction)
	b0 (LSB)	b24 (exponent)	b16 (fraction)	b8 (fraction)	b0 (fraction)
	Bit number	UDW18	UDW19	UDW20	UDW21
B_{user} primary *x*	b9 (MSB)	Not b8	Not b8	Not b8	Not b8
	b8	Even parity [1)]	Even parity [1)]	Even parity [1)]	Even parity [1)]
	b7	b31 (sign)	b23 (exponent)	b15 (fraction)	b7 (fraction)
	b6	b30 (exponent)	b22 (fraction)	b14 (fraction)	b6 (fraction)
	b5	b29 (exponent)	b21 (fraction)	b13 (fraction)	b5 (fraction)
	b4	b28 (exponent)	b20 (fraction)	b12 (fraction)	b4 (fraction)
	b3	b27 (exponent)	b19 (fraction)	b11 (fraction)	b3 (fraction)
	b2	b26 (exponent)	b18 (fraction)	b10 (fraction)	b2 (fraction)
	b1	b25 (exponent)	b17 (fraction)	b9 (fraction)	b1 (fraction)
	b0 (LSB)	b24 (exponent)	b16 (fraction)	b8 (fraction)	b0 (fraction)
	Bit number	UDW22	UDW23	UDW24	UDW25
B_{user} primary *y*	b9 (MSB)	Not b8	Not b8	Not b8	Not b8
	b8	Even parity [1)]	Even parity [1)]	Even parity [1)]	Even parity [1)]
	b7	b31 (sign)	b23 (exponent)	b15 (fraction)	b7 (fraction)
	b6	b30 (exponent)	b22 (fraction)	b14 (fraction)	b6 (fraction)
	b5	b29 (exponent)	b21 (fraction)	b13 (fraction)	b5 (fraction)
	b4	b28 (exponent)	b20 (fraction)	b12 (fraction)	b4 (fraction)
	b3	b27 (exponent)	b19 (fraction)	b11 (fraction)	b3 (fraction)
	b2	b26 (exponent)	b18 (fraction)	b10 (fraction)	b2 (fraction)
	b1	b25 (exponent)	b17 (fraction)	b9 (fraction)	b1 (fraction)
	b0 (LSB)	b24 (exponent)	b16 (fraction)	b8 (fraction)	b0 (fraction)

[1)] Even parity for b0 through b7

Table 30 – Bit-assignment of reference white primaries

	Bit number	UDW26	UDW27	UDW28	UDW29
reference white *x*	b9 (MSB)	Not b8	Not b8	Not b8	Not b8
	b8	Even parity [1)]	Even parity [1)]	Even parity [1)]	Even parity [1)]
	b7	b31 (sign)	b23 (exponent)	b15 (fraction)	b7 (fraction)
	b6	b30 (exponent)	b22 (fraction)	b14 (fraction)	b6 (fraction)
	b5	b29 (exponent)	b21 (fraction)	b13 (fraction)	b5 (fraction)
	b4	b28 (exponent)	b20 (fraction)	b12 (fraction)	b4 (fraction)
	b3	b27 (exponent)	b19 (fraction)	b11 (fraction)	b3 (fraction)
	b2	b26 (exponent)	b18 (fraction)	b10 (fraction)	b2 (fraction)
	b1	b25 (exponent)	b17 (fraction)	b9 (fraction)	b1 (fraction)
	b0 (LSB)	b24 (exponent)	b16 (fraction)	b8 (fraction)	b0 (fraction)
	Bit number	UDW30	UDW31	UDW32	UDW33
reference white *y*	b9 (MSB)	Not b8	Not b8	Not b8	Not b8
	b8	Even parity [1)]	Even parity [1)]	Even parity [1)]	Even parity [1)]
	b7	b31 (sign)	b23 (exponent)	b15 (fraction)	b7 (fraction)
	b6	b30 (exponent)	b22 (fraction)	b14 (fraction)	b6 (fraction)
	b5	b29 (exponent)	b21 (fraction)	b13 (fraction)	b5 (fraction)
	b4	b28 (exponent)	b20 (fraction)	b12 (fraction)	b4 (fraction)
	b3	b27 (exponent)	b19 (fraction)	b11 (fraction)	b3 (fraction)
	b2	b26 (exponent)	b18 (fraction)	b10 (fraction)	b2 (fraction)
	b1	b25 (exponent)	b17 (fraction)	b9 (fraction)	b1 (fraction)
	b0 (LSB)	b24 (exponent)	b16 (fraction)	b8 (fraction)	b0 (fraction)

[1)] Even parity for b0 through b7

Table 31 – Bit-assignment of α, β, δ, ε parameters

	Bit number	UDW34	UDW35	UDW36	UDW37
α	b9 (MSB)	Not b8	Not b8	Not b8	Not b8
	b8	Even parity [1)]	Even parity [1)]	Even parity [1)]	Even parity [1)]
	b7	b31 (sign)	b23 (exponent)	b15 (fraction)	b7 (fraction)
	b6	b30 (exponent)	b22 (fraction)	b14 (fraction)	b6 (fraction)
	b5	b29 (exponent)	b21 (fraction)	b13 (fraction)	b5 (fraction)
	b4	b28 (exponent)	b20 (fraction)	b12 (fraction)	b4 (fraction)
	b3	b27 (exponent)	b19 (fraction)	b11 (fraction)	b3 (fraction)
	b2	b26 (exponent)	b18 (fraction)	b10 (fraction)	b2 (fraction)
	b1	b25 (exponent)	b17 (fraction)	b9 (fraction)	b1 (fraction)
	b0 (LSB)	b24 (exponent)	b16 (fraction)	b8 (fraction)	b0 (fraction)
	Bit number	UDW38	UDW39	UDW40	UDW41
β	b9 (MSB)	Not b8	Not b8	Not b8	Not b8
	b8	Even parity [1)]	Even parity [1)]	Even parity [1)]	Even parity [1)]
	b7	b31 (sign)	b23 (exponent)	b15 (fraction)	b7 (fraction)
	b6	b30 (exponent)	b22 (fraction)	b14 (fraction)	b6 (fraction)
	b5	b29 (exponent)	b21 (fraction)	b13 (fraction)	b5 (fraction)
	b4	b28 (exponent)	b20 (fraction)	b12 (fraction)	b4 (fraction)
	b3	b27 (exponent)	b19 (fraction)	b11 (fraction)	b3 (fraction)
	b2	b26 (exponent)	b18 (fraction)	b10 (fraction)	b2 (fraction)
	b1	b25 (exponent)	b17 (fraction)	b9 (fraction)	b1 (fraction)
	b0 (LSB)	b24 (exponent)	b16 (fraction)	b8 (fraction)	b0 (fraction)
	Bit number	UDW42	UDW43	UDW44	UDW45
δ	b9 (MSB)	Not b8	Not b8	Not b8	Not b8
	b8	Even parity [1)]	Even parity [1)]	Even parity [1)]	Even parity [1)]
	b7	b31 (sign)	b23 (exponent)	b15 (fraction)	b7 (fraction)
	b6	b30 (exponent)	b22 (fraction)	b14 (fraction)	b6 (fraction)
	b5	b29 (exponent)	b21 (fraction)	b13 (fraction)	b5 (fraction)
	b4	b28 (exponent)	b20 (fraction)	b12 (fraction)	b4 (fraction)
	b3	b27 (exponent)	b19 (fraction)	b11 (fraction)	b3 (fraction)
	b2	b26 (exponent)	b18 (fraction)	b10 (fraction)	b2 (fraction)
	b1	b25 (exponent)	b17 (fraction)	b9 (fraction)	b1 (fraction)
	b0 (LSB)	b24 (exponent)	b16 (fraction)	b8 (fraction)	b0 (fraction)
	Bit number	UDW46	UDW47	UDW48	UDW49
ε	b9 (MSB)	Not b8	Not b8	Not b8	Not b8
	b8	Even parity [1)]	Even parity [1)]	Even parity [1)]	Even parity [1)]
	b7	b31 (sign)	b23 (exponent)	b15 (fraction)	b7 (fraction)
	b6	b30 (exponent)	b22 (fraction)	b14 (fraction)	b6 (fraction)
	b5	b29 (exponent)	b21 (fraction)	b13 (fraction)	b5 (fraction)
	b4	b28 (exponent)	b20 (fraction)	b12 (fraction)	b4 (fraction)
	b3	b27 (exponent)	b19 (fraction)	b11 (fraction)	b3 (fraction)
	b2	b26 (exponent)	b18 (fraction)	b10 (fraction)	b2 (fraction)
	b1	b25 (exponent)	b17 (fraction)	b9 (fraction)	b1 (fraction)
	b0 (LSB)	b24 (exponent)	b16 (fraction)	b8 (fraction)	b0 (fraction)

[1)] Even parity for b0 through b7

Table 32 – Bit-assignment of k_{exp}

	Bit number	UDW50	UDW51	UDW52	UDW53
k_{exp}	b9 (MSB)	Not b8	Not b8	Not b8	Not b8
	b8	Even parity [1)]	Even parity [1)]	Even parity [1)]	Even parity [1)]
	b7	b31 (sign)	b23 (exponent)	b15 (fraction)	b7 (fraction)
	b6	b30 (exponent)	b22 (fraction)	b14 (fraction)	b6 (fraction)
	b5	b29 (exponent)	b21 (fraction)	b13 (fraction)	b5 (fraction)
	b4	b28 (exponent)	b20 (fraction)	b12 (fraction)	b4 (fraction)
	b3	b27 (exponent)	b19 (fraction)	b11 (fraction)	b3 (fraction)
	b2	b26 (exponent)	b18 (fraction)	b10 (fraction)	b2 (fraction)
	b1	b25 (exponent)	b17 (fraction)	b9 (fraction)	b1 (fraction)
	b0 (LSB)	b24 (exponent)	b16 (fraction)	b8 (fraction)	b0 (fraction)

[1)] Even parity for b0 through b7

Table 33 – Bit-assignment of L_{B1}, L'_{B1}, L_{B2}, L'_{B2}, L_{B3}, L'_{B3}

	Bit number	UDW54	UDW55	UDW56	UDW57
L_{B1}	b9 (MSB)	Not b8	Not b8	Not b8	Not b8
	b8	Even parity [1)]	Even parity [1)]	Even parity [1)]	Even parity [1)]
	b7	b31 (sign)	b23 (exponent)	b15 (fraction)	b7 (fraction)
	b6	b30 (exponent)	b22 (fraction)	b14 (fraction)	b6 (fraction)
	b5	b29 (exponent)	b21 (fraction)	b13 (fraction)	b5 (fraction)
	b4	b28 (exponent)	b20 (fraction)	b12 (fraction)	b4 (fraction)
	b3	b27 (exponent)	b19 (fraction)	b11 (fraction)	b3 (fraction)
	b2	b26 (exponent)	b18 (fraction)	b10 (fraction)	b2 (fraction)
	b1	b25 (exponent)	b17 (fraction)	b9 (fraction)	b1 (fraction)
	b0 (LSB)	b24 (exponent)	b16 (fraction)	b8 (fraction)	b0 (fraction)
	Bit number	UDW58	UDW59	UDW60	UDW61
L'_{B1}	b9 (MSB)	Not b8	Not b8	Not b8	Not b8
	b8	Even parity [1)]	Even parity [1)]	Even parity [1)]	Even parity [1)]
	b7	b31 (sign)	b23 (exponent)	b15 (fraction)	b7 (fraction)
	b6	b30 (exponent)	b22 (fraction)	b14 (fraction)	b6 (fraction)
	b5	b29 (exponent)	b21 (fraction)	b13 (fraction)	b5 (fraction)
	b4	b28 (exponent)	b20 (fraction)	b12 (fraction)	b4 (fraction)
	b3	b27 (exponent)	b19 (fraction)	b11 (fraction)	b3 (fraction)
	b2	b26 (exponent)	b18 (fraction)	b10 (fraction)	b2 (fraction)
	b1	b25 (exponent)	b17 (fraction)	b9 (fraction)	b1 (fraction)
	b0 (LSB)	b24 (exponent)	b16 (fraction)	b8 (fraction)	b0 (fraction)
	Bit number	UDW62	UDW63	UDW64	UDW65
L_{B2}	b9 (MSB)	Not b8	Not b8	Not b8	Not b8
	b8	Even parity [1)]	Even parity [1)]	Even parity [1)]	Even parity [1)]
	b7	b31 (sign)	b23 (exponent)	b15 (fraction)	b7 (fraction)
	b6	b30 (exponent)	b22 (fraction)	b14 (fraction)	b6 (fraction)
	b5	b29 (exponent)	b21 (fraction)	b13 (fraction)	b5 (fraction)
	b4	b28 (exponent)	b20 (fraction)	b12 (fraction)	b4 (fraction)
	b3	b27 (exponent)	b19 (fraction)	b11 (fraction)	b3 (fraction)
	b2	b26 (exponent)	b18 (fraction)	b10 (fraction)	b2 (fraction)
	b1	b25 (exponent)	b17 (fraction)	b9 (fraction)	b1 (fraction)
	b0 (LSB)	b24 (exponent)	b16 (fraction)	b8 (fraction)	b0 (fraction)
	Bit number	UDW66	UDW67	UDW68	UDW69
L'_{B2}	b9 (MSB)	Not b8	Not b8	Not b8	Not b8
	b8	Even parity [1)]	Even parity [1)]	Even parity [1)]	Even parity [1)]
	b7	b31 (sign)	b23 (exponent)	b15 (fraction)	b7 (fraction)
	b6	b30 (exponent)	b22 (fraction)	b14 (fraction)	b6 (fraction)
	b5	b29 (exponent)	b21 (fraction)	b13 (fraction)	b5 (fraction)
	b4	b28 (exponent)	b20 (fraction)	b12 (fraction)	b4 (fraction)
	b3	b27 (exponent)	b19 (fraction)	b11 (fraction)	b3 (fraction)
	b2	b26 (exponent)	b18 (fraction)	b10 (fraction)	b2 (fraction)
	b1	b25 (exponent)	b17 (fraction)	b9 (fraction)	b1 (fraction)
	b0 (LSB)	b24 (exponent)	b16 (fraction)	b8 (fraction)	b0 (fraction)
	Bit number	UDW70	UDW71	UDW72	UDW73
L_{B3}	b9 (MSB)	Not b8	Not b8	Not b8	Not b8
	b8	Even parity [1)]	Even parity [1)]	Even parity [1)]	Even parity [1)]
	b7	b31 (sign)	b23 (exponent)	b15 (fraction)	b7 (fraction)
	b6	b30 (exponent)	b22 (fraction)	b14 (fraction)	b6 (fraction)
	b5	b29 (exponent)	b21 (fraction)	b13 (fraction)	b5 (fraction)
	b4	b28 (exponent)	b20 (fraction)	b12 (fraction)	b4 (fraction)
	b3	b27 (exponent)	b19 (fraction)	b11 (fraction)	b3 (fraction)
	b2	b26 (exponent)	b18 (fraction)	b10 (fraction)	b2 (fraction)
	b1	b25 (exponent)	b17 (fraction)	b9 (fraction)	b1 (fraction)
	b0 (LSB)	b24 (exponent)	b16 (fraction)	b8 (fraction)	b0 (fraction)
	Bit number	UDW74	UDW75	UDW76	UDW77
L'_{B3}	b9 (MSB)	Not b8	Not b8	Not b8	Not b8
	b8	Even parity [1)]	Even parity [1)]	Even parity [1)]	Even parity [1)]
	b7	b31 (sign)	b23 (exponent)	b15 (fraction)	b7 (fraction)
	b6	b30 (exponent)	b22 (fraction)	b14 (fraction)	b6 (fraction)
	b5	b29 (exponent)	b21 (fraction)	b13 (fraction)	b5 (fraction)
	b4	b28 (exponent)	b20 (fraction)	b12 (fraction)	b4 (fraction)
	b3	b27 (exponent)	b19 (fraction)	b11 (fraction)	b3 (fraction)
	b2	b26 (exponent)	b18 (fraction)	b10 (fraction)	b2 (fraction)
	b1	b25 (exponent)	b17 (fraction)	b9 (fraction)	b1 (fraction)
	b0 (LSB)	b24 (exponent)	b16 (fraction)	b8 (fraction)	b0 (fraction)

[1)] Even parity for b0 through b7

Table 34 – Bit-assignment of L_{C1}, L'_{C1}, L_{C2}, L'_{C2}, L_{C3}, L'_{C3}

	Bit number	UDW78	UDW79	UDW80	UDW81
L_{C1}	b9 (MSB)	Not b8	Not b8	Not b8	Not b8
	b8	Even parity [1)]	Even parity [1)]	Even parity [1)]	Even parity [1)]
	b7	b31 (sign)	b23 (exponent)	b15 (fraction)	b7 (fraction)
	b6	b30 (exponent)	b22 (fraction)	b14 (fraction)	b6 (fraction)
	b5	b29 (exponent)	b21 (fraction)	b13 (fraction)	b5 (fraction)
	b4	b28 (exponent)	b20 (fraction)	b12 (fraction)	b4 (fraction)
	b3	b27 (exponent)	b19 (fraction)	b11 (fraction)	b3 (fraction)
	b2	b26 (exponent)	b18 (fraction)	b10 (fraction)	b2 (fraction)
	b1	b25 (exponent)	b17 (fraction)	b9 (fraction)	b1 (fraction)
	b0 (LSB)	b24 (exponent)	b16 (fraction)	b8 (fraction)	b0 (fraction)
	Bit number	UDW82	UDW83	UDW84	UDW85
L'_{C1}	b9 (MSB)	Not b8	Not b8	Not b8	Not b8
	b8	Even parity [1)]	Even parity [1)]	Even parity [1)]	Even parity [1)]
	b7	b31 (sign)	b23 (exponent)	b15 (fraction)	b7 (fraction)
	b6	b30 (exponent)	b22 (fraction)	b14 (fraction)	b6 (fraction)
	b5	b29 (exponent)	b21 (fraction)	b13 (fraction)	b5 (fraction)
	b4	b28 (exponent)	b20 (fraction)	b12 (fraction)	b4 (fraction)
	b3	b27 (exponent)	b19 (fraction)	b11 (fraction)	b3 (fraction)
	b2	b26 (exponent)	b18 (fraction)	b10 (fraction)	b2 (fraction)
	b1	b25 (exponent)	b17 (fraction)	b9 (fraction)	b1 (fraction)
	b0 (LSB)	b24 (exponent)	b16 (fraction)	b8 (fraction)	b0 (fraction)
	Bit number	UDW86	UDW87	UDW88	UDW89
L_{C2}	b9 (MSB)	Not b8	Not b8	Not b8	Not b8
	b8	Even parity [1)]	Even parity [1)]	Even parity [1)]	Even parity [1)]
	b7	b31 (sign)	b23 (exponent)	b15 (fraction)	b7 (fraction)
	b6	b30 (exponent)	b22 (fraction)	b14 (fraction)	b6 (fraction)
	b5	b29 (exponent)	b21 (fraction)	b13 (fraction)	b5 (fraction)
	b4	b28 (exponent)	b20 (fraction)	b12 (fraction)	b4 (fraction)
	b3	b27 (exponent)	b19 (fraction)	b11 (fraction)	b3 (fraction)
	b2	b26 (exponent)	b18 (fraction)	b10 (fraction)	b2 (fraction)
	b1	b25 (exponent)	b17 (fraction)	b9 (fraction)	b1 (fraction)
	b0 (LSB)	b24 (exponent)	b16 (fraction)	b8 (fraction)	b0 (fraction)
	Bit number	UDW90	UDW91	UDW92	UDW93
L'_{C2}	b9 (MSB)	Not b8	Not b8	Not b8	Not b8
	b8	Even parity [1)]	Even parity [1)]	Even parity [1)]	Even parity [1)]
	b7	b31 (sign)	b23 (exponent)	b15 (fraction)	b7 (fraction)
	b6	b30 (exponent)	b22 (fraction)	b14 (fraction)	b6 (fraction)
	b5	b29 (exponent)	b21 (fraction)	b13 (fraction)	b5 (fraction)
	b4	b28 (exponent)	b20 (fraction)	b12 (fraction)	b4 (fraction)
	b3	b27 (exponent)	b19 (fraction)	b11 (fraction)	b3 (fraction)
	b2	b26 (exponent)	b18 (fraction)	b10 (fraction)	b2 (fraction)
	b1	b25 (exponent)	b17 (fraction)	b9 (fraction)	b1 (fraction)
	b0 (LSB)	b24 (exponent)	b16 (fraction)	b8 (fraction)	b0 (fraction)
	Bit number	UDW94	UDW95	UDW96	UDW97
L_{C3}	b9 (MSB)	Not b8	Not b8	Not b8	Not b8
	b8	Even parity [1)]	Even parity [1)]	Even parity [1)]	Even parity [1)]
	b7	b31 (sign)	b23 (exponent)	b15 (fraction)	b7 (fraction)
	b6	b30 (exponent)	b22 (fraction)	b14 (fraction)	b6 (fraction)
	b5	b29 (exponent)	b21 (fraction)	b13 (fraction)	b5 (fraction)
	b4	b28 (exponent)	b20 (fraction)	b12 (fraction)	b4 (fraction)
	b3	b27 (exponent)	b19 (fraction)	b11 (fraction)	b3 (fraction)
	b2	b26 (exponent)	b18 (fraction)	b10 (fraction)	b2 (fraction)
	b1	b25 (exponent)	b17 (fraction)	b9 (fraction)	b1 (fraction)
	b0 (LSB)	b24 (exponent)	b16 (fraction)	b8 (fraction)	b0 (fraction)
	Bit number	UDW98	UDW99	UDW100	UDW101
L'_{C3}	b9 (MSB)	Not b8	Not b8	Not b8	Not b8
	b8	Even parity [1)]	Even parity [1)]	Even parity [1)]	Even parity [1)]
	b7	b31 (sign)	b23 (exponent)	b15 (fraction)	b7 (fraction)
	b6	b30 (exponent)	b22 (fraction)	b14 (fraction)	b6 (fraction)
	b5	b29 (exponent)	b21 (fraction)	b13 (fraction)	b5 (fraction)
	b4	b28 (exponent)	b20 (fraction)	b12 (fraction)	b4 (fraction)
	b3	b27 (exponent)	b19 (fraction)	b11 (fraction)	b3 (fraction)
	b2	b26 (exponent)	b18 (fraction)	b10 (fraction)	b2 (fraction)
	b1	b25 (exponent)	b17 (fraction)	b9 (fraction)	b1 (fraction)
	b0 (LSB)	b24 (exponent)	b16 (fraction)	b8 (fraction)	b0 (fraction)

[1)] Even parity for b0 through b7