RP 168-2009
Revision of RP 168-2002

SMPTE RECOMMENDED PRACTICE

Definition of Vertical Interval Switching Point for Synchronous Video Switching

Table of Contents

Page

Approved July 17, 2009

Foreword

SMPTE (the Society of Motion Picture and Television Engineers) is an internationally-recognized standards developing organization. Headquartered and incorporated in the United States of America, SMPTE has members in over 80 countries on six continents. SMPTE's Engineering Documents, including Standards, Recommended Practices, and Engineering Guidelines, are prepared by SMPTE's Technology Committees. Participation in these Committees is open to all with a bona fide interest in their work. SMPTE cooperates closely with other standards-developing organizations, including ISO, IEC and ITU.

SMPTE Engineering Documents are drafted in accordance with the rules given in Part XIII of its Administrative Practices.

SMPTE Recommended Practice RP 168 was prepared by Technology Committee 22TV.

Intellectual Property

At the time of publication no notice had been received by SMPTE claiming patent rights essential to the implementation of this Recommended Practice. However, attention is drawn to the possibility that some of the elements of this document may be the subject of patent rights. SMPTE shall not be held responsible for identifying any or all such patent rights.

Introduction

This section is entirely informative and does not form an integral part of this Engineering Document.

This practice defines a switching point and area such that the effects of any signal discontinuity in the chain are minimized, regardless of whether the interface is carrying an uncompressed television signal or a data signal. The line designated for the switching point is chosen to be after vertical sync at the interface (to minimize the possibility of disturbances to vertical sync), but early in the vertical blanking interval. This ensures that signals transmitted during the vertical blanking interval (time code, audio data, etc.) remain with the video frame with which they are associated. It is recommended that vital ancillary data or payload data be excluded from the line following the switch line. Individual data applications may provide an appropriate provision for protection during switching. This practice applies to equipment that uses an external reference signal to time switching as well as equipment which does not.

1 Scope

This practice defines the line number and line timing for the switching point of serial digital and analog interfaces carrying television and data payloads to minimize any disturbance in the active payload area.

The switching point location is defined for uncompressed television interfaces operating with composite or component signals, where the payload signals may be in analog or digital format.

2 Conformance Notation

Normative text is text that describes elements of the design that are indispensable or contains the conformance language keywords: "shall", "should", or "may". Informative text is text that is potentially helpful to the user, but not indispensable, and can be removed, changed, or added editorially without affecting interoperability. Informative text does not contain any conformance keywords.

All text in this document is, by default, normative, except: the Introduction, any section explicitly labeled as "Informative" or individual paragraphs that start with "Note:"

The keywords "shall" and "shall not" indicate requirements strictly to be followed in order to conform to the document and from which no deviation is permitted.

The keywords, "should" and "should not" indicate that, among several possibilities, one is recommended as particularly suitable, without mentioning or excluding others; or that a certain course of action is preferred but not necessarily required; or that (in the negative form) a certain possibility or course of action is deprecated but not prohibited.

The keywords "may" and "need not" indicate courses of action permissible within the limits of the document.

The keyword "reserved" indicates a provision that is not defined at this time, shall not be used, and may be defined in the future. The keyword "forbidden" indicates "reserved" and in addition indicates that the provision will never be defined in the future.

A conformant implementation according to this document is one that includes all mandatory provisions ("shall") and, if implemented, all recommended provisions ("should") as described. A conformant implementation need not implement optional provisions ("may") and need not implement them as described.

Unless otherwise specified, the order of precedence of the types of normative information in this document shall be as follows: Normative prose shall be the authoritative definition; Tables shall be next; followed by formal languages; then figures; and then any other language forms.

3 Definition of Terms

These definitions apply to the terms as used in this practice:

3.1 horizontal reference point: The 50% amplitude point of the leading edge of horizontal sync.

3.2 interface raster: The payload area of the interface normally occupied by uncompressed video.

3.3 progressive segmented frame: The video data structure, which is defined in Recommendation ITU-R BT.709-5, has a progressive image capture structure and is transmitted via an interface that has an interlace raster structure.

3.4 start of active video: The first sample following SAV.

3.5 switching area: The position and tolerance within the switching line where the switch is permitted to occur.

3.6 switching line: The line number on which a change from one source to another is performed.

4 Normative References

The following standards contain provisions which, through reference in this text, constitute provisions of this recommended practice. At the time of publication, the editions indicated were valid. All standards are subject to revision, and parties to agreements based on this recommended practice are encouraged to investigate the possibility of applying the most recent edition of the standards indicated below.

SMPTE 170M-2004, Television — Composite Analog Video Signal — NTSC for Studio Applications

SMPTE 259M-2008, Television — SDTV Digital Signal/Data — Serial Digital Interface

SMPTE 274M-2008, Television – 1920 × 1080 Image Sample Structure, Digital Representation and Digital Timing Reference Sequences for Multiple Picture Rates

SMPTE 292-2008, 1.5 Gb/s Signal/Data Serial Interface

SMPTE 293M-2003, Television – 720 × 483 Active Line at 59.94-Hz Progressive Scan Production — Digital Representation

SMPTE 294M-2001, Television — 720 × 483 Active Line at 59.94-Hz Progressive Scan Production — Bit-Serial Interfaces

SMPTE 296M-2001, Television – 1280 × 720 Progressive Image Sample Structure — Analog and Digital Representation and Analog Interface (R2006)

SMPTE 344M-2000, Television — 540 Mb/s Serial Digital Interface (Archived 2006)

SMPTE 347M-2001, Television – 540 Mb/s Serial Digital Interface – Source Image Format Mapping (Archived 2006)

SMPTE 349M-2001, Television — Transport of Alternate Source Image Formats through SMPTE 292M (Archived 2006)

SMPTE 424M-2006, Television — 3 Gb/s Signal/Data Serial Interface

Recommendation ITU-R BT.709-5 (04/02), Parameter Values for the HDTV Standards for Production and International Programme Exchange

Recommendation ITU-R BT.799-4 (12/07), Interface for Digital Component Video Signals in 525-Line and 625-Line Television Systems Operating at the 4:4:4 Level of Recommendation ITU-R BT.601

Recommendation ITU-R BT.1358-1 (09/07), Studio Parameters of 625- and 525-Line Progressive Television Systems

Recommendation ITU-R BT.1362 (02/98), Interfaces for Digital Component Video Signals in 525- and 625-Line Progressive Scan Television Systems

Recommendation ITU-R BT.1700 (02/05), Characteristics of Composite Video Signals for Conventional Analogue Television Systems

5 Switching Line and Switching Area — Analog Systems

The switching line and switching area are shown in Table 1 and Figure 1 for 525/59.94/I systems, and Figure 2 for 625/50/I systems.

Note: The precise value of 59.94 is 60/1.001; this also applies to values such as 29.97, 23.98, and 74.18.

Table 1 – Switching line and switching area – Analog systems

Standard	Format	Switching line		Switching area in µs after horizontal reference point
		Field 1,3	Field 2,4	
SMPTE 170M-2004	525/59.94/I	10	273	30 ± 5
Rec. ITU-R BT.1700 (2005)	625/50 /I	6	319	30 ± 5

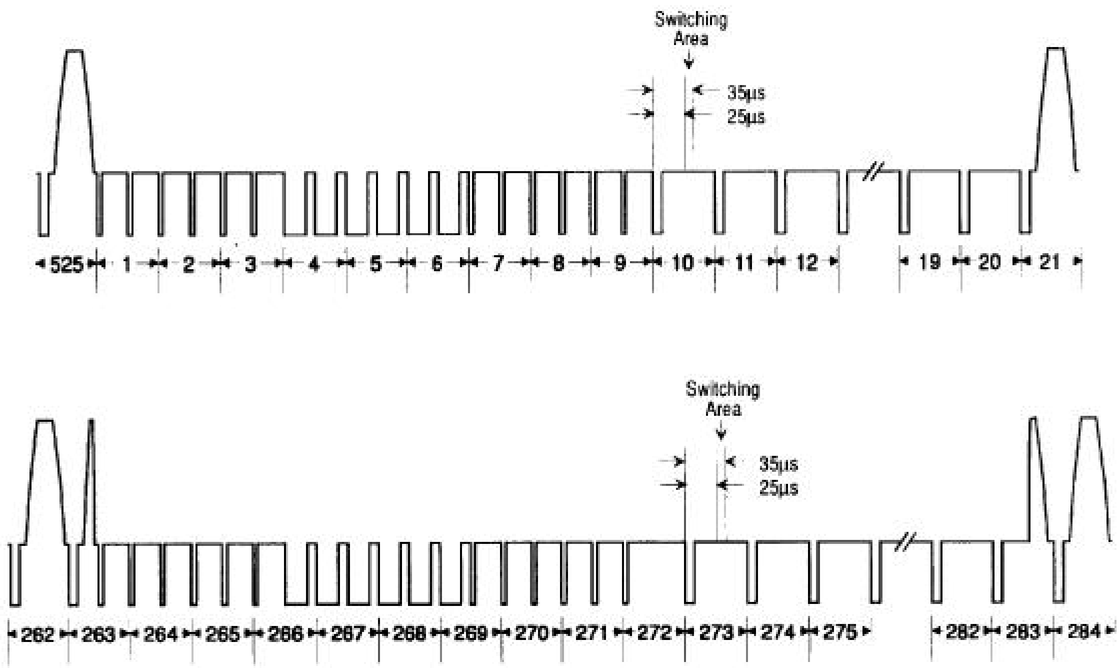


Figure 1 – 525-line system switching line and switching area

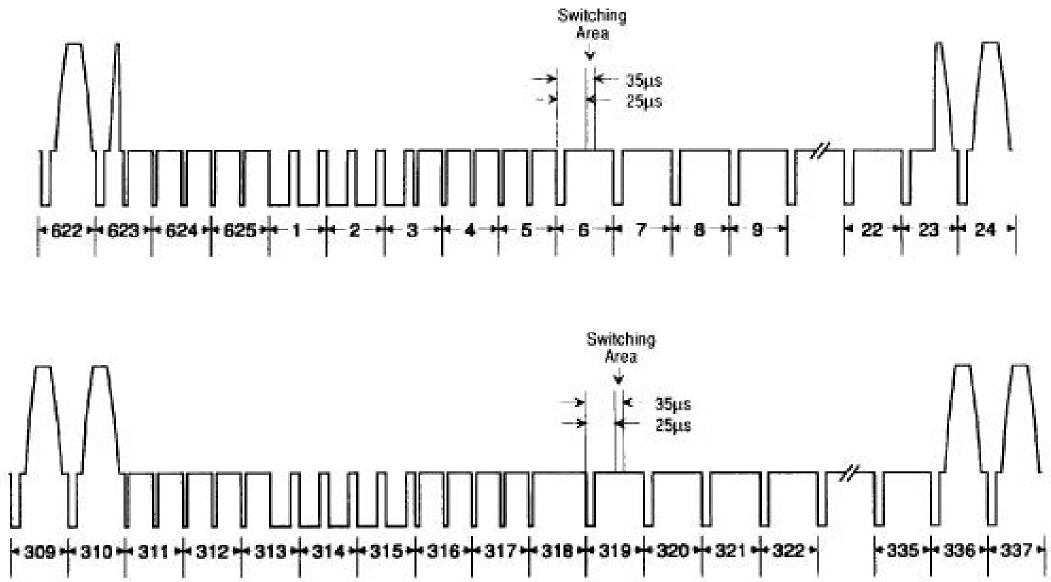


Figure 2 – 625-line system switching line and switching area

6 Switching Line and Switching Area — Digital Systems

The switching line and switching area for each digital system are shown in Table 2. For each raster structure listed in the table, both the switching area and the switching lines are defined by the Progressive or Interlaced serial interface structure used to convey the signal. The switching area is defined in word-clock cycles from the start of active video. Progressive digital video systems have one switching line and switching area per frame. Interlaced (including progressive segmented frame) digital video systems have two switching lines and switching areas per frame, one for each field. Table 2 lists these two switching lines as “Field 1 (Recommended)” and “Field 2”.

Existing devices may have been designed to switch on either field. New digital interlaced video devices should switch using the recommended Field 1 line.

Under current conditions, for a system with both interlaced video at a specific frame rate and progressive video at double that frame rate, devices handling the progressive video should be referenced to a signal derived from an interlaced format at the interlaced frame rate. Having established this referencing relationship, progressive video devices should switch using the recommended line during Field 1 of the reference signal.

Informative Note: In current practice, both video and audio signals are switched with reference to Field 1 of an interlaced reference to allow ancillary signal sequences spanning two fields to be switched error-free.

Notes:

1 In Table 2, frame rates scaled by 1/1.001 are also applied in the case of 60/P, 60/I, 30/P, 24/P, 30/PsF, and 24/PsF. Serial interface data rate 1.485 Gb/s is also scaled by 1/1.001 in these frame rates.

2 In a multiple signal environment, such as 1125/59.94/I and 525/59.94/I mixed operation, the switching line and switching area in table 2 for both signals may not be realized simultaneously (see Annex A).

3 (Informative) In Table 2, 1125/59.94/P and 1125/50/P video at a 2.97Gb/s serial interface data rate has two possible formats, Level A and Level B, as described in SMPTE 425M-2006. Throughout this document these two formats will be referred to as S425M-A and S425M-B, respectively.

Table 2 – Switching line and switching area – Digital systems

Total line No.	Raster structure	Serial interface data rate, Rs	Serial interface structure	Switchingline		Switching area, nxTclk Tclk=10/Rs	Normative reference(s)	Informative notes		
				Field 1 (Recommended)	Field 2			Serial interface	Signal	Mapping structure
1125	1920×1080 60/P, 50P	2.97Gb/s	P	7	–	1250-2140	424M, 274M	424M	274M	425-A #1
			I	7	569				274M×2	425-B #1
		1.485Gb/s×2				625-1070	292, 274M	292		372
	60/I, 50/I	1.485Gb/s							274M	274M
		1.485Gb/s×2							274M×2	372
	30/P, 25/P, 24/P	1.485Gb/s	P	7	–				274M	274M
		1.485Gb/s×2							274M×2	372
	30/PsF, 25/PsF, 24/PsF	1.485Gb/s	I	7	569				274M	274M
		1.485Gb/s×2							274M×2	372
750	1280×720 60/P, 50/P, 30/P 25/P, 24/P	2.97Gb/s	P	7	–	910-1560	424M, 296M	424M	296M	425-A #2
									296M×2	425-B(*)
		1.485Gb/s				455-780	292, 296M	292	296M	296M
625	720×576/50/P	2.97Gb/s	I	6	319	6214-9184	424M, BT1358	424M	BT1358×2	425-B(*) +349M
		1.485Gb/s				3107-4592	292, BT1358	292	BT1358	349M
		540Mb/s	P	6	–	1130-1670	344M, BT1358	344M		347M
		270Mb/s×2	I	6	319	565-835	BT1362	BT1362	BT1358×2	BT1362
	960×576/50/I	2.97Gb/s	I	6	319	6214-9184	424M, 349M	424M	BT601×2	425-B(*) +349M
		1.485Gb/s				3107-4592	292, 349M	292	BT601	349M
		360Mb/s				753-1113	259M	259M		BT656
	720×576/50/I	2.97Gb/s				6214-9184	424M, 349M	424M	BT601×2	425-B(*) +349M
		1.485Gb/s				3107-4592	292, 349M	292	BT601	349M
		540Mb/s				1130-1670	344M, BT799	344M	BT799	347M
		270Mb/s×2				565-835	259M	259M	BT601×2	BT799
		270Mb/s							BT601	BT656
		177Mb/s				267-455			259M	IEC 61179
525	720×483/59.94/P	2.97Gb/s	I	10	273	6214-9184	424M, 293M	424M	293M×2	425-B(*) +349M
		1.485Gb/s				3107-4592	292, 293M	292	293M	349M
		540Mb/s	P	10	–	1130-1670	344M, 293M	344M		347M
		270Mb/s×2	I	10	273	565-835	294M	294M		294M
		360Mb/s				847-1252				
	960×483/59.94/I	2.97Gb/s	I	10	273	6214-9184	424M, 349M	424M	267M×2	425-B(*) +349M
		1.485Gb/s				3107-4592	292, 349M	292	267M	349M
		360Mb/s				753-1113	259M	259M		267M
	720×483/59.94/I	2.97Gb/s				6214-9184	424M, 349M	424M	125M×2	425-B(*) +349M
		1.485Gb/s				3107-4592	292, 349M	292	125M	349M
		540Mb/s				1130-1670	344M, 347M	344M	RP174	347M
		270Mb/s×2				565-835	259M	259M	RP175	RP175
		270Mb/s							125M	125M
		143Mb/s				232-376			244M	244M
HD-SDTI	1920×1080 30/P, 25/P, 24/P	2.97Gb/s	P	7	–	1250-2140	424M, 274M	424M	274M×2	425-B(*) +348M
		1.485Gb/s				625-1070	292, 174M	292	274M	274M+348M
	1920×1080 60/I, 50/I, 30/PsF 25/PsF, 24/PsF	2.97Gb/s	I	7	569	1250-2140	424M, 274M	424M	274M×2	425-B(*) +348M
		1.485Gb/s				625-1070	292, 274M	292	274M	274M+348M
	1280×720 60/P, 50/P, 30/P, 25/P, 24/P	2.97Gb/s	P	7	–	910-1560	424M, 296M	424M	296M×2	425-B(*) +348M
		1.485Gb/s				455-780	292, 296M	292	296M	296M+348M
SDTI	720×576/50/I	270Mb/s	I	6	319	565-835	259M	259M	BT656	BT656+305M
	720×483/59.94/I			10	273				125M	125M+305M

(*) dual-link in these cases is two (×2) SMPTE 292 HD-SDI Mappings of a payload defined by the associated Signal standard, and the appropriate Payload Identifier described in Section 5 of SMPTE 425.

Note: Formats identified as BTxxx are Recommendation ITU-R BT.xxx.

Annex A
Signal Alignment and Switching Point Relationship for 1125-, 750-, 525- and 625-Line Systems

A.1 Signal Alignment for 1125-, 750-, 525- and 625-Line Systems (Normative)

The first line of each of the vertical reference sync timing signals that correspond to systems with different numbers of scan lines but which have the same frame rate shall all be coincident with each other. For example, in 59.94-Hz frame rate systems, the horizontal reference points of line 1 of 1125-line, line 1 of 750-line, and line 4 of 525-line signals shall be coincident (see Figure A.1). In 50-Hz frame rate systems, the horizontal reference points of line 1 of 1125-line, line 1 of 750-line, and line 1 of 625-line signals shall be coincident (see Figure A.2).

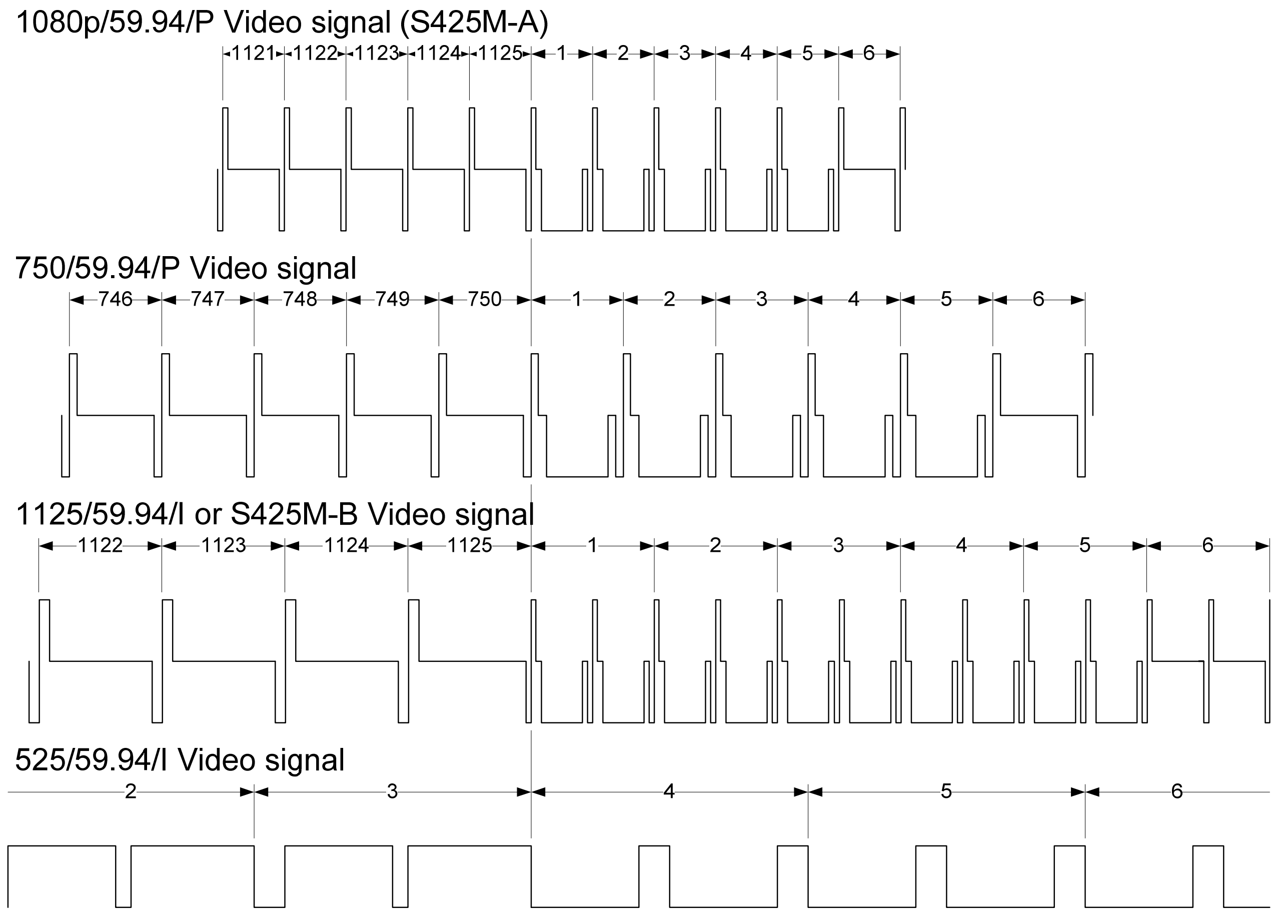


Figure A.1 – Signal alignment in 59.94-Hz field rate systems

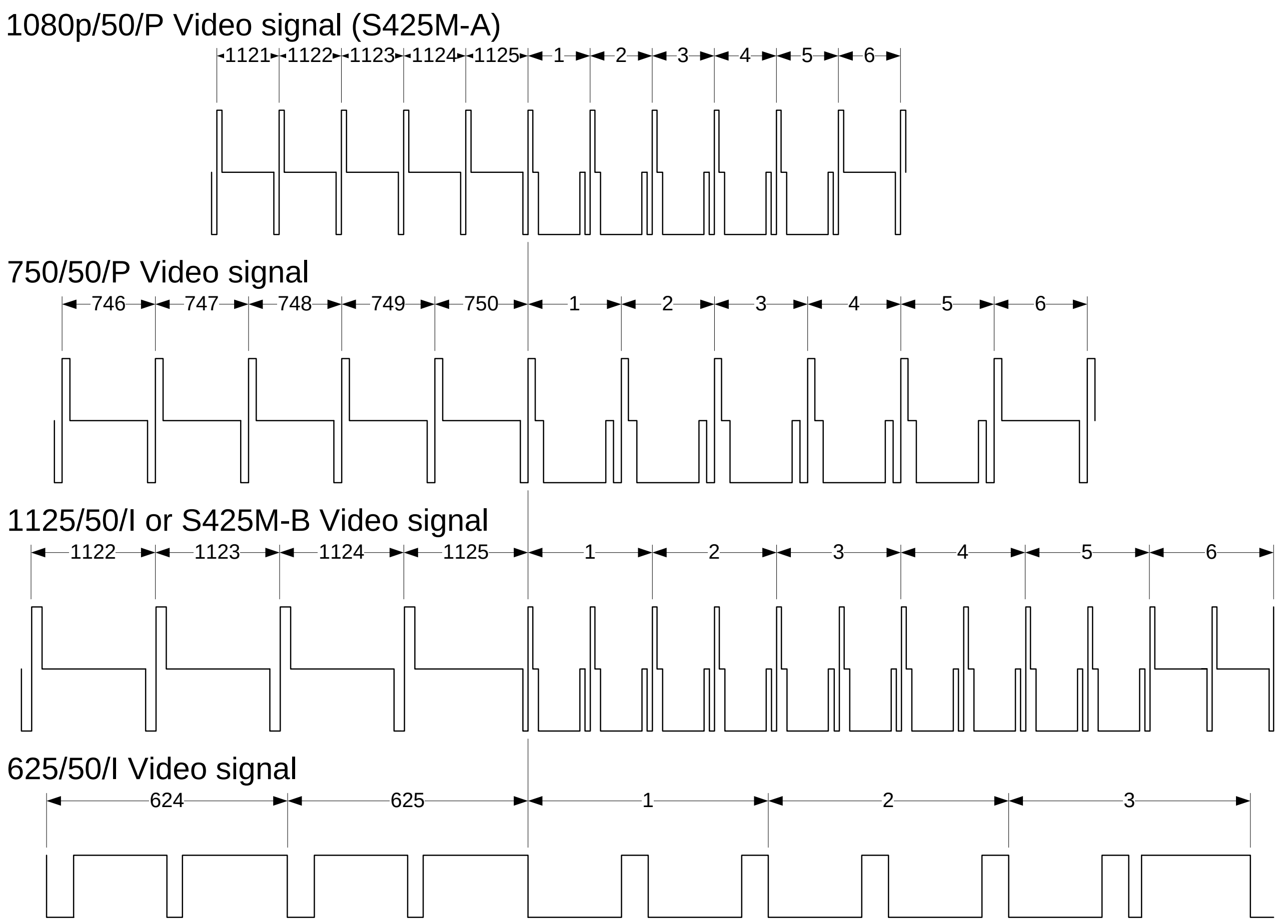


Figure A.2 – Signal alignment in 50-Hz field rate systems

A.2 Switching Point Relationship between 1125-, 750-, 525- and 625-line Television Signals (Informative)

In systems designs, an analog SDTV reference signal can be used as the reference for HDTV devices, such as routers. Tables A.1 and A.2 provide guidance on the timing relationship between the SDTV reference and the HDTV signals in order that the switching area defined in this practice may be achieved. For example, when using these reference signals, the switching positions of 1125/59.94/I, 750/59.94/P, and 525/59.94/I and those of 1125/50/I, 750/50/P, and 625/50/I can be seen in Tables A.1 and A.2, respectively.

A.2.1 59.94-Hz systems

Table A.1 – Switching point relationship in 59.94Hz frame and 59.94 field rate systems

1125/59.94/I	When using 525/59.94/I
Line 7, clock intervals 625 – 1070 (74.18 MHz)	Line 6.9733 – 7.0677 (27 MHz)
Line 569,clock intervals 625 – 1070 (74.18 MHz)	Line 269.2400 - 269.3344 (27 MHz)
1125/59.94/P	
Line 7, clock intervals 625 – 1070 (148.5 MHz)	Line 5.4866 – 5.5338 (27 MHz)
(next frame)	Line 267.9866 – 268.0338 (27 MHz)
750/59.94/P	
Line 7clock intervals 455 – 780 (74.18 MHz)	Line 6.2517 – 6.3206 (27 MHz)
(next frame)	Line 268.7517 – 268.8206 (27 MHz)
525/59.94/I	
Line 10, clock intervals 565 – 835 (27 MHz)	Line 10.4714 – 10.6288 (27 MHz)
Line 273, clock intervals 565 – 835 (27 MHz)	Line 273.4714 – 273.6288 (27 MHz)

Calculation:

A.2.1.1 Timing relationship between 1125/59.94/I and 525/59.94/I

The timing relationship of any line m and sample n of 1125/59.94/I and line M of 525/59.94/I in Figure A.1. is calculated as follows:

$$[(m-1) \times 2200 + (192+n)] \;/\; (1125 \times 29.97 \times 2200) = [(M-4) \times 1716] \;/\; (525 \times 29.97 \times 1716)$$

Therefore,

$$M = 4 + [(m-1) \times 2200 + (192 + n)] \times 7 / 33000$$

Each switching point of 1125/59.94/I is located at the following positions in 525/59.94/I:

a) m = 7, n = 625, M = 6.9733 b) m = 7, n = 1070, M = 7.0677

c) m = 569, n = 625, M = 269.2400 d) m = 569, n = 1070, M = 269.3344

A.2.1.2 Timing relationship between 750/59.94/P and 525/59.94/I

The timing relationship of line m and sample n of 750/59.94/P and line M of 525/59.94/I in Figure A.1 is calculated as follows:

$$[(m-1) \times 1650 + (260 + n)] \;/\; (750 \times 59.94 \times 1650) = [(M-4) \times 1716 \times 2] \;/\; (525 \times 59.94 \times 1716)$$

Therefore,

$$M = 4 + [(m-1) \times 1650 + (260 + n)] \times 7 / 33000$$

Each switching point of 750/59.94/P is located at the following positions in 525/59.94/I.

a) m = 7, n = 455, M = 6.2517 b) m = 7, n = 780, M = 6.3206

c) m = 757, n = 455, M = 268.7517 d) m = 757, n = 780, M = 268.8206

A.2.1.3 525/59.94/I

The analog horizontal reference point in the 525/59.94/I system is located 244 clock intervals before digital sample 0. The position of the clock intervals 565 and 835 counts from the analog horizontal reference point are therefore calculated as follows:

Clock interval 565: (244 + 565) / 1716 = 0.4714
Clock interval 835: (244 + 835) / 1716 = 0.6288

Clock intervals 565 to 835 of lines 10 and 273 can, therefore, be respectively shown as line 10.4714 to 10.6288 and 273.4714 to 273.6288.

A.2.1.4 Timing relationship between 1125/59.94/P and 525/59.94/I

The timing relationship of any line m and sample n of 1125/59.94/P and line M of 525/59.94/I in Figure A.1. is calculated as follows:

$$[(m-1) \times 2200 + (192+n)] / (1125 \times 59.94 \times 2200) = [(M-4) \times 1716 \times 2] / (525 \times 59.94 \times 1716)$$

Therefore,

$$M = 4 + [(m-1) \times 2200 + (192 + n)] \times 7 / 66000$$

Each switching point of 1125/59.94/P is located at the following positions in 525/59.94/I:

a) m = 7, n = 625, M = 5.4866

b) m = 7, n = 1070, M = 5.5338

c) m = 1132, n = 625, M = 267.9866

d) m = 1132, n = 1070, M = 268.0338

A.2.2 50Hz systems

Table A.2 – Switching point relationship in 50Hz frame/field rate systems

1125/50/I	When using 625/50/I
Line 7, clock intervals 625 – 1070 (74.25 MHz)	Line 4.5053 – 4.5990 (27 MHz)
Line 569, clock intervals 625 – 1070 (74.25 MHz)	Line 316.7275 – 316.8211 (27 MHz)
1125/50/P	
Line 7, clock intervals 625 – 1070 (148.5 MHz)	Line 2.7526 – 2.7994 (27 MHz)
(next frame)	Line 315.2526 – 315.2994 (27 MHz)
750/50/P	
Line 7, clock intervals 455 – 780 (74.25 MHz)	Line 3.6504 – 3.7189 (27 MHz)
(next frame)	Line 316.1505 – 316.2189 (27 MHz)
625/50/I	
Line 6, clock intervals 565 – 835 (2 MHz)	Line 6.4797 – 6.6360 (27 MHz)
Line 319, clock intervals 565 – 835 (27 MHz)	Line 319.4797 – 319.6360 (27 MHz)

Calculation:

A.2.2.1 Timing relationship between 1125/50/I and 625/50/I

The timing relationship of any line m and clock interval n of 1125/50/I and line M of 625/50/I in Figure A.2 is calculated as follows:

$$[(m-1) \times 2640 + (192+n)] \;/\; (1125 \times 25 \times 2640) = [(M-1) \times 1728] \;/\; (625 \times 25 \times 1728)$$

Therefore,

$$M = 1 + [(m-1) \times 2640 + (192 + n)] \;/\; 4752$$

Each switching point of 1125/50/I is located at the following position in 625/50/I:

a) m = 7, n = 625, M = 4.5053 b) m = 7, n = 1070, M = 4.5990

c) m = 569, n = 625, M = 316.7275 d) m = 569, n = 1070, M = 316.8211

A.2.2.2 Timing relationship between 750/50/P and 625/50/I

The timing relationship of line m and clock interval n of 750/50/P and line M of 625/50/I in Figure A.2 is calculated as follows:

$$[(m-1) \times 1980 + (260 + n)] \;/\; (750 \times 50 \times 1980) = [(M-1) \times 1728 \times 2] \;/\; (625 \times 50 \times 1728)$$

Therefore,

$$M = 1 + [(m-1) \times 1980 + (260 + n)] \;/\; 4752$$

Each switching point of 750/50/P is located at the following position in 625/50/I:

a) m = 7, n = 455, M =3.6504 b) m = 7, n = 780, M = 3.7189

c) m = 757, n = 455, M = 316.1505 d) m = 757, n = 780, M = 316.2189

A.2.2.3 625/50/I

The analog horizontal reference point in the 625/50/I system is located 264 clock intervals before digital sample 0. The digital clock intervals 565 and 835 from the analog horizontal reference point are therefore calculated as follows:

Clock interval 565: (264 + 565) / 1728 = 0.4797
Clock interval 835: (264 + 835) / 1728 = 0.6360

Clock intervals 565 to 835 of lines 6 and 319 can, therefore, be respectively shown as line 6.4797 to 6.6360 and 319.4797 to 319.6360.

A.2.2.4 Timing relationship between 1125/50/P and 625/50/I

The timing relationship of any line m and clock interval n of 1125/50/P and line M of 625/50/I in Figure A.2 is calculated as follows:

$$[(m-1) \times 2640 + (192+n)] \;/\; (1125 \times 50 \times 2640) = [(M-1) \times 1728 \times 2] \;/\; (625 \times 50 \times 1728)$$

Therefore,

$$M = 1 + [(m-1) \times 2640 + (192 + n)] / 9504$$

Each switching point of 1125/50/P is located at the following position in 625/50/I:

a) m = 7, n = 625, M = 2.7526

b) m = 7, n = 1070, M = 2.7994

c) m = 1132, n = 625, M = 315.2526

d) m = 569, n = 1070, M = 315.2994

Annex B (Informative)
External Reference Signals of 1125-Line Systems

B.1 Scope

Recommendation ITU-R BT.709-5 defines various frame rates of 1125 television systems. In these systems, 1125-line tri-level analog sync, 525/59.94/I, or 625/50/I analog signals can be used as the reference signal. This annex defines the V and H phase relationships between 1125 tri-level analog sync, 525/59.94/I, and 625/50/I analog sync signals.

B.2 1125 tri-level analog sync, 525/59.94/I and 625/50/I as external reference signals

Both tri-level analog sync, 525/59.94/I or 625/50/I analog sync can be used as external reference signals. Tri-level analog sync is used because it covers all frame rates. On the other hand, the 525/59.94/I analog sync, although it does not cover all the frame rates, can be used as a reference signal for 1125/59.94/I, 59.94/P, 29.97/PsF, 29.97/P, 750/59.94/P, 29.97/P, 525/59.94/P, and 525/59.94/I. It also covers 1125/23.98/PsF and 23.98/P with some limitation. The 625/50/I analog sync can be used as the reference signal for 1125/50/I, 50/P, 25/PsF, 25/P, 750/50/P, 25/P, 625/50/P, and 625/50/I. It could cover 1125/60/I, 60/P, 30/PsF, 30/P, 24/PsF, and 24/P with some limitation.

Table B.1 – Coverage of various external reference signals

<table>
<tr><th rowspan="2">1125-line system field or frame rates</th><th colspan="2">Tri-level analog sync</th><th colspan="2">525/59.94/I analog sync</th><th colspan="2">625/50/I analog sync</th></tr>
<tr><th>Potential use</th><th>Standard</th><th>Potential use</th><th>Standard</th><th>Potential use</th><th>Standard</th></tr>
<tr><td>59.94/I, 59.94/P, 29.97/PsF, 29.97/P</td><td rowspan="4">Yes, but limited (Note 1)</td><td rowspan="4">Rec. ITU-R BT.709-5</td><td>Yes</td><td>SMPTE 318M</td><td>No</td><td>—</td></tr>
<tr><td>50/I, 50/P, 25/PsF, 25/P</td><td>No</td><td>—</td><td>Yes</td><td>SMPTE 318M</td></tr>
<tr><td>23.98/PsF, 23.98/P</td><td>Yes but limited</td><td>SMPTE 318M-B (Note 3)</td><td>No</td><td>—</td></tr>
<tr><td>60/I, 60/P, 30/PsF, 30/P, 24/PsF, 24/P</td><td>No</td><td>—</td><td>Yes but limited</td><td>SMPTE 318M-A (Note 4)</td></tr>
</table>

Notes:

1. 1125/59.94/P.tri-level sync cannot synchronize 1080/59.94/I, 29.97/PsF, 29.97/P, 23.98/PsF or 23.98/P signals, and 1125/50/P tri-level sync cannot synchronize 1080/50/I, 25/PsF, 25/P, 24/P or 24/PsF signals.

2. A 525/59.94/I or 625/50/I analog sync carrying vertical interval time code (VITC) conforms to SMPTE 318M-A.

3. A 525/59.94/I analog sync carrying the 10-field reference coding conforms to SMPTE 318M-B.

4. The VITC frame count of a 625/50/I analog sync that conforms to SMPTE 318M-A will provide for alignment of 24-Hz video signals at 1s intervals, and 30-Hz and 60-Hz video signals at 0.2s intervals.

B.2.1 V and H sync phase relationship between 1125 tri-level analog sync and 525/59.94/I analog sync

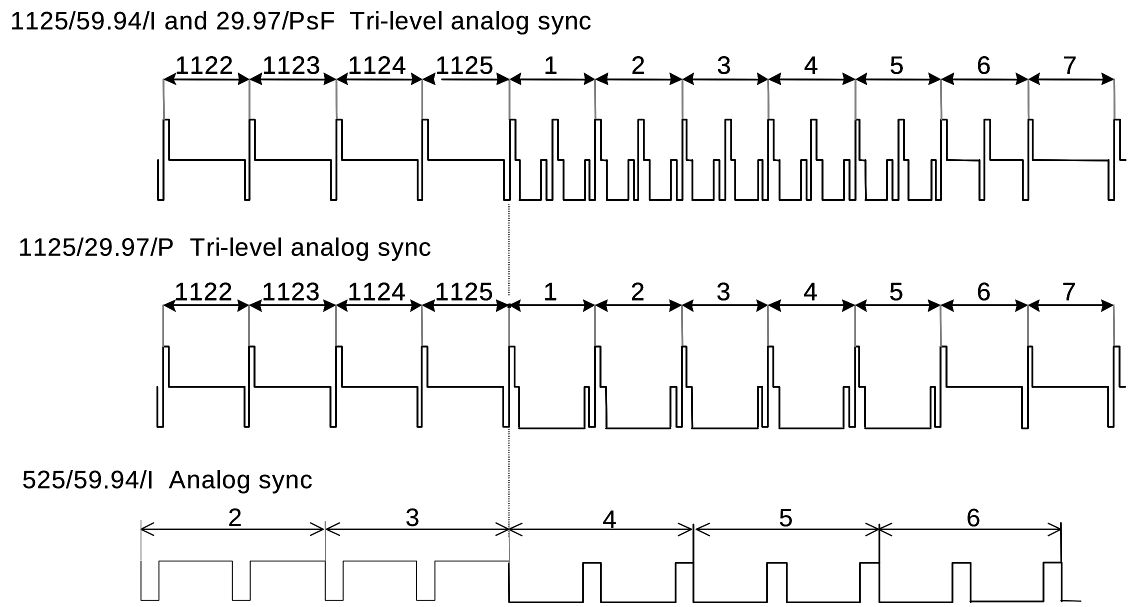


Figure B.1 – V and H sync phase relationship between 1125 tri-level sync and 525/59.94/I analog sync

B.2.2 V and H sync phase relationship between 1125 tri-level sync and 625/50/I analog sync

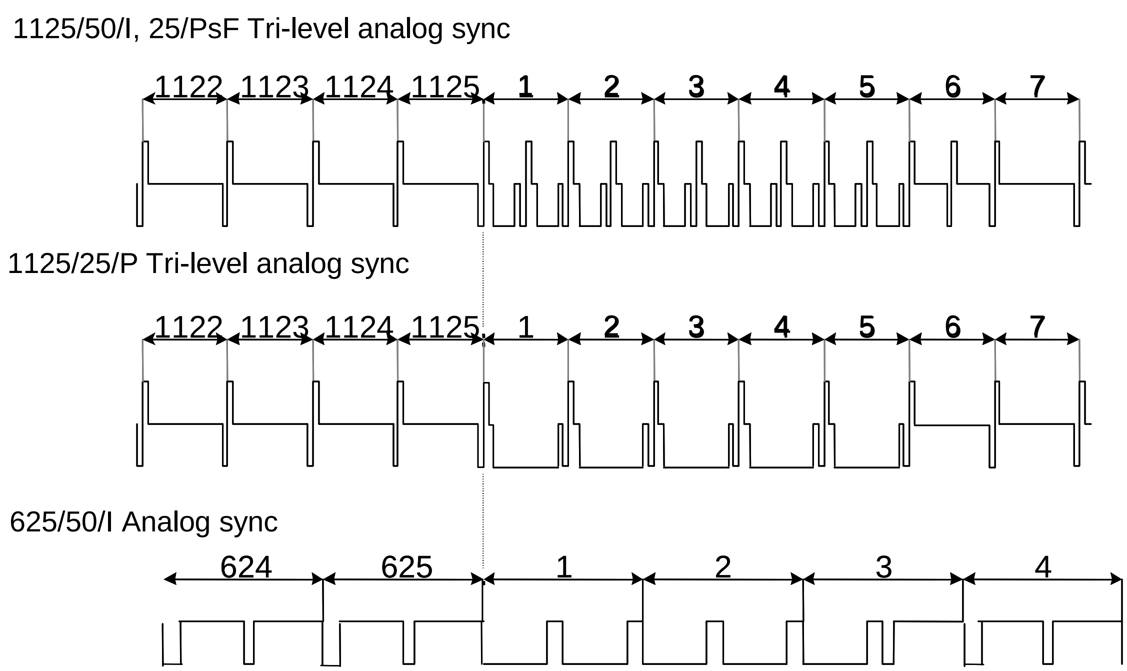


Figure B.2 – V and H sync phase relationship between 1125 tri-level sync and 625/50/I analog sync

B.2.3 V and H sync phase relationship between 1125 tri-level sync with 23.98 frames and 525/59.94/I with 10 fields ID analog sync

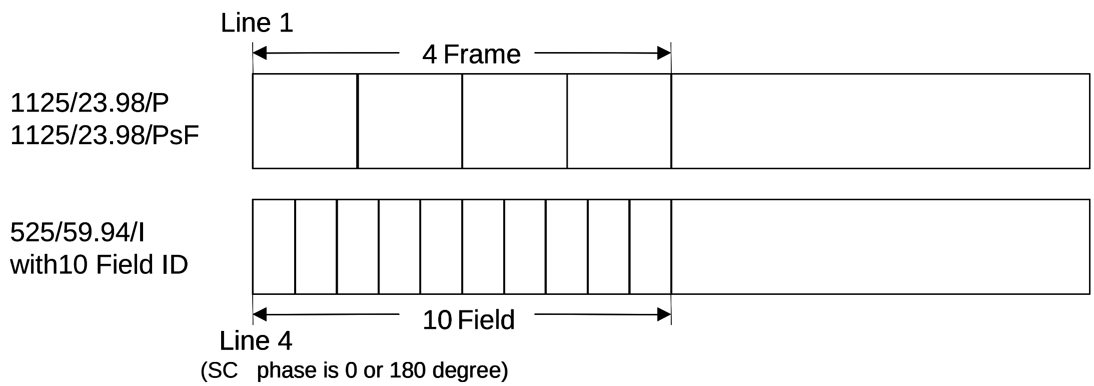


Figure B.3 – V and H sync phase relationship between 1125 tri-level sync and 525/59.94/I with 10 fields ID analog sync

B.2.4 1125/60/I, 30/P, 30/PsF, 24/P and 24/PsF

Tri-level sync with the same frame rates as those of the video signals are always used as the reference signals. The 525/59.94/I analog sync or 625/50/I analog sync cannot be used for these signals. However, the frame number sequence of a 625/50/I analog sync carrying Vertical Interval Time Code (VITC) conforming to SMPTE 12M-1 can be decoded to align every 6 frames of 60/I, 30/P or 30/PsF video, or every 24 frames of 24/P or 24/PsF video as shown in Figure B.4.

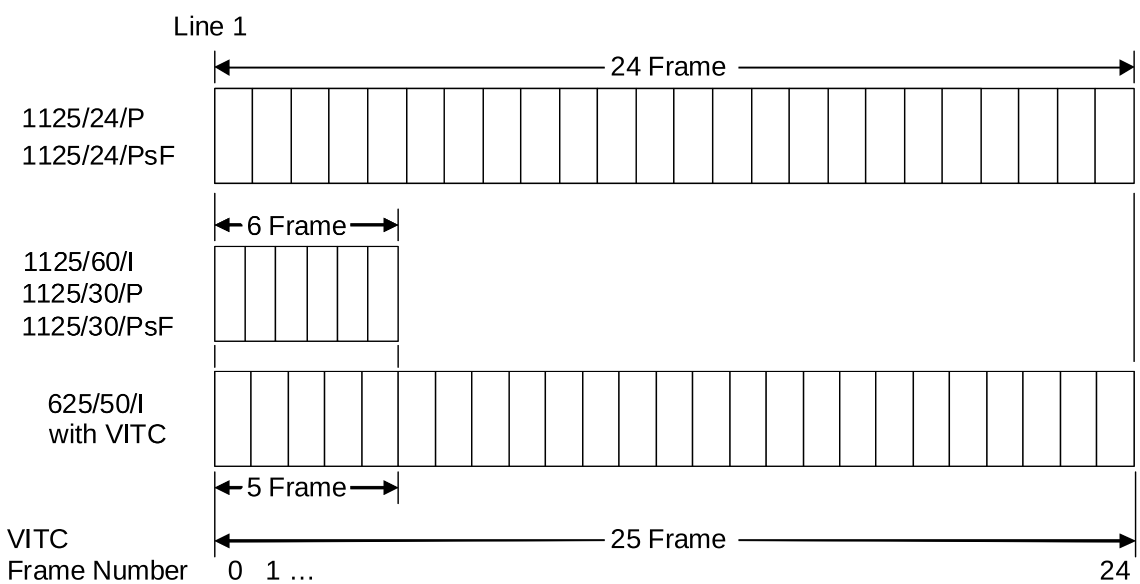


Figure B.4 – V and H sync (frame) phase relationship between 1125 tri-level sync and 625/50/I with VITC

B.3 Phase relationship between 1125/59.94/I and 525/59.94/I, video and sync signals

When 1125/59.94/I and 525/59.94/I equipment is used in the same studio, the following four options are applied to the phase relationship between 1125/59.94/I and 525/59.94/I, video and sync signals. Appropriate option of operation will be determined by the studio system architecture.

B.3.1 Same phase in 1125/59.94/I and 525/59.94/I, video and sync signals The horizontal reference point of line 1 of 1125/59.94/I and 4 of 525/59.94/I, video and sync are in phase as shown in Figure B.4.

B.3.2 525-line video signal delayed by 1 frame from the 1125-line video signal. 1125-line and 525-line, video and sync have the same waveform as shown in Figure B.4, but 525-line video is delayed by 1 frame from the 1125-line video.

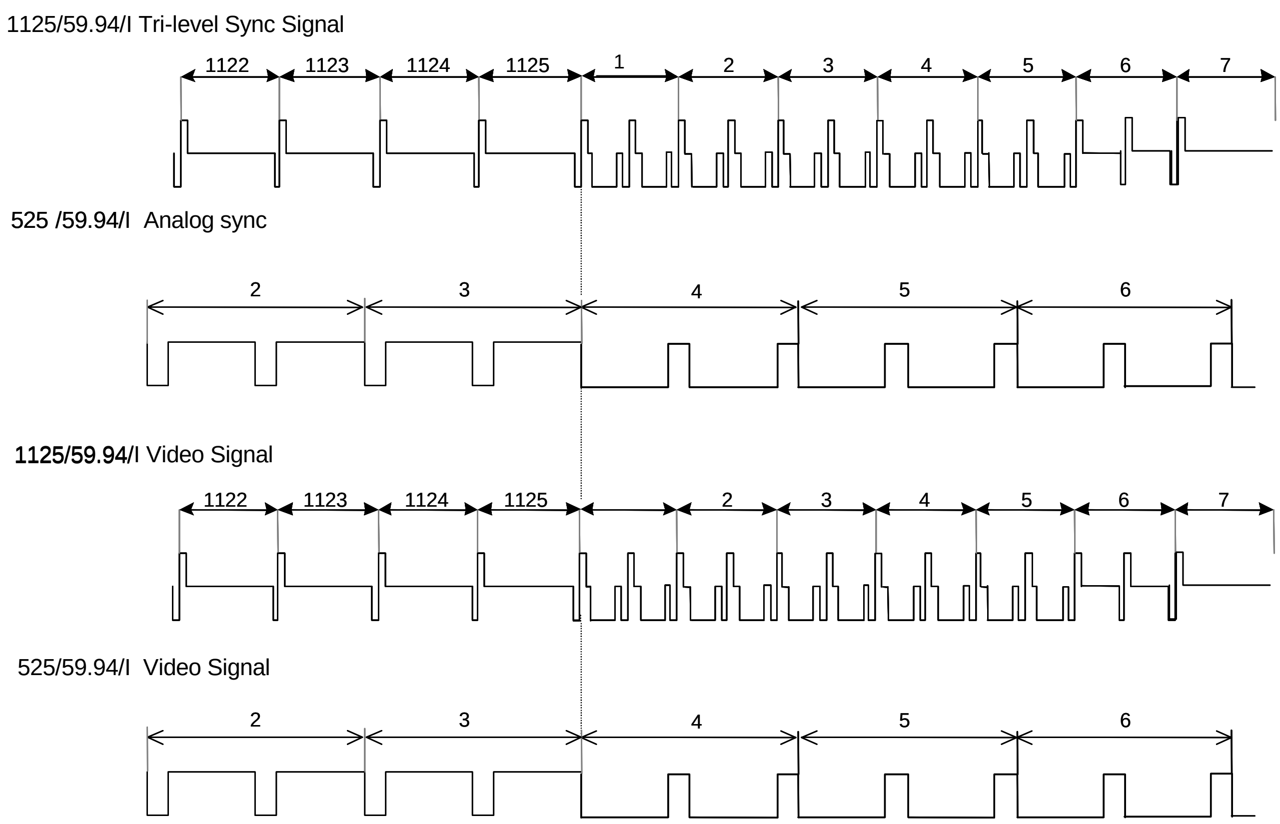


Figure B.4 – 525 and 1125 video signals are in phase, or 525 video signal delays by 1 frame from 1125 video signal

B.3.3 The 1125-line video signal synchronized with external reference signal and 525-line video signal delayed by 90 lines from 1125 video signal as shown in Figure B.5.

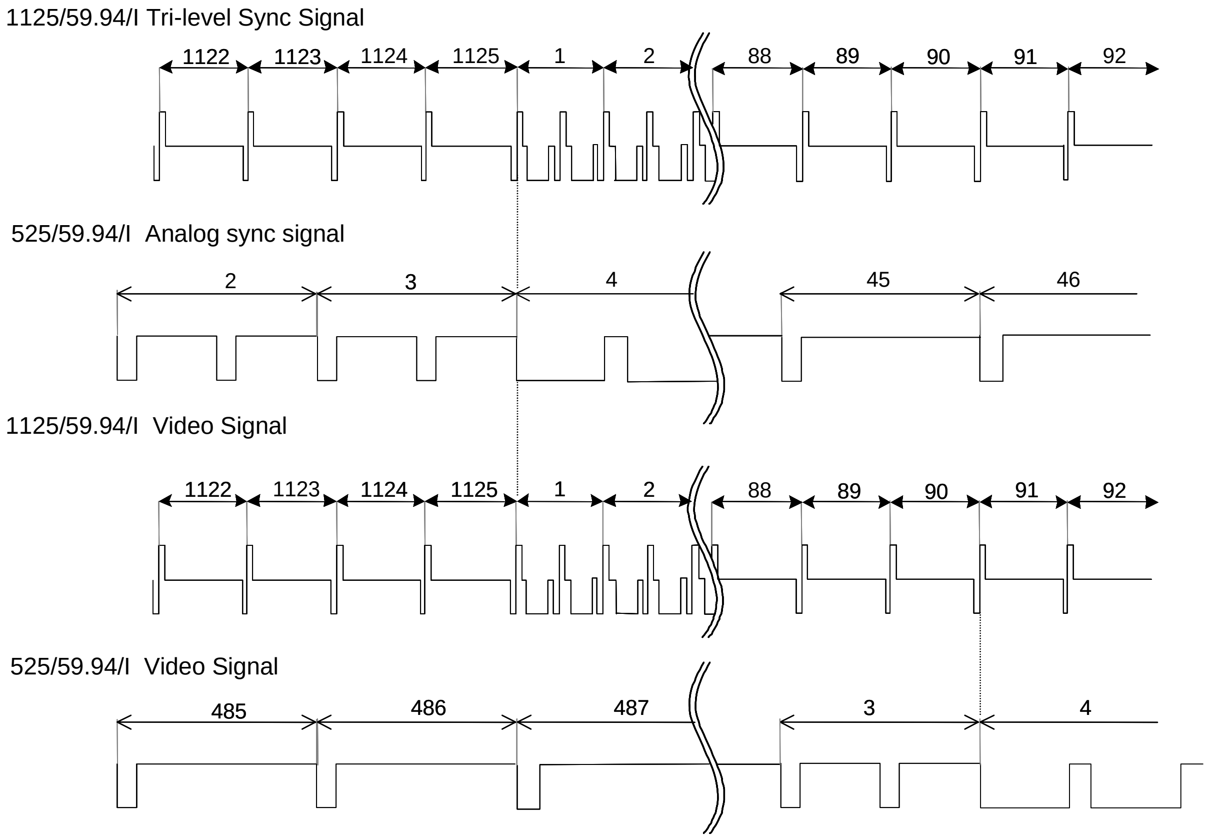


Figure B.5 – 1125 video signal synchronized with external reference signal and 525 video signal delayed by 90 lines from 1125 video signal

B.3.4 The 525-line video signal synchronized with external reference signal and 1125-line video signal advanced by 90 lines from the 525 video signal as shown in Figure B.6

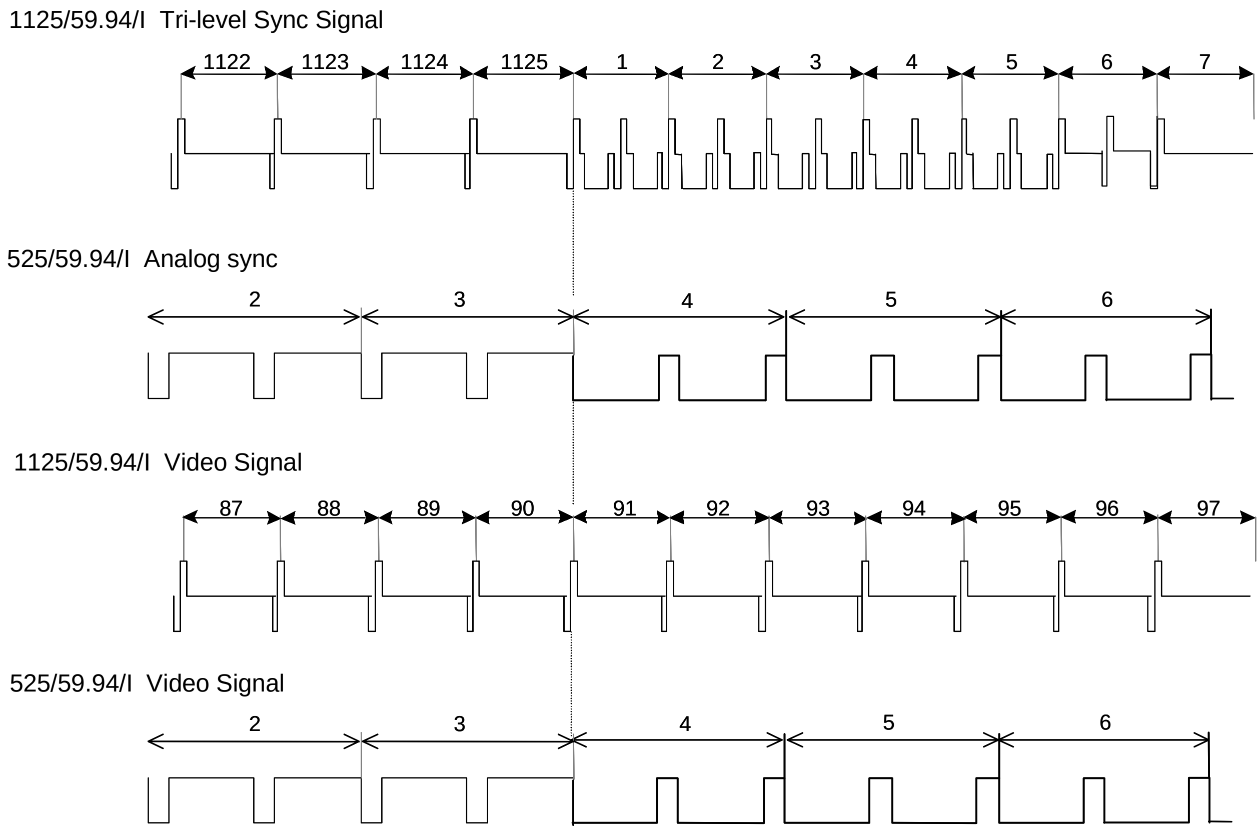


Figure B.6 – 525 video signal synchronized with external reference signal and 1125 video signal advanced by 90 lines from 525 video signal

Note: The same relationship applies to a 50-Hz system. In a 50-Hz system, line 1 of 625 corresponds to line 1 of 1125 and line 1 of 750; while in a 59.94-Hz system, line 4 of 525 corresponds to line 1 of 1125 and line 1 of 750.

B4. Tolerance of video output phase in the 1125/59.94/I signal

B.4.1 Tolerance of video output phase

The video output phase should synchronize with the external reference sync. The tolerance of video output phase shall be as follows. This term is not applied to routers and other similar equipment in which the external reference sync is used only to time the switching.

Analog video phase: ± 0.1µs

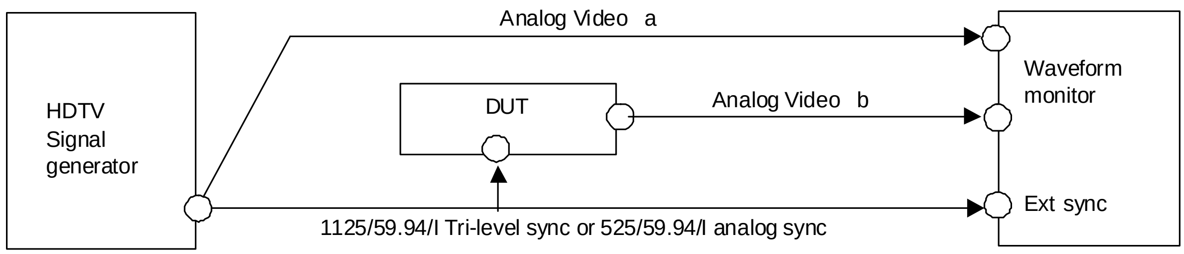
Digital video phase : ± 1.5µs

Note: ±1.5 µs in digital video phase is about 1/10 of half line period.

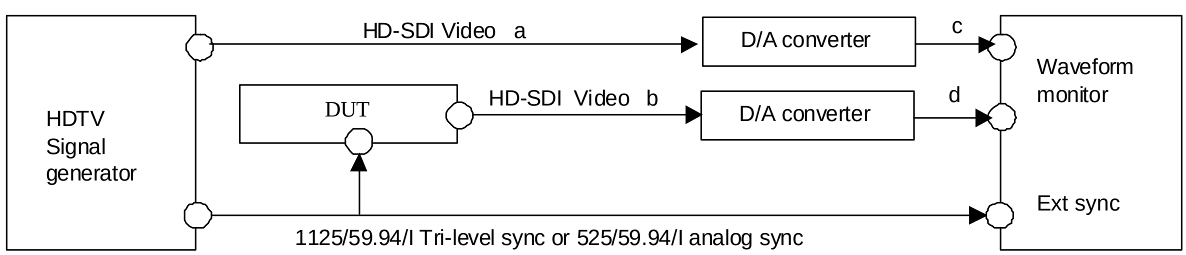
B.4.2 An example of Measurement method of video output phase

Figure B.7 shows the block diagrams how to measure the video output phase.

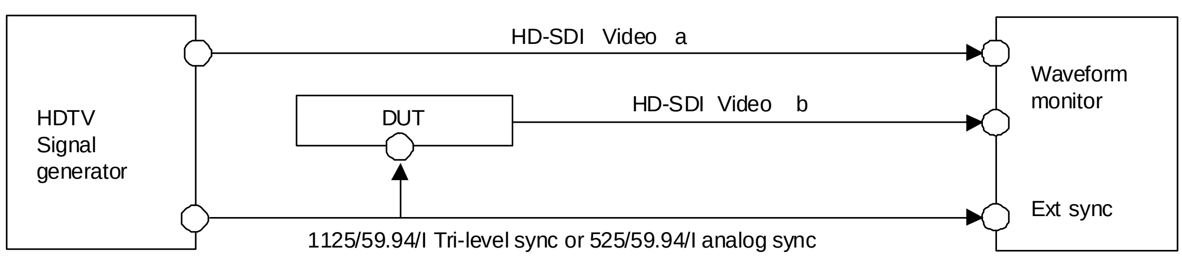
Figure B.7.1: HD analog video output and waveform monitor with analog input;
Figure B.7.2: HD-SDI video output and waveform monitor with analog input;
Figure B.7.3: HD-SDI video output and waveform monitor with HD-SDI input.



B.7.1 Analog video output and WFM with analog input



B.7.2 HD-SDI video output and WFM with analog input



B.7.3 HD-SDI video output and WFM with HD-SDI input

Figure B.7 – Block diagram for video output phase measurement

Annex C (Informative)
Line Number Relationship of the Source Signal and Interface Format

C.1 Segmented Frame (Ex. 1125/24/PsF)

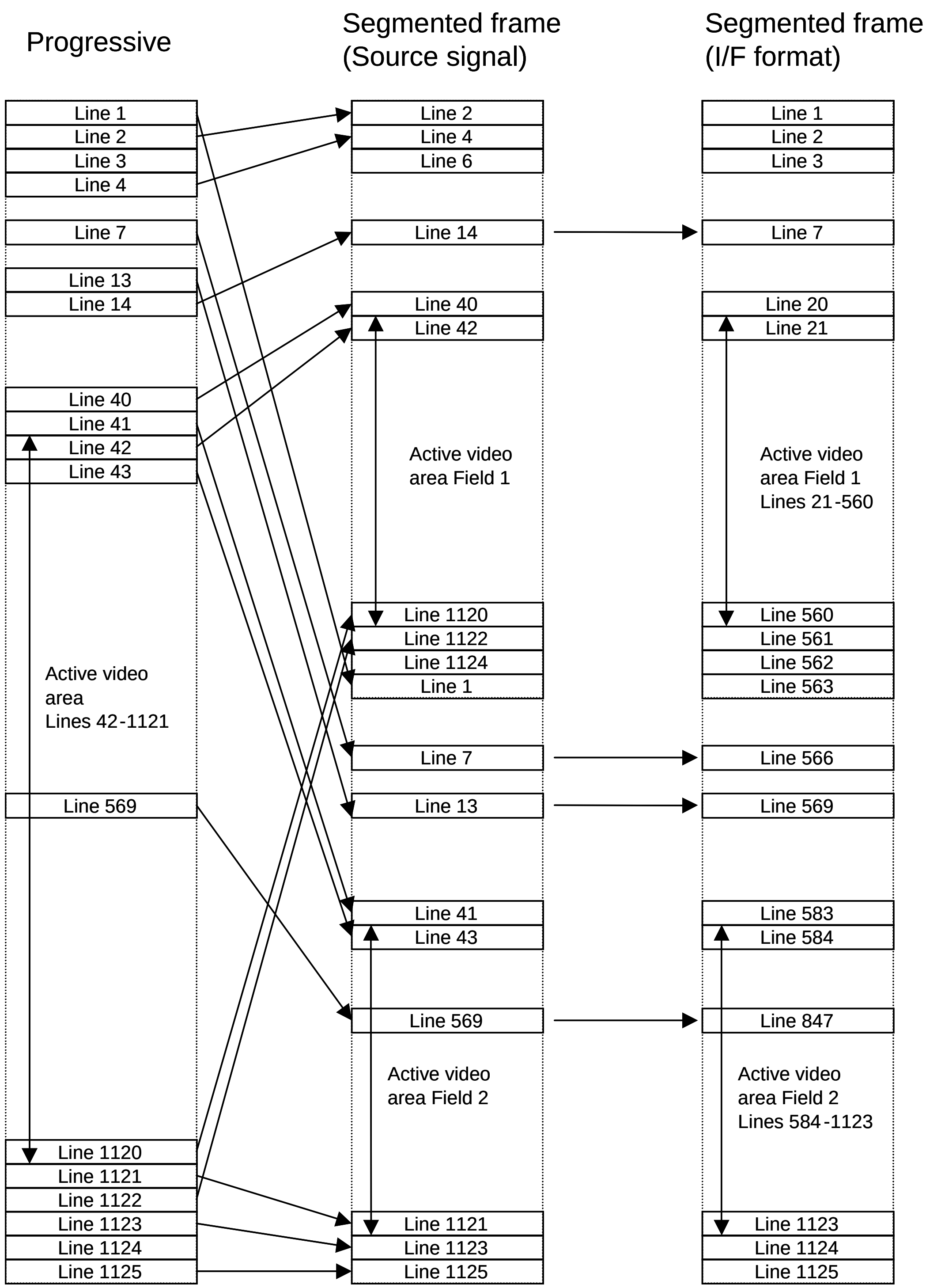


Figure C.1 – Line number relationship in segmented frame system

C.2 Dual Link (Ex. 525/59.94/P)

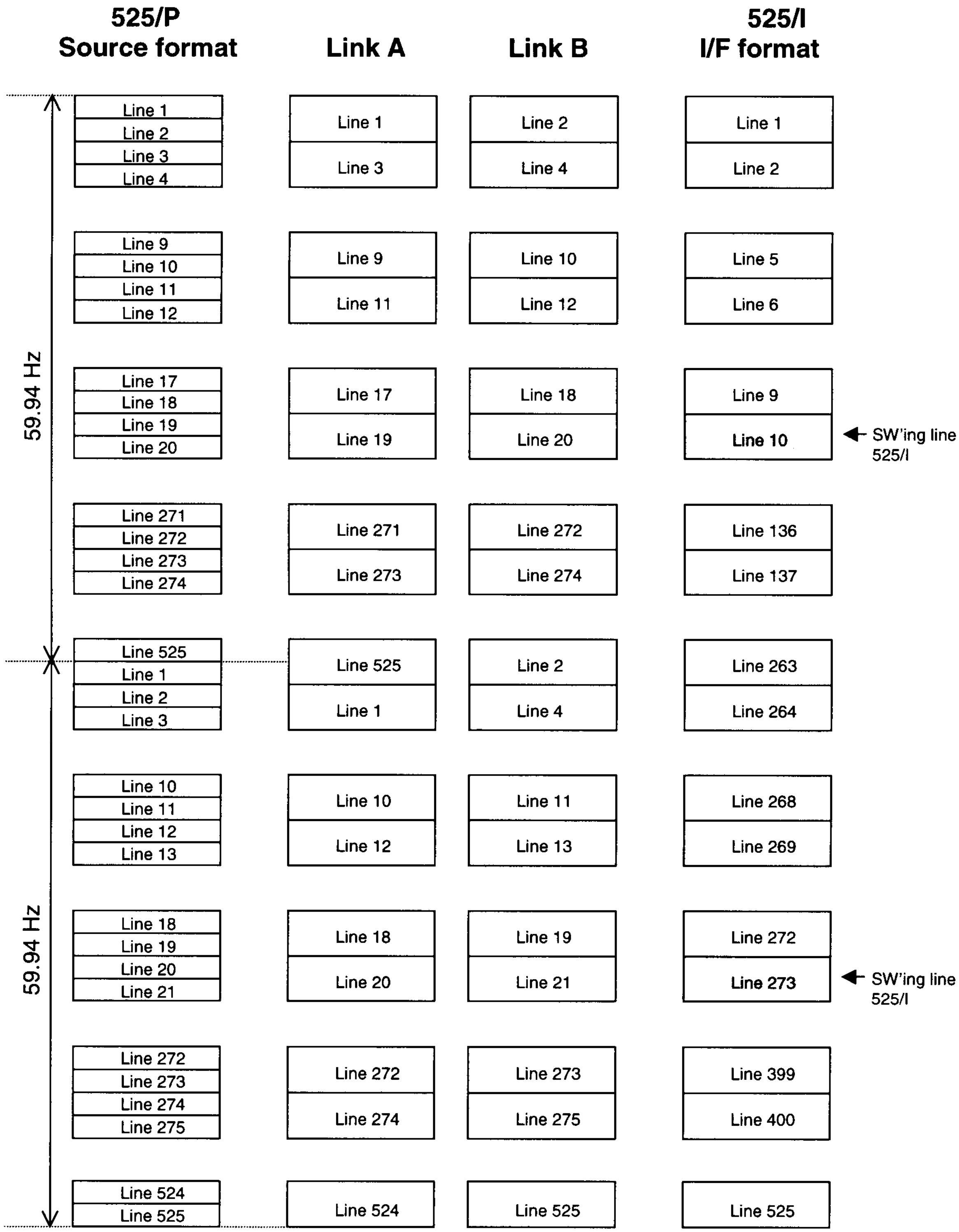


Figure C.2 – Line number relationship in dual-link 259M system

Annex D (Informative)
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