SMPTE RECOMMENDED PRACTICE

Bit-Parallel Digital Interface for 4:4:4:4 Component Video Signal (Single Link)

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1 Scope

This practice describes the means of interconnecting digital video equipment operating in system M (525/60) and complying with the 4:4:4 encoding parameters as defined in CCIR Recommendation 601-2, annex 1 with a nominal sampling frequency of 13.5 MHz. Provision is made to convey signal at 10-bit precision and to carry a fourth auxiliary channel as part of the signal multiplex (yielding 4:4:4:4 or 4×4 overall). The practice has application in the television studio over distances up to 100 m (320 ft). The characteristics of the interface are summarized below:

1.1 The video signal is transmitted in the form of three color-component signals and an auxiliary signal (G, B, R, and A or Y, C_B, C_R, and A).

1.2 The video signal is transmitted at the 4:4:4 family level of CCIR 601-2, with a nominal sampling frequency of 13.5 MHz. Provision is made to convey signals at 10-bit precision.

1.3 The bits of the digital code words that describe the video signal are transmitted in a parallel arrangement using 10 conductor pairs. Each pair carries a multiplexed stream of bits (of the same significance) of each of the component signals. Accordingly, the bit rate used in each pair is nominally 54 Mbits/s. An eleventh conductor pair carries a clock signal at 54 MHz.

1.4 The signals on the interface are transmitted using balanced conductor pairs for a distance up to 25 m (80 ft) without equalization and up to 100 m (320 ft) with appropriate equalization.

1.5 The interface consists of one transmitter and one receiver in a point-to-point connection.

1.6 Parameters of the signal format are chosen to facilitate conversion to and from a serial digital interface format.

1.7 The interface allows the transmission of appropriate ancillary signals that may be multiplexed into the data stream during video blanking intervals.

1.8 Where hexadecimal values are used, they are indicated by a subscript h, such as $3FF_h$; other values are decimal.

2 Normative references

The following standard contains provisions which, through reference in this text, constitute provisions of this practice. At the time of publication, the edition indicated was valid. All standards are subject to revision, and parties to agreements based on this

Approved September 1, 1993

practice are encouraged to investigate the possibility of applying the most recent edition of the standard indicated below.

SMPTE RP 157-1990, Key Signals

3 General

3.1 Signal convention

The signaling sense of the voltage appearing across the interconnection cable is positive binary and defined as follows (refer to figure 1):

3.1.1 The A terminal of the transmitter shall be negative with respect to the B terminal for a binary 0 (LOW or L or OFF) state.

3.1.2 The A terminal of the transmitter shall be positive with respect to the B terminal for a binary 1 (HIGH or H or ON) state.

3.2 Signal names

The data lines are designated DATA 0 through DATA 9. The group of 10 signals is identified by placing parentheses around the range of subscripts included, as DATA (0-9). DATA 9 is always the most significant bit.

3.3 Sin x/x

The characteristics of the data word at the interface are based on the assumption that the location of any required sin x/x correction is at the point where the digital signal is converted to an analog format.

3.4 Blanking interval

This practice does not require the device feeding the interface to transmit video data during the entire blanking interval. Therefore, ancillary information may be inserted into the horizontal blanking interval by the user within the constraints specified in 4.4 and 4.5.

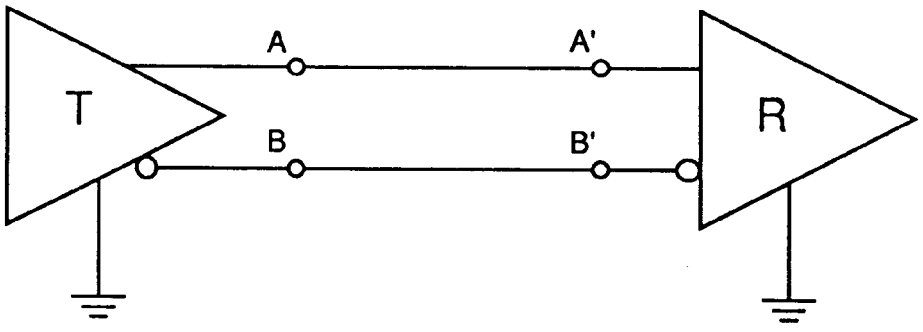
The vertical blanking duration is a minimum of nine lines. Ancillary information may be inserted into this nine-line interval by the user within the constraints specified in 4.4 and 4.5.

3.5 Signal specifications

All digital signal time intervals are specified at the half-amplitude points. All transitions are specified between the 20% and 80% amplitude points.

3.6 Electromagnetic interference

Digital apparatus can radiate a significant amount of energy at harmonics of the clock frequency. In the case of 13.5 MHz, clock harmonics lie at 121.5 MHz and 243 MHz, both of which are aeronautical distress frequencies. Equipment and system designers must, therefore, pay particular attention to the provision of adequate screening.



T = transmitter
R = receiver
A, A′ = the data line
B, B′ = the return line

Figure 1 -- Positive binary signal convention

4 Interface format

4.1 General description

The interface consists of a unidirectional, 11-pair interconnection between a transmitting equipment and a receiving equipment. Video data, timing reference information, and ancillary signals are time multiplexed and transferred on 10 data pairs in NRZ form. An eleventh pair provides a synchronous clock.

4.2 Encoding parameters

Table 1 summarizes the encoding parameter values, which are in accordance with CCIR 601-2.

4.3 Interface characteristics

Table 2 specifies the interface characteristics.

Table 1 – Encoding parameters

Matrixing formulas:	$Y = 0.299R + 0.587G + 0.114B$ $C_B = 0.564 (B-Y) = 0.500B - 0.169R - 0.331G$ $C_R = 0.713 (R-Y) = 0.500R - 0.419G - 0.081B$
Number of samples per line:	Total / Active
-- each of the 3 video components	858 / 720
-- auxiliary channel	858 / 720
-- total number of samples	3432 / 2880
Sampling structure:	Orthogonal: line, field, and frame repetitive.
Sampling frequency:	
-- each of 3 video components	13.5 MHz nominal
-- auxiliary channel	13.5 MHz nominal
Form of encoding:	Uniformly quantized, PCM, 10 bits per sample, for each of the primary signals and the auxiliary channel.
Correspondence between video signal levels and quantization levels:	
-- each of the 3 primaries (G, B, R), the luminance signal (Y), and the auxiliary channel.	877 quantization levels with the black corresponding to level 64 and the peak white level corresponding to level 940.
-- each color-difference signal (C_B, C_R)	897 quantization levels symmetrically distributed about level 512, corresponding to the zero signal.

Table 2 – Interface characteristics

Digital format:	Parallel: 11 balanced signal pairs carrying clock and 10 data bits
Interface clock:	54.0 MHz nominal
Voltage levels:	Standard ECL (10KH series)
Driver impedance:	Standard ECL (10KH series)
Receiver impedance:	110 ohms nominal, balanced

4.4 Digital blanking relationship

4.4.1 Horizontal sync relationship

Figure 2 shows the relationship between video signals in the digital and analog domains for 525-line systems. Figure 3 shows the multiplex structure.

Transmitted during each active line are 2880 multiplexed green, red, blue, and auxiliary or luminance, chrominance, and auxiliary values.

Eight of the remaining 552 interface clock intervals are used to transmit synchronizing information; the other 544 interface clock intervals may be used to carry ancillary information.

The first of these 3432 interface clock intervals is designated line word 0 for the purpose of reference only. The 3432 sample words per total line are, therefore, numbered 0 through 1715. Intervals 0 through 3431, inclusive, contain video data. The interface clock intervals occurring during digital blanking are designated 2880 through 3431.

Intervals 2880 through 2883 are reserved for the end-of-active video (EAV) timing reference described in 4.5.4. Intervals 3428 through 3431 are reserved for the start-of-active-video (SAV) timing reference described in 4.5.4.

The half-amplitude point of the leading (falling) edge of the analog horizontal sync signal shall be coincident with a sample point which would be conveyed by word 2945, if carried across the interface.

4.4.2 Vertical sync relationship

Figure 4 shows the relationship between video signals in the digital and analog domains for 525-line systems.

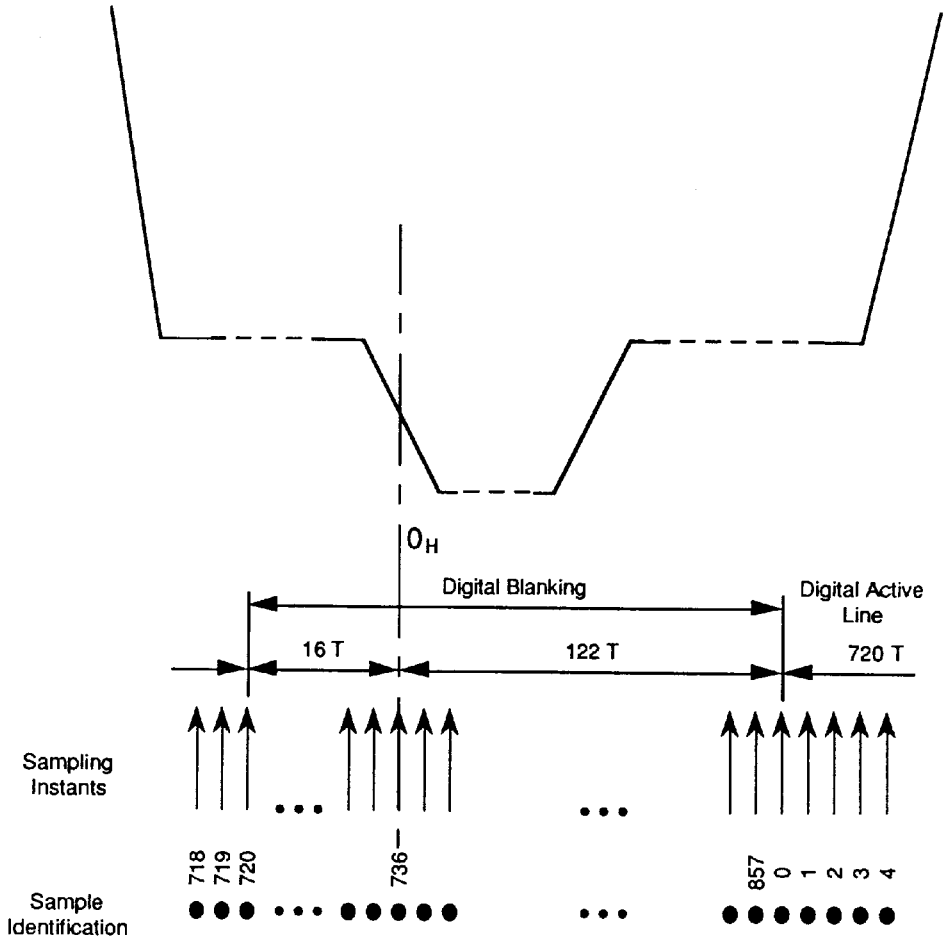


Figure 2 – Horizontal sync relationship

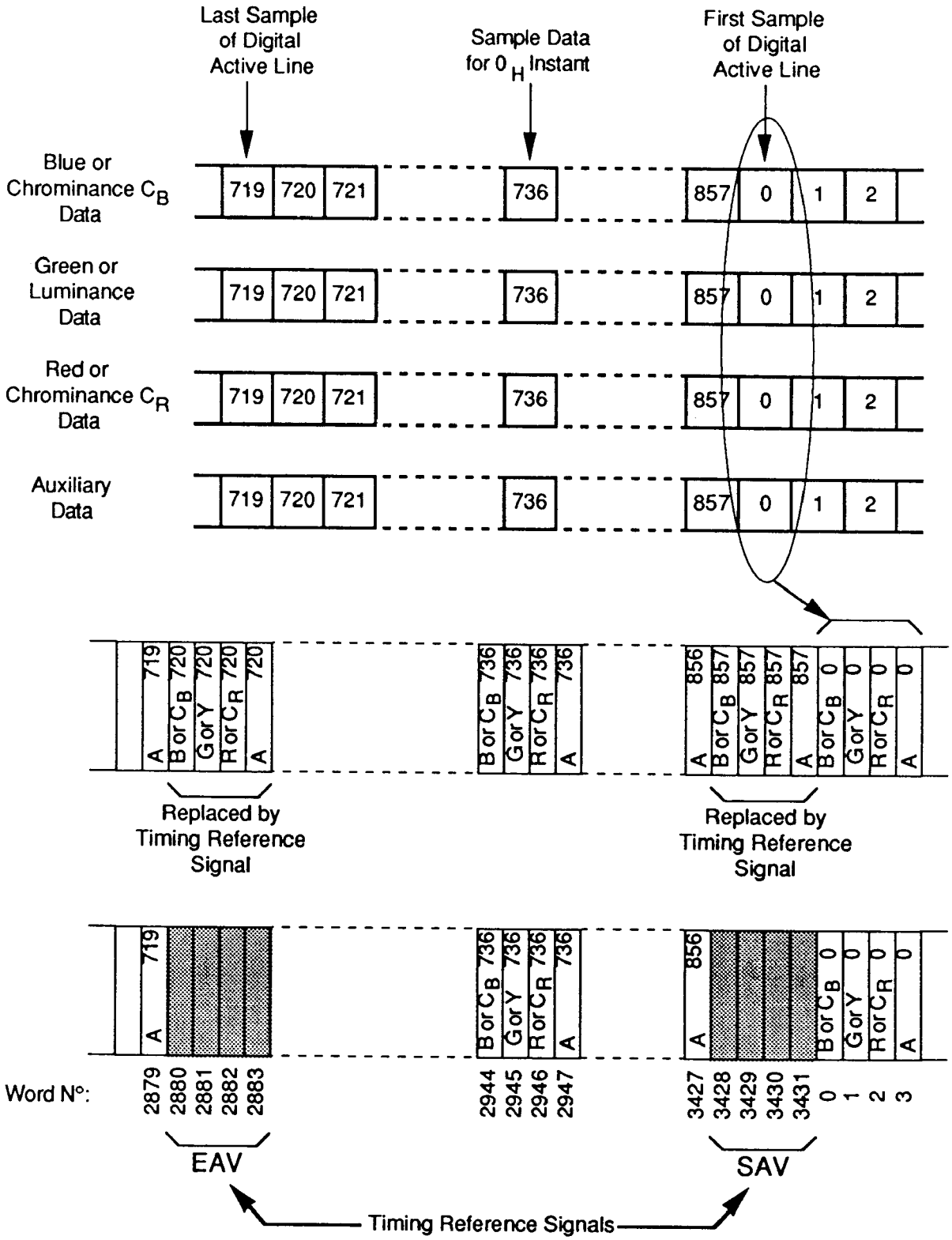
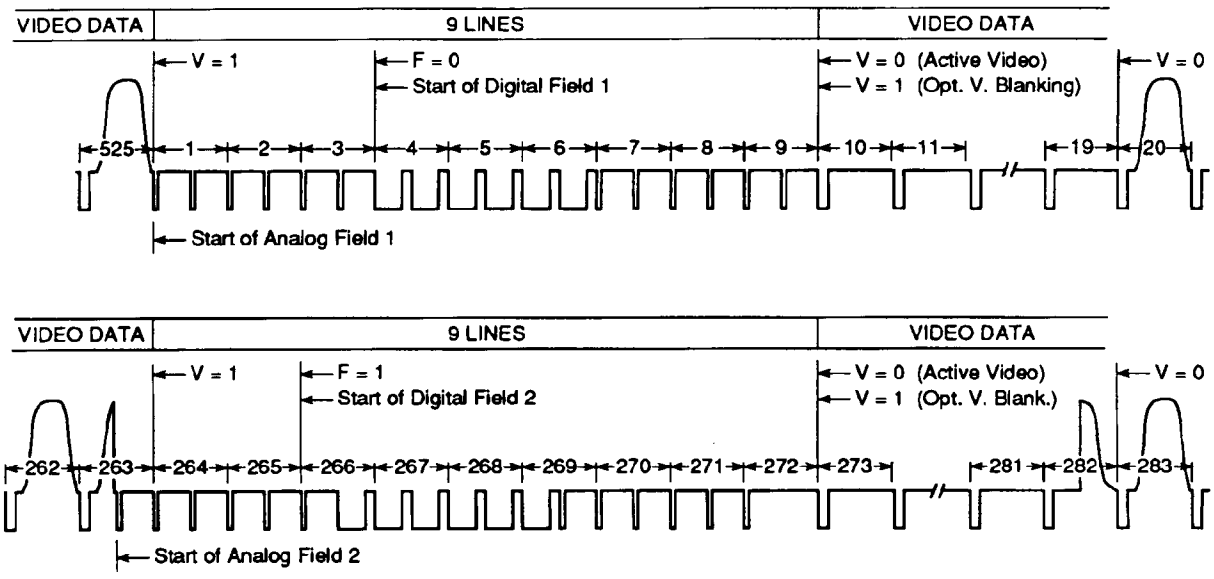


Figure 3 – Multiplex structure



Digital field 1 has 262 lines
Digital field 2 has 263 lines

Figure 4 -- Relationship of video data/vertical sync

4.5 Video data signal format

4.5.1 Data signal format

Data is transmitted across the interface on 10 data pairs: DATA 0 through DATA 9. DATA 9 is the most significant bit (MSB). Of the 1024 levels (digital levels 4 through 1019 or 004_h through $3FB_h$ in the hexadecimal representation) of the 10-bit word, 1016 are used to express quantized values.

Data levels 0 to 3 and 1020 to 1023 (000_h to 003_h and $3FC_h$ to $3FF_h$ in the hexadecimal representation) are reserved to indicate timing references.

4.5.2 Auxiliary signal

The auxiliary signal (A) is used to transmit the key signal associated with the G, B, R or the Y, C_B, C_R signals. The auxiliary signal channel can also be used to transmit a Y signal for monitoring in the case of G, B, R signals or for other purposes.

4.5.2.1 Key signal

On the key signal, black level (040_h) represents complete transparency and white level ($3AD_h$) represents complete opacity. The key signal should comply with SMPTE RP 157.

4.5.3 Multiplex structure

The video data words shall be conveyed as a 27-Mword/s multiplex in the following order:

B G R A B ... or C_B Y C_R A C_B ...

The first video data word in each active line period shall be B or C_B.

4.5.4 Timing reference signals — Video

Figure 2 shows the position of the timing reference signals with respect to horizontal blanking in the multiplexed data stream. It is implicit that the timing reference signals are contiguous with the video data,

when present, and continue through the vertical blanking interval. Each timing reference signal consists of a four-word sequence in the following format: 3FF 000 000 PQR.

The first three words are a fixed preamble. The fourth word shall contain information defining:

– even field (field 2) identification;
– state of vertical blanking;
– state of horizontal blanking;
– G B R A or C_B Y C_R A signals.

Figure 5 is a spatial representation of the timing reference signals during a television frame.

Assignment of bits within the fourth word is shown in table 3.

P0, P1, P2, and P3 have states dependent on states of bits F, V, and H according to table 4.

Lines are numbered from 1 through 525 as shown in figure 4. Vertical blanking in the digital interface is in full-line increments. EAV and SAV are the digital horizontal synchronization signals and occur on every line. The interval starting at EAV and ending with SAV is the digital horizontal blanking period as shown in figure 3.

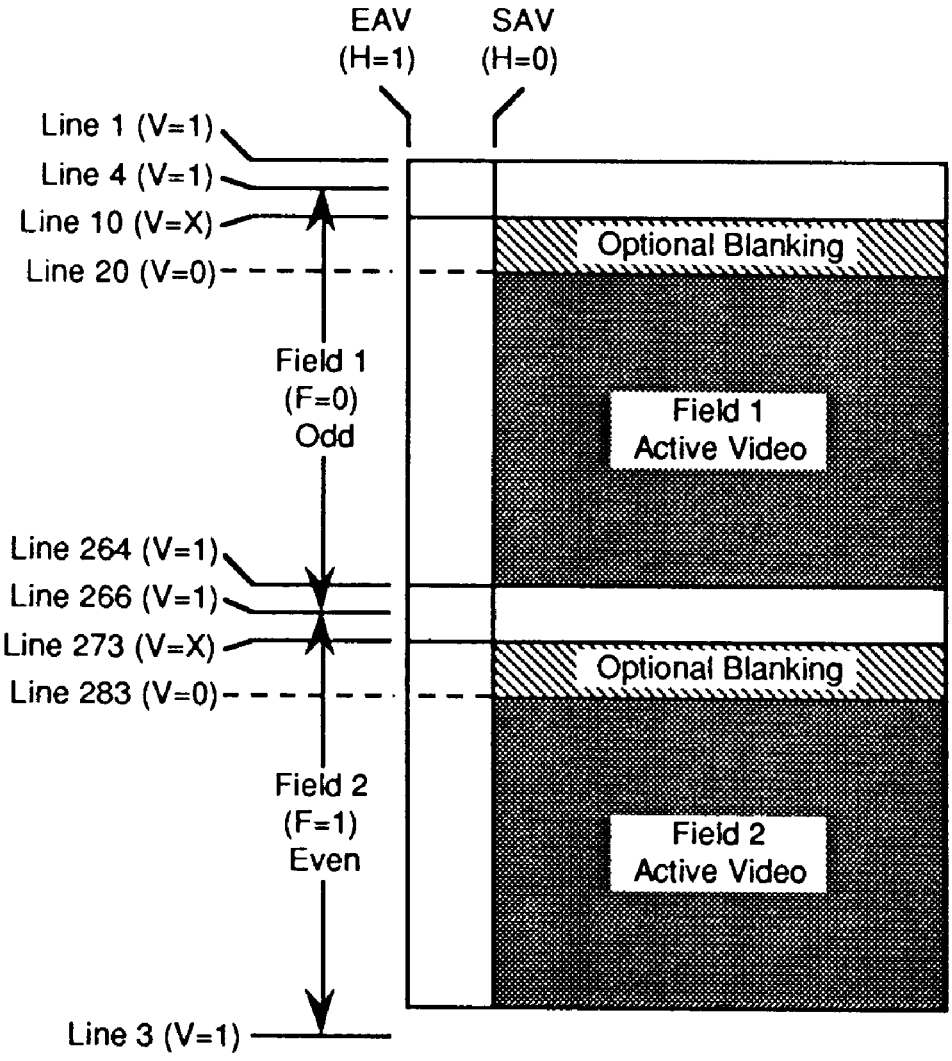


Figure 5 – Timing reference signal locations

Table 3 – Timing reference signals

Bit	Word 2880 and 3428	Word 2881 and 3429	Word 2882 and 3430	Word 2883 and 3431	
9	1	0	0	1	Fixed
8	1	0	0	F	F = 0 during field 1 F = 1 during field 2
7	1	0	0	V	V = 0 during active video V = 1 during vertical blanking
6	1	0	0	H	H = 1 for EAV H = 0 for SAV
5	1	0	0	S	S = 0 for GBR signals S = 1 for Y, C_B, C_R signals
4	1	0	0	P4	See table 4
3	1	0	0	P3	
2	1	0	0	P2	
1	1	0	0	P1	
0	1	0	0	P0	

NOTES
1 The H, V, and F bits (bits 6-8) provide the necessary information. Bits (0-4) provide error detection and correction information.
2 Each 525-line digital video frame is divided into two fields. Field 1 contains 262 complete horizontal lines. Field 2 contains 263 complete horizontal lines.
3 The protection bits allow correction of all single-bit errors and detection of two-bit errors.

Table 4 -- Protection bit states

Bit	9	8	7	6	5	4	3	2	1	0
		F	V	H	S	P4	P3	P2	P1	P0
	1	0	0	0	0	0	0	0	0	0
	1	0	0	0	1	0	1	1	1	0
	1	0	0	1	0	1	0	1	1	0
	1	0	0	1	1	1	1	0	0	0
	1	0	1	0	0	1	1	1	0	0
	1	0	1	0	1	1	0	0	1	0
	1	0	1	1	0	0	1	0	1	0
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	1	1	0	1	1	0	0	0	1	0
	1	1	1	0	0	0	0	1	1	0
	1	1	1	0	1	0	1	0	0	0
	1	1	1	1	0	1	0	0	0	0
	1	1	1	1	1	1	1	1	1	0

4.6 Ancillary data

Small blocks of data, less than 544 words in total length, including the HANC sequence (as described in 4.6.2), can be transmitted within the horizontal blanking period on every line.

Large blocks of data, up to 2880 words in total length, including the ANC sequence, can be transmitted within the interval starting with the end of SAV and terminating with the beginning of EAV on lines 1 through 19 and 264 through 282 only.

Video data will not be present on lines 1-9 and 264-272 and may optionally be present on lines 10-19 and 273-282. Ancillary data could be optionally transmitted in the active portion of these lines.

The words during:

– the horizontal blanking period on every line;
– the active portion of lines 1-9 and 264-272;
– the active portion of lines 10-19 and 273-282 (when video data is not present)

not used to transmit ancillary data must have the following values:

– 040_h for GBR signals;
– 040_h for the words corresponding to Y samples;
– 200_h for the words corresponding to C_B and C_R samples in Y, C_B, C_R signals.

4.6.1 Ancillary data signal format

Ancillary data may be inserted in any portion of the data stream not occupied by timing reference signals or video data (see 4.4.1 and 4.4.2). Two categories of ancillary data, HANC and VANC, are defined for different portions of the data stream. Note that the three-word header used to identify ancillary data is the same for HANC and VANC.

4.6.2 HANC data

HANC data are permitted in all horizontal intervals, but not in the active portion of lines. HANC data are of 10-bit format, and each block of HANC data is preceded by the three-word ancillary data header 000 3FF 3FF.

The ancillary data header may occur multiple times during each horizontal blanking period if different blocks of data are transmitted. All permitted data identification words and data formats will protect the values (000_h to 003_h) and ($3FC_h$ to $3FF_h$).

4.6.3 VANC data

VANC data are permitted only in the active portion of lines 1-13, 15-19, 264-276, and 278-282. (Lines 14 and 277 are reserved for digital vertical interval time code (DVITC) and video index. VANC data are of 8-bit format, and each block of VANC data is preceded by the three-word ancillary data header 000 3FF 3FF.

The ancillary data header may occur multiple times during each line period if different blocks of data are transmitted. All permitted data identification words and data formats will protect the values (000_h to 003_h) and ($3FC_h$ to $3FF_h$).

4.7 Digital vertical interval time code and video index

Digital vertical interval time code (DVITC) and video index, if present, are carried by the data in the active portion of lines 14 and 277.

4.7.1 DVITC

This signal, if present, is carried by the luminance data in the active portion of lines 14 and 277.

4.7.2 Video index

This signal, if present, is carried by the color-difference data in the active portion of lines 14 and 277. A total of 90 8-bit data words is represented serially by DATA(2) of the 1440 B and R or color-difference samples of the active portion of the line.

The first word of the active portion of the line (word 0 of the multiplexed signal, normally a B or C_B sample) represents the least significant bit (bit 0) of video index word 0. The second word represents bit 1 of the same word, etc. Word 1438 of the multiplexed signal, normally an R or C_R sample, represents the most significant bit (bit 7) of video index word 89.

For all samples, a value of 204_h represents a binary 1 for the appropriate video index bit, and a value of 200_h represents a binary 0 for the appropriate video index bit. This transmission method ensures that, after digital to analog conversion, the video signal may be sent to an NTSC encoder without any requirement for special blanking. DVITC will be preserved through the

encoder without interference from any video index information which may be present.

4.8 Clock signal

4.8.1 Clock signal description (at transmitter)

The clock signal is a 54-MHz square wave as shown in figure 6. The clock pulse width (tw) is 9.3 ns ± 1.5 ns.

4.8.2 Clock jitter

The peak-to-peak jitter between rising edges shall be within 1.5 ns of the average time of the rising edge computed over at least one field.

4.8.3 Clock data timing relationship

The positive transition of the clock signal nominally occurs midway between data transitions (figure 6).

5 Electrical characteristics

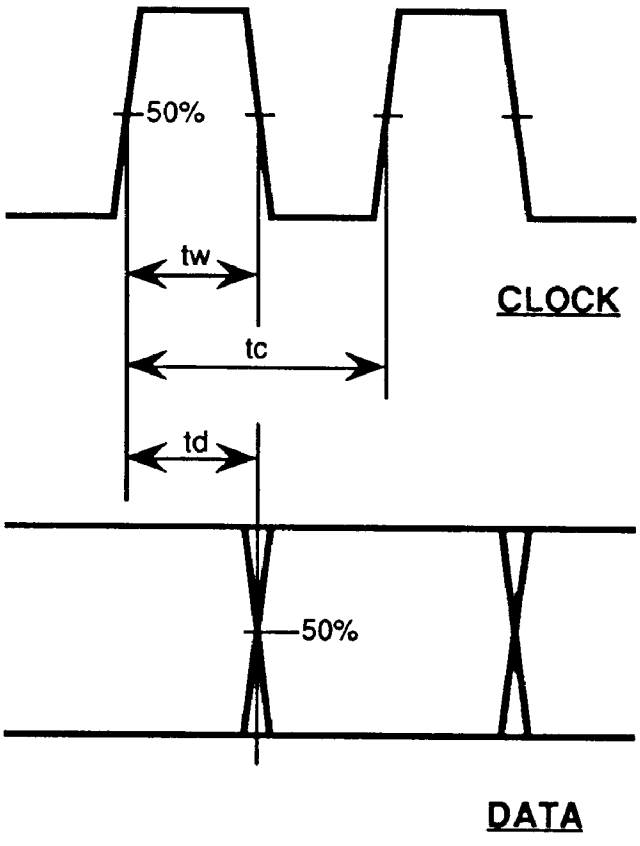
5.1 General

The eleven signals shall be transmitted via balanced signal pairs. Although the use of ECL technology is not specified, the line driver and receiver must be ECL-compatible to permit the use of standard ECL parts for either or both ends in applications where such ECL parts are deemed adequate. Standard ECL parameters are provided in annex A.

5.2 Transmitter characteristics

5.2.1 Output impedance

The transmitter shall have a balanced output with a maximum output impedance of 110 ohms.



$tw = 9.3 \pm 1.5$ ns

$tc = \frac{1}{3432\ f_h} = 18.5$ ns (nominal)

$td = 9.3 \pm 1.5$ ns

$f_h = 15.734...$KHz (nominal)

Figure 6 – Clock to data timing (at transmitter)

5.2.2 Common mode voltage

The average of the voltages on the two terminals of the line driver shall be –1.3 V ± 15% with reference to the ground terminal.

5.2.3 Signal amplitude

The generated signal shall lie between 0.8 V peak-to-peak and 2.0 V peak-to-peak, measured across a 110-ohm resistor connected to the output terminals without any transmission line.

5.2.4 Rise and fall times

Rise and fall times shall be no longer than 3 ns and differ by not more than 1 ns, as measured between the 20% and 80% amplitude points across a 110-ohm resistor connected to the output terminals without any transmission line.

5.3 Receiver characteristics

5.3.1 Terminating impedance

The cable shall be terminated by 110 ohms ± 10 ohms.

5.3.2 Maximum input signal

The line receiver must sense properly the binary data when connected directly to a line driver operating at the extreme voltage limits permitted by 5.2.3.

5.3.3 Input sensitivity

The receiver shall require a differential input voltage of no more than 185 mV to attain correctly the intended binary state.

5.3.4 Common mode rejection

The receiver shall operate correctly in the presence of common mode noise having a maximum amplitude of ± 0.5 V.

5.3.5 Differential delay

The receiver shall operate with a differential delay between the received clock and any received data signals up to 5.5 ns.

6 Mechanical characteristics

6.1 General

This clause defines the mechanical specifications for the interface of digital video systems used in environments where the physical distance between devices is limited and the general physical environment can be termed interior.

6.2 Interconnecting cable characteristics

The interface is designed to operate with a nominal signal pair impedance of 110 ohms.

6.2.1 Cable length

The majority of applications of this interface involves lengths less than 50 m. For these lengths, cables with reasonable uniformity will generally give satisfactory results. For cable lengths greater than 25 m, the cable and termination characteristics become more critical, in some cases requiring equalization.

6.2.2 Cable construction

The cable shall contain 12 pairs of conductors of which 11 pairs shall be used as signal lines. The remaining pair shall be used as system ground.

The cable shall be constructed to minimize the effects of crosstalk between signal lines, the susceptibility of the signal lines to external noise, and the transmission of interface signals to the external environment.

The cable shall contain an overall shield to minimize radiation, carried through the cable assembly and connectors via the cable shield pins and the connector body at each end. The cable shall be constructed to minimize the differential delay between any two conductor pairs.

6.3 Connector characteristics

6.3.1 Mechanical considerations

The connectors shall have the mechanical characteristics conforming to the industry standard 25 contact D subminiature connector described below. Additional information may be found in MIL-C-24308C.

(Most applications of this interface require that the connectors be inserted many times. ECL voltage and

current levels are relatively low. The materials used in the connector should be appropriate to the application.)

6.3.2 Connector contact assignments

The connector contact assignments shall be in accordance with table 5.

6.3.3 Cable connector assembly

Cable connectors employ pin contacts and equipment connectors employ socket contacts (see figure 7).

6.3.4 Connector retaining mechanism

The cable connectors shall be provided with #4-40 mounting screws and the equipment connectors shall be provided with female screw locks or mating threads (see annex B).

Table 5 -- Connector contact assignments

Pin	Signal line	Pin	Signal line
1	Clock	14	Clock return
2	System ground A	15	System ground B
3	DATA 9 (MSB)	16	DATA 9 return
4	DATA 8	17	DATA 8 return
5	DATA 7	18	DATA 7 return
6	DATA 6	19	DATA 6 return
7	DATA 5	20	DATA 5 return
8	DATA 4	21	DATA 4 return
9	DATA 3	22	DATA 3 return
10	DATA 2	23	DATA 2 return
11	DATA 1	24	DATA 1 return
12	DATA 0	25	DATA 0 return
13	Cable shield		

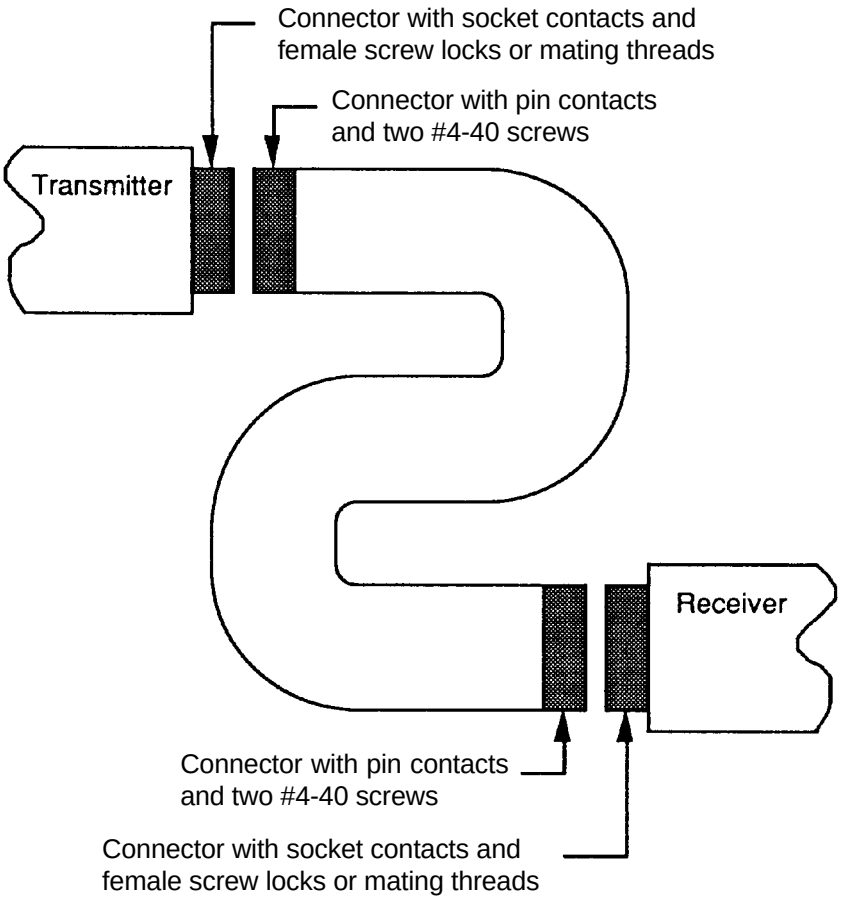


Figure 7 -- Cable connector assembly

Annex A (informative)
ECL 10H000 parameters

A.1 Standard ECL parameters

"Standard ECL" in this application means an integrated circuit device of the ECL 10H000 series or the equivalent. Typical key parameters are:

System power supply (V): --4.7 V to --5.7 V
--5.2 V nominal

Logic states with respect to ground (typical):
"1" = --0.8 V = High (H)
"0" = --1.85 V = Low (L)

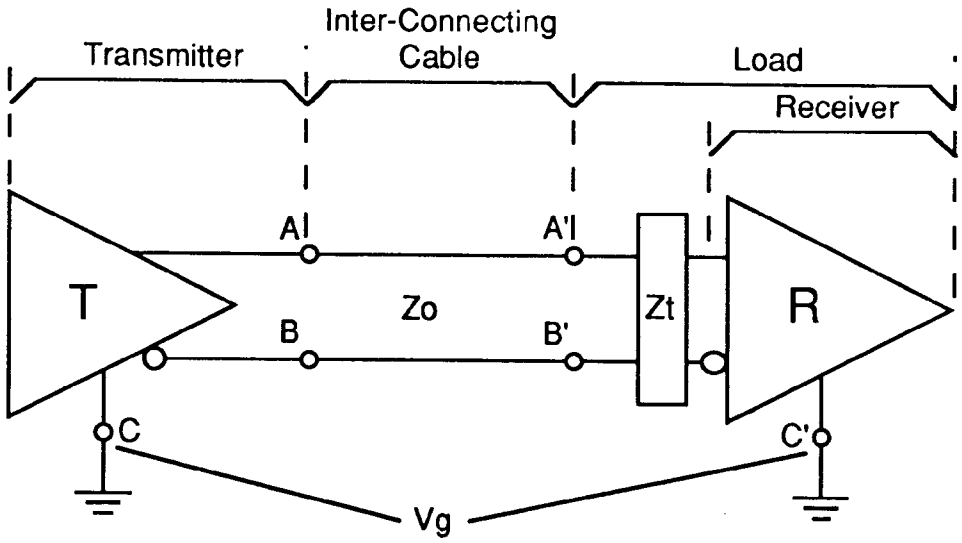
Output impedance: Open emitter-follower output (7 ohm typical) to drive terminated lines

Propagation delay: 1-2 ns per gate. Typical edge speeds are 1-2 ns (20% to 80%)

A.2 Balanced interface circuit

Each circuit consists of three parts as shown in figure A.1: the line driver, the balanced interconnecting cable, and the load. The line driver is comprised of a single transmitter (T) with a low-output impedance. The load is comprised of a single receiver (R) and a cable termination impedance (Zt).

Electrical characteristics of the receiver without cable termination shall conform to standard balanced ECL specifications. Use of a cable termination (Zt) is mandatory. Zt shall be nominally 110 ohms.



A, A′ = data line
B, B′ = return line
Zt = cable termination
A, B = transmitter interface points
A′, B′ = load interface points
C = transmitter circuit ground
C′ = load circuit ground
Vg = ground potential difference
Zo = cable characteristic impedance

Figure A.1 -- Balanced interface circuit

Annex B (informative)
Connector characteristics

The interface employs the 25 contact D-subminiature connector, with the connectors on the transmitter and receivers using socket contact and the connectors on the cable both using pin contacts. Connectors are locked together by two #4-40 screws on the cable connectors, which go in the female screw lock mounted on the equipment connector. Detailed dimensions for the connector are given in MIL-C-24308C.

The relative position of the connector and the female screw lock is defined in figure B.1. The connector spacing is defined in figure B.2.

It is recommended that the cable connectors employ a conductive backshell to maintain shielding of the signal conductors. Care must be taken to select designs that are appropriate for use with the screw-latching method specified.

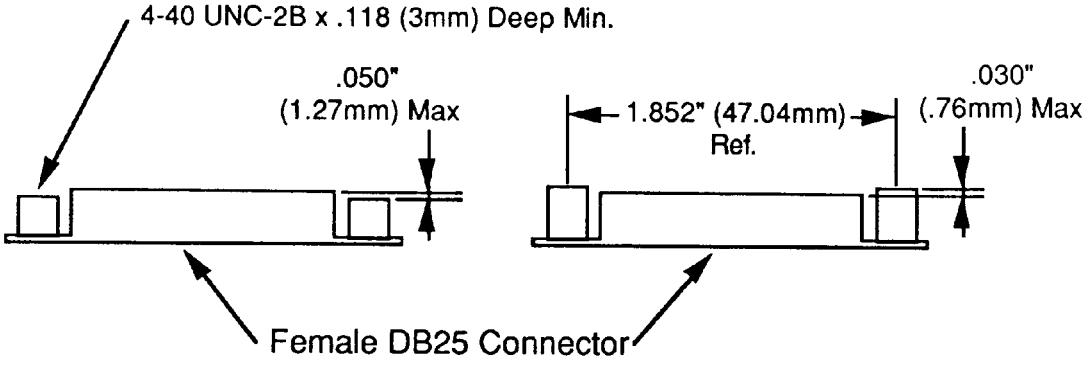


Figure B.1 – Female screw lock mounting

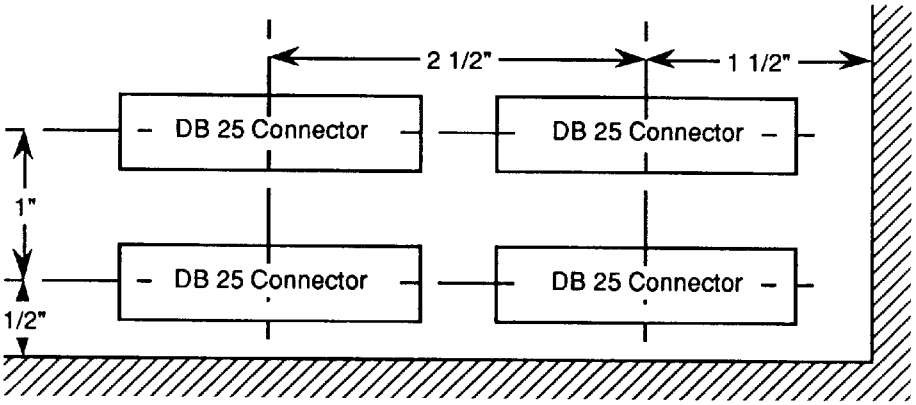


Figure B.2 – Minimum connector spacing

Annex C (informative)
Cable shield pin

The cable shield (pin 13) is for the purpose of controlling electromagnetic radiation from the cable. It is recommended that pin 13 provide high-frequency continuity to the chassis ground at both ends and, in addition, provide DC continuity to the chassis ground at the transmit end.

Annex D (informative)
Connector orientation

Vertical or horizontal mounting: Contact 1 uppermost.

Annex E (informative)
Monochrome operation

Monochrome operation at a 29.97-Hz frame rate can be achieved by transmitting the same values on the three primary channels (G, B, R) on GBR signals or by setting the color-difference signals (C_B, C_R) to zero (200_h) on Y, C_B, C_R signals.

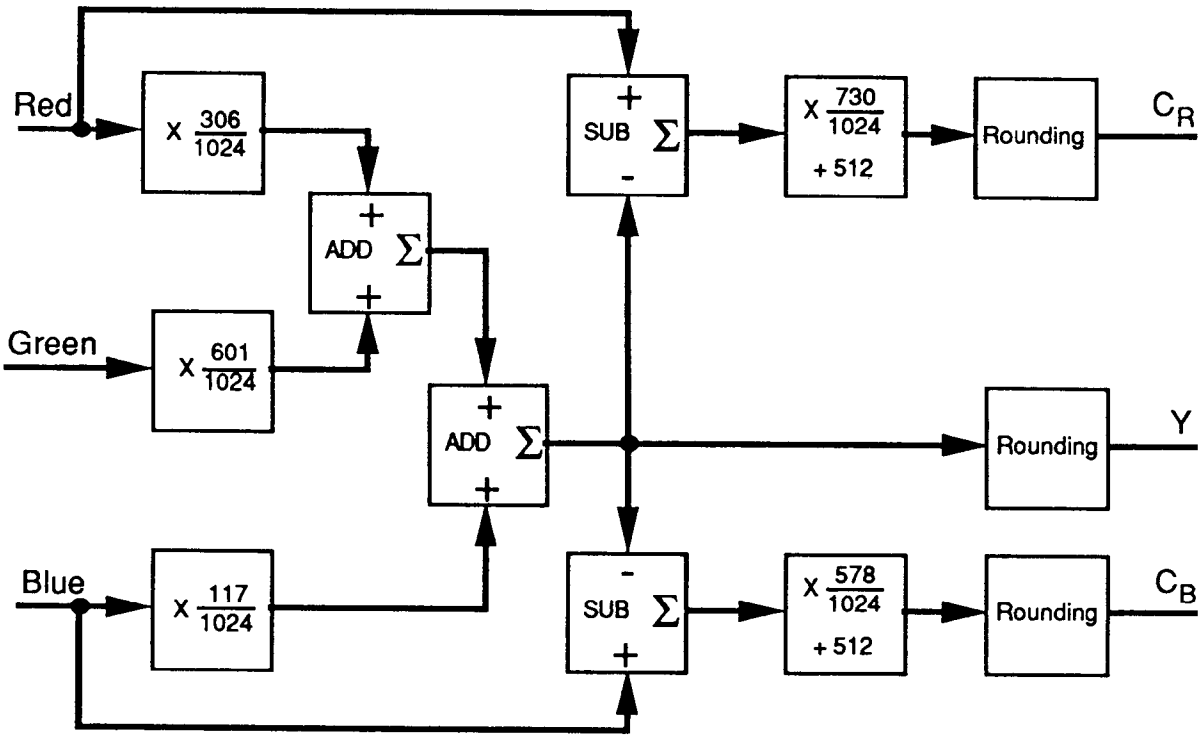
Annex F (informative)
Error detection and correction in the video timing reference signal

Table F.1 enables single-bit errors in the fourth bytes of EAV and SAV to be corrected. Double errors and some multiple-bit errors are detected, but not corrected. The table gives corrected values for bits 8, 7, 6, and 5, where possible. Multiple errors are denoted by asterisks.

Table F.1 -- Error correction table

Received P4 - P0	Received bits 8, 7, 6 & 5 (F, V, H & S)															
	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
00000	0000	0000	0000	*	0000	*	*	0111	0000	*	*	1011	*	1101	1110	*
00001	0000	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*
00010	0000	*	*	1011	*	0101	0110	*	*	1011	1011	1011	1100	*	*	1011
00011	*	*	*	*	*	*	*	*	*	*	*	1011	*	*	*	*
00100	0000	*	*	0111	*	0111	0111	0111	*	1001	1010	*	1100	*	*	0111
00101	*	*	*	*	*	*	*	0111	*	*	*	*	*	*	*	*
00110	*	0001	0010	*	1100	*	*	0111	1100	*	*	1011	1100	1100	1100	*
00111	*	*	*	*	*	*	*	*	*	*	*	*	1100	*	*	*
01000	0000	*	*	0011	*	1101	0110	*	*	1101	1010	*	1101	1101	*	1011
01001	*	*	*	*	*	*	*	*	*	*	*	*	*	1101	*	*
01010	*	0001	0110	*	0110	*	0110	0110	1000	*	*	1011	*	1101	0110	*
01011	*	*	*	*	*	*	0110	*	*	*	*	*	*	*	*	*
01100	*	0001	1010	*	0100	*	*	0111	1010	*	1010	1010	*	1101	1010	*
01101	*	*	*	*	*	*	*	*	*	*	1010	*	*	*	*	*
01110	0001	0001	*	0001	*	0001	0110	*	*	0001	1010	*	1100	*	*	1111
01111	*	0001	*	*	*	*	*	*	*	*	*	*	*	*	*	*
10000	0000	*	*	0011	*	0101	1110	*	*	1001	1110	*	1110	*	1110	1110
10001	*	*	*	*	*	*	*	*	*	*	*	*	*	*	1110	*
10010	*	0101	0010	*	0101	0101	*	0101	1000	*	*	1011	*	0101	1110	*
10011	*	*	*	*	*	0101	*	*	*	*	*	*	*	*	*	*
10100	*	1001	0010	*	0100	*	*	0111	1001	1001	*	1001	*	1001	1110	*
10101	*	*	*	*	*	*	*	*	*	1001	*	*	*	*	*	*
10110	0010	*	0010	0010	*	0101	0010	*	*	1001	0010	*	1100	*	*	1111
10111	*	*	0010	*	*	*	*	*	*	*	*	*	*	*	*	*
11000	*	0011	0011	0011	0100	*	*	0011	1000	*	*	0011	*	1101	1110	*
11001	*	*	*	0011	*	*	*	*	*	*	*	*	*	*	*	*
11010	1000	*	*	0011	*	0101	0110	*	1000	1000	1000	*	1000	*	*	1111
11011	*	*	*	*	*	*	*	*	1000	*	*	*	*	*	*	*
11100	0100	*	*	0011	0100	0100	0100	*	*	1001	1010	*	0100	*	*	1111
11101	*	*	*	*	0100	*	*	*	*	*	*	*	*	*	*	*
11110	*	0001	0010	*	0100	*	*	1111	1000	*	*	1111	*	1111	1111	1111
11111	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	1111

Annex G (informative)
Signal conversion (GBR to Y, C_B, C_R and inverse)



$\frac{306}{1024} = 0.299$

$\frac{601}{1024} = 0.587$

$\frac{117}{1024} = 0.114$

$\frac{730}{1024} = 0.713$

$\frac{578}{1024} = 0.564$

Figure G.1 – Matrix GBR / Y, C_B, C_R

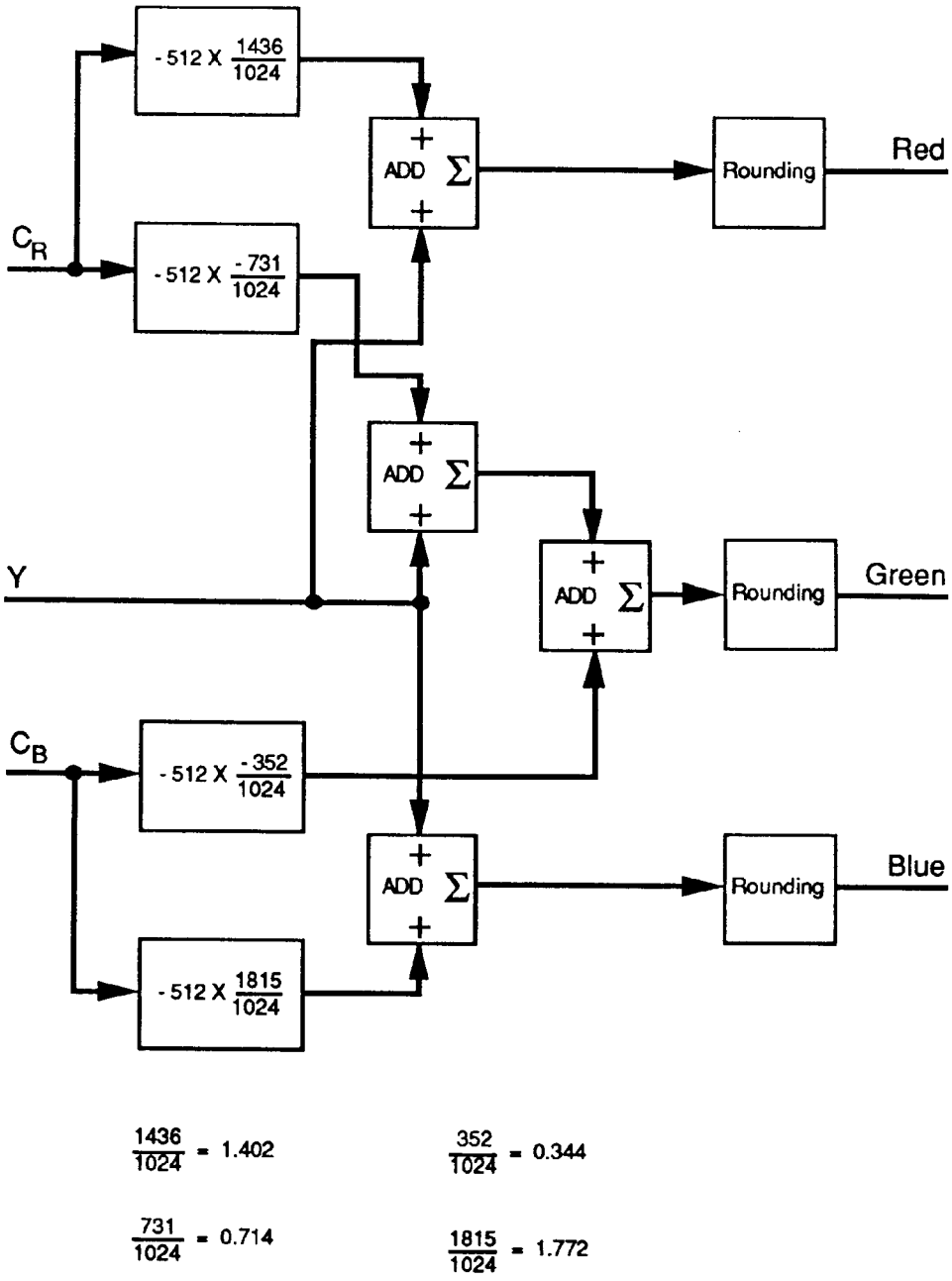


Figure G.2 – Matrix Y, C_B, C_R / GBR

Annex H (informative)
Bibliography

MIL-C-24308C, General Specifications for Connectors, Electric, Rectangular, Nonenvironmental, Miniature, Polarized Shell, Rack and Panel

CCIR Recommendation 601-2, Encoding Parameters of Digital Television for Studios

CCIR Report 962-1, The Filtering, Sampling and Multiplexing for Digital Encoding of Colour Television Signals

Documents are in preparation to cover auxiliary signals (HANC, VANC, DVITC, and video index), but are not yet available.