RP 178-2004
Revision of RP 178-1996

SMPTE RECOMMENDED PRACTICE

Serial Digital Interface Checkfield for 10-Bit 4:2:2 Component and 4fsc Composite Digital Signals

1 Scope

This practice specifies digital test signals suitable for evaluating the low-frequency response of equipment handling serial digital video signals as defined by ANSI/SMPTE 259M. These test signals are fully valid digital component video as defined in ANSI/SMPTE 125M. They are also useful digital composite video signals suitable for testing serial equipment in an out-of-service mode. Although a range of signals will produce the desired low-frequency effects, two specific signals are defined to test cable equalization and phase locked loop (PLL) lock-in, respectively.

2 Normative references

The following standards contain provisions which, through reference in this text, constitute provisions of this practice. At the time of publication, the editions indicated were valid. All standards are subject to revision, and parties to agreements based on this practice are encouraged to investigate the possibility of applying the most recent edition of the standards indicated below.

ANSI/SMPTE 125M-1995, Television — Component Video Signal 4:2:2 — Bit-Parallel Digital Interface

ANSI/SMPTE 259M-1997, Television — 10-Bit 4:2:2 Component and 4fsc NTSC Composite Digital Signals — Serial Digital Interface

SMPTE 244M-2003, Television — System M/NTSC Composite Video Signals — Bit-Parallel Digital Interface

3 General considerations

Stressing of the automatic equalizer is accomplished by using a signal with the maximum number of 1s or 0s with infrequent single clock periods with the other polarity. Stressing of the phase locked loop is accomplished by using a signal with a maximum low-frequency content; that is, with maximum time between transitions.

3.1 Channel coding of the serial digital signal defined by ANSI/SMPTE 259M utilizes scrambling and encoding into NRZI (non-return to zero inverted) accomplished by a concatenation of the following two functions:

$$G_1(X) = X^9 + X^4 + 1 \qquad G_2(X) = X + 1$$

As a result of the channel coding, long runs of 0s in the $G_2(X)$ output data can be obtained when the scrambler, $G_1(X)$, is in a certain state at the time when specific data words arrive. That certain state will be present on a regular basis; therefore, continuous application of the specific data words will regularly produce the low-frequency effects (see annex A).

3.2 Although the longest run of parallel data 0s will occur during the EAV/SAV for component signals and the TRS-ID for composite signals, the probability of coincidence with the required scrambler state to permit either stressing condition to occur is small. The amount of low-frequency effect is so time limited that equalizers and phase locked loops are not maximally stressed.

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3.3 In the data portions of digital video signals (that is, all samples except the EAV, SAV, and ANC data flags), the sample values are restricted to exclude data levels 0 to 3 and 1020 to 1023 (000_h to 003_h and $3FC_h$ to $3FF_h$ in the hexadecimal representation). The result of this restriction is that the longest run of 0s, at the input to the scrambler is 16, occurring when a sample of value 200_h is followed by a sample of value between 004_h and 007_h. This situation can produce up to 26 0s at the encoder output which is also not a maximally stressed case.

3.4 Other specific data words in combination with specific scrambler states can produce a repetitive low-frequency serial output signal until the next EAV or TRS-ID is received to change the state of the scrambler. It is these combinations of data words that form the basis for the test signals defined by this practice.

3.5 Because of the Y/C interleaved nature of the component digital signal, it is possible to obtain nearly all combinations of sample word pairs by defining a particular flat color field in a noise-free environment. It is such sample word pairs which will produce the desired low-frequency effect. Because of the non-interleaved nature of the composite digital signal, such pairs will produce a square wave at one-half the clock frequency which is not a valid signal, but may be used for out-of-service testing.

4 Checkfield data

4.1 Receiver equalizer testing is accomplished by producing a serial digital signal with maximum dc content. Applying the sequence 300_h, 198_h continuously during the active line will produce a signal of 19 high (low) states followed by 1 low (high) state in a repetitive manner once the scrambler attains the required starting condition. Either polarity of the signal will be obtained depending on whether the 19 bits are high or low. By producing at least one-half field of such active lines, the required starting condition, and hence desired signal, will be produced on several lines.

4.2 Since an ITU-R BT.601color black frame has an even number of 1s with no other data present, the polarity of the equalizer stress signal would be the same on each occurrence. The stressing sequence also has an even number of 1s in each word. Therefore, in component systems, it is necessary to add an odd number of 1s to each frame. For the equalizer test signal defined in this practice, the last active sample in line 20 for 525-line systems and the last sample in line 23 for 625-line systems should be 80_h instead of the 198_h which would otherwise be present. Designers are cautioned to ensure there is an odd number of 1s in a majority of frames if other data has been added to the signal in order to ensure both polarities of the test signal are produced.

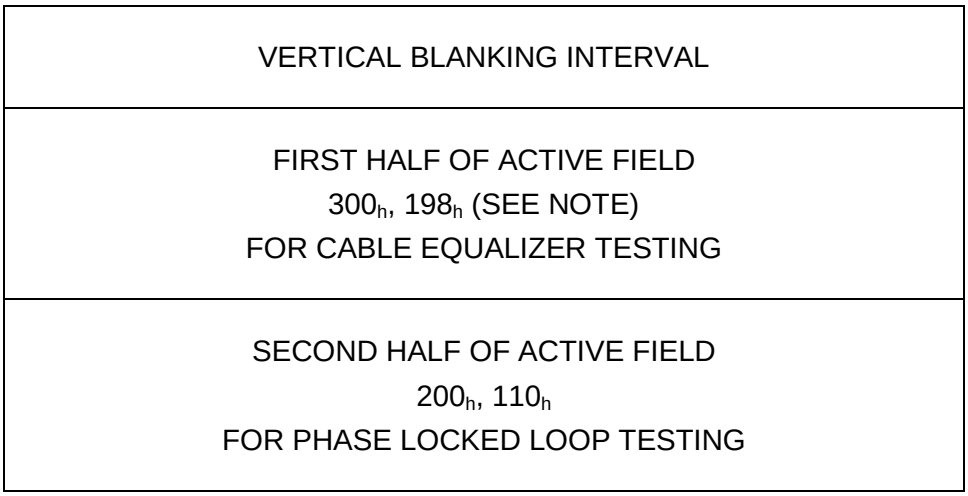
4.3 Receiver phase locked loop testing is accomplished by producing a serial digital signal with maximum low-frequency content and minimum number of zero crossings. Applying the sequence 200_h, 110_h continuously during the active line will produce a signal of 20 high (low) states followed by 20 low (high) states in a repetitive manner once the scrambler attains the required starting condition. By producing at least one-half field of such active lines, the required starting condition, hence desired signal, will be produced on several lines.

4.4 The signals defined in 4.1 and 4.2 are valid component digital signals as defined by ANSI/SMPTE 125M due to the interleaved nature of component digital signals. The same values (except for the single 80_h of 4.2) are used for composite digital testing of systems using the serial form of SMPTE 244M; however, the signals are not valid as they represent a square wave at one-half the clock frequency. There are sequences which represent a small amplitude signal for composite digital which could be considered valid by virtue of their amplitude being more than 20 dB below video peak signal level. However, such signals have an average value more negative than blanking level which could disturb some systems under test. Therefore, for convenience of generation and ease of test operation, the composite digital test signals are chosen to be the same as the component digital test signals.

5 Serial digital interface (SDI) checkfield

5.1 Distribution of data in the SDI check field is shown in figure 1 for the signal standards referenced in clause 2. Specific distribution of sample values are shown in tables 1, 2, 3, and 4 for component 525/625 and composite 525/625, respectively. In each field, the line where the signal changes from one test signal to the other is defined as a range rather than a specific line.

NOTE – The alternate distribution of sample values (that is, interchanging the Y values with the C_b/C_r values) produces the same test signal result in the serial digital signal. Use of the alternate distribution is in compliance with this recommendation and may be preferred in some applications as picture disturbances are more visible in the resulting green display colors.



NOTE – For component signals, the last sample in the first active line of the first field is 80_h (see 4.2).

Figure 1 – Serial digital interface checkfield

Table 1 – 525-component SDI checkfield sample values

Line number	Word numbers	Sample	Word value
20, 283	0 ... 1436 1 ... 1437 2 ... 1438 4 ... 1439 : : :	C_b Y C_r Y	300_h 198_h 300_h 198_h
140 to 148 400 to 408 (approx mid-field)	0 ... 1436 1 ... 1437 2 ... 1438 4 ... 1439 : : :	C_b Y C_r Y	200_h 110_h 200_h 110_h
263, 525	0 ... 1436 1 ... 1437 2 ... 1438 4 ... 1439	C_b Y C_r Y	200_h 110_h 200_h 110_h
NOTE – Sample 1439 in line 20 is 80_h (see 4.2).			

Table 2 – 625-components SDI checkfield sample values

Line number	Word numbers	Sample	Word value
23, 336	C_B0 ... C_B359 Y 1 ... Y 718 C_R0 ... C_R359 Y 2 ... Y 719 : : :	C_b Y C_r Y	300_h 198_h 300_h 198_h
160 to 168 470 to 478 (approx mid-field)	C_B0 ... C_B359 Y 1 ... Y 718 C_R0 ... C_R359 Y 2 ... Y 719 : : :	C_b Y C_r Y	200_h 110_h 200_h 110_h
310, 623	C_B0 ... C_B359 Y 1 ... Y 718 C_R0 ... C_R359 Y 2 ... Y 719	C_b Y C_r Y	200_h 110_h 200_h 110_h
NOTE – Sample Y 719 in line 23 is 80_h (see 4.2).			

Table 3 – 525-compisute SDI checkfield sample values

Line number	Word numbers	Word value
21, 284	0 ... 764 1 ... 765 2 ... 766 4 ... 767 : : :	300_h 198_h 300_h 198_h
140 to 148 400 to 408 (approx mid-field)	0 ... 764 1 ... 765 2 ... 766 4 ... 767 : : :	200_h 110_h 200_h 110_h
262, 525	0 ... 764 1 ... 765 2 ... 766 4 ... 767	200_h 110_h 200_h 110_h

Table 4 – 625-composite SDI checkfield sample values

Line number	Word numbers	Word value
23, 336	0 ... 944 1 ... 945 2 ... 946 4 ... 947 : : :	300_h 198_h 300_h 198_h
160 to 168 470 to 478 (approx mid-field)	0 ... 944 1 ... 945 2 ... 946 4 ... 947 : : :	200_h 110_h 200_h 110_h
310, 623	0 ... 944 1 ... 945 2 ... 946 4 ... 947	200_h 110_h 200_h 110_h

Annex A (informative)
Bibliography

ITU-R BT.601-5 (10/95), Studio Encoding Parameters of Digital Television for Standard 4:3 and Wide-Screen 16:9 Aspect Ratios

Eguchi, Takeo. Pathological check codes for serial digital interface systems. SMPTE Journal 101(8): 553-558; August 1992.