RP 184-2004
Revision of RP 184-1996

SMPTE RECOMMENDED PRACTICE

Specification of Jitter in Bit-Serial Digital Systems

1 Scope

This practice describes techniques for specifying jitter in self-clocking, bit-serial digital systems. It is applicable to sources, receivers, and regenerators. It is specifically intended for, but not limited to, ANSI/SMPTE 259M serial systems. Methods for measuring these specifications are found in SMPTE RP 192.

2 Normative references

The following standards contain provisions which, through reference in this text, constitute provisions of this practice. At the time of publication, the editions indicated were valid. All standards are subject to revision, and parties to agreements based on this practice are encouraged to investigate the possibility of applying the most recent edition of the standards indicated below.

ANSI/SMPTE 259M-1997, Television — 10-Bit 4:2:2 Component and $4f_{sc}$ Composite Digital Signals — Serial Digital Interface

SMPTE RP 192-2003, Jitter Measurement Procedures in Bit-Serial Digital Interfaces

3 Definitions

3.1 alignment jitter: The variation in position of a signal's transitions relative to those of a clock extracted from that signal. The bandwidth of the clock extraction process determines the low-frequency limit for alignment jitter.

3.2 input jitter tolerance: Peak-to-peak amplitude of sinusoidal jitter that, when applied to an equipment input, causes a specified degradation of error performance.

3.3 intrinsic jitter: Jitter at an equipment output in the absence of input jitter.

3.4 jitter: The variation of a digital signal's transitions from their ideal positions in time.

3.5 jitter transfer: Jitter on the output of equipment resulting from applied input jitter.

3.6 jitter transfer function: Ratio of the output jitter to the applied input jitter as a function of frequency.

3.7 output jitter: Jitter at the output of equipment that is embedded in a system or network. It consists of intrinsic jitter and the jitter transfer of jitter at the equipment input.

3.8 timing jitter: The variation in position of a signal's transitions occurring at a rate greater than a specified frequency, typically 10 Hz or less. Variations occurring below this specified frequency are termed wander and are not addressed by this practice.

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3.9 unit interval (UI): Abbreviated UI, it is the period of one clock cycle. It corresponds to the nominal minimum time between transitions of the serial signal.

4 Jitter specifications

Equipment jitter specifications fall into three categories: input jitter tolerance, jitter transfer, and intrinsic jitter. A fourth specification, output jitter, is a network specification and may be used to specify jitter limits at equipment interfaces.

4.1 Input jitter tolerance

Input jitter tolerance is the peak-to-peak amplitude of sinusoidal jitter that, when applied to an equipment input, causes a specified degradation of error performance. Input jitter tolerance is applicable to most serial inputs.

4.1.1 Input jitter tolerance requirements are specified with a jitter template that covers a specified sinusoidal amplitude/frequency region (see figure 1). This template represents the minimum amount of jitter that the equipment must accept without causing the specified degradation of error performance. Equipment meeting a jitter tolerance requirement must have an actual jitter tolerance greater than the requirement (see figure 2).

4.1.2 Input jitter tolerance requirements are specified with the parameters given in table 1.

4.1.2.1 Frequency band f1 to f2 forms the low-frequency jitter tolerance bandpass. At least A1 UI of peak-to-peak sinusoidal jitter shall be tolerated over this bandpass without exceeding the specified error criterion.

4.1.2.2 Frequency band f3 to f4 forms the high-frequency jitter tolerance bandpass. At least A2 UI of peak-to-peak sinusoidal jitter shall be tolerated over this bandpass without exceeding the specified error criterion.

4.1.2.3 A1 and A2 shall be specified in UI.

4.1.2.4 The slope of the jitter tolerance requirement between f2 and f3 shall be 20 dB/decade. Frequencies f2 and f3 are related as follows: F2 = f3/(A1/A2).

4.1.2.5 The criterion for reaching the onset of errors shall be specified. Either a BER limit or a maximum number of errored seconds over a specified measurement interval should be used.

4.1.2.6 The test signal used for the measurement (to which sinusoidal jitter is added) shall be specified.

4.1.3 Numerical input jitter tolerance values are provided in the appropriate SMPTE standards which reference this practice. The terminology shall comply with 4.1.2.

Table 1 – Input jitter tolerance

Parameters	Units	Description
Data rate	(bits/s)	(Serial bit rate)
f1	(Hz)	(Low-frequency specification limit)
f2	(Hz)	(Upper band edge for A1, low-frequency jitter tolerance)
f3	(Hz)	(Upper band edge for A2, high-frequency jitter tolerance)
f4	(Hz)	(High-frequency specification limit)
A1	(UI)	(Low-frequency jitter tolerance, f1 to f2)
A2	(UI)	(High-frequency jitter tolerance, f3 to f4)
Error criterion		(Criterion for onset of errors)
Test signal		(Test signal used for measurement)

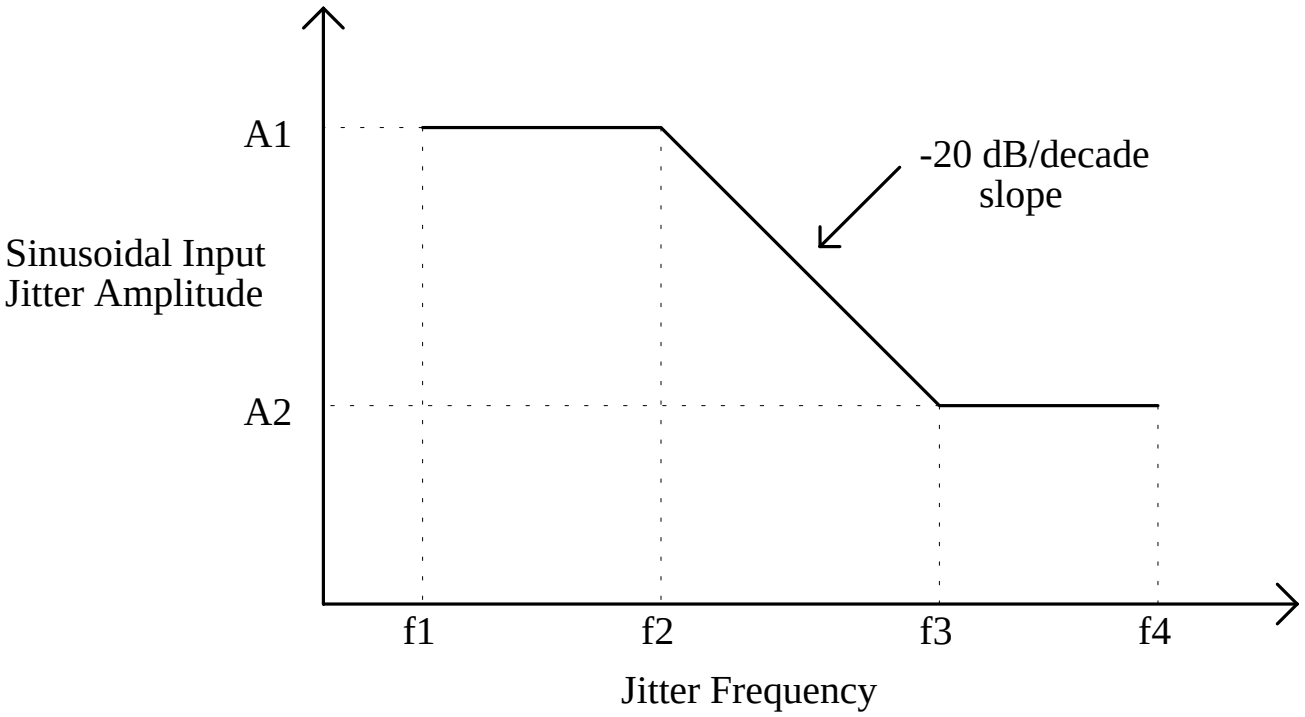

Figure 1 – Input jitter tolerance template

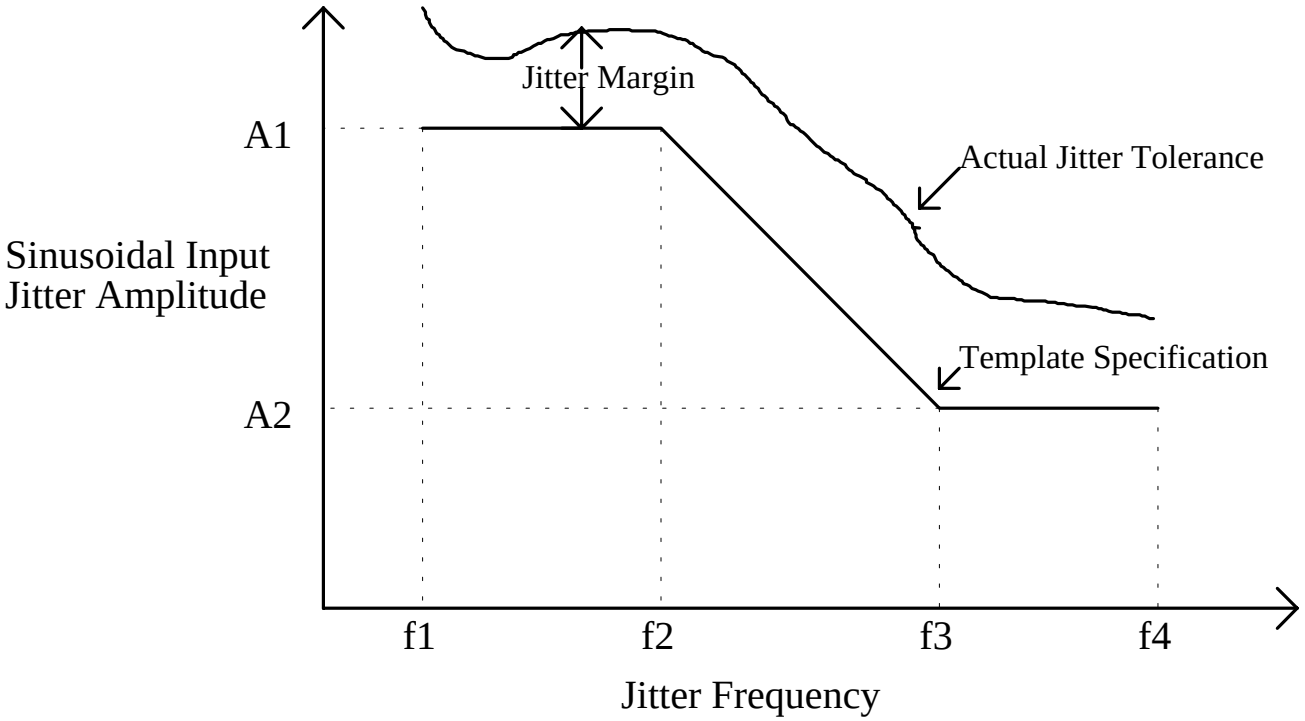

Figure 2 – Jitter tolerance specification and a compliant jitter tolerance

4.2 Jitter transfer

Jitter transfer is jitter on the output of equipment resulting from applied input jitter. Jitter transfer is applicable to a device which produces a serial output from a serial input, such as a regenerator.

Jitter transfer can also occur from reference signals applied to equipment, such as analog black burst. The jitter transfer templates described below are intended for serial input to serial output jitter transfer.

4.2.1 Jitter transfer requirements are specified with a template showing the maximum jitter gain as a function of frequency (see figure 3). Equipment meeting a jitter transfer requirement will have a jitter transfer function that lies within this template (see figure 4).

4.2.2 Jitter transfer requirements are specified with the parameters given in table 2.

4.2.2.1 Frequency band f1 to fc forms the jitter transfer bandpass. The maximum jitter gain over this bandpass shall be P.

4.2.2.2 From frequency fc to at least 10 (fc), the jitter transfer template shall decrease at 20 dB/decade.

4.2.2.3 P shall be specified in decibels.

4.2.2.4 The test signal used for the measurement (to which sinusoidal jitter is added) shall be specified.

4.2.3 Numerical jitter transfer values are provided in the appropriate SMPTE standards which reference this practice. The terminology shall comply with 4.2.2.

4.3 Intrinsic jitter and output jitter

Intrinsic jitter and output jitter are both measurements of jitter at an equipment output. They differ in the specification of the input signal to the equipment. Except for this, they are measured identically.

Intrinsic jitter is defined as the amount of jitter at an equipment output when a jitter-free input signal is applied. It is a measure of the amount of jitter generated in the equipment, independent of any jitter transfer. Intrinsic jitter applies to most serial outputs.

Output jitter is the amount of jitter at the output of equipment that is embedded in a system or network. It consists of intrinsic jitter and the jitter transfer of jitter at the equipment input. Output jitter is a network specification, not an equipment specification. Individual equipment should be specified in terms of intrinsic jitter, jitter transfer, and input jitter tolerance. Network interface specifications may use output jitter.

4.3.1 Intrinsic and output jitter shall be specified as peak-to-peak quantities and measured over defined jitter frequency bands. Two measurement bands are specified, one is a subset of the other (see figure 5).

4.3.2 Intrinsic and output jitter shall be specified with the parameters given in table 3.

4.3.2.1 The timing jitter measurement bandpass is formed by f1 to f4. The maximum peak-to-peak jitter allowed over this bandpass is specified as A1.

4.3.2.2 The alignment jitter measurement bandpass is formed by f3 to f4. The maximum peak-to-peak jitter allowed over this bandpass is specified as A2.

4.3.2.3 A1 and A2 shall be specified in unit intervals.

4.3.2.4 Bandpass slopes shall be at least 20 dB/decade and have a mimimum phase response unless otherwise specified. Stop band rejection shall be at least 20 dB. Pass band ripple shall be less than ± 1 dB.

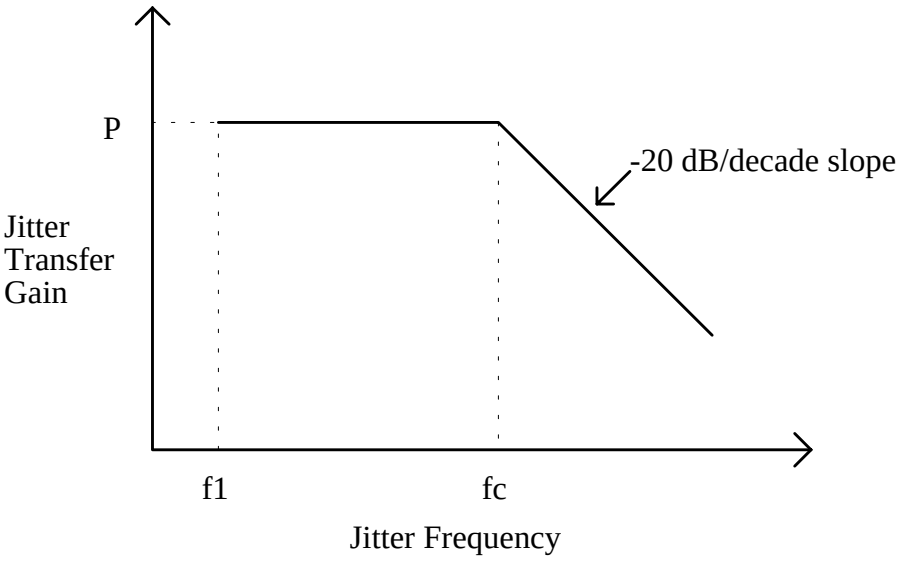

Figure 3 – Jitter transfer template

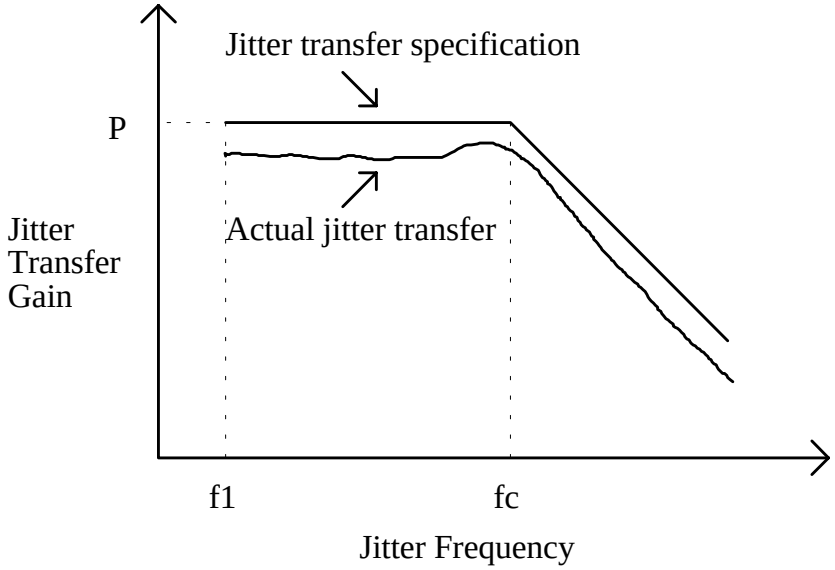

Figure 4 – Jitter transfer specification and a compliant jitter transfer function

Table 2 – Jitter transfer requirements

Parameters	Units	Description
Data rate	(bits/s)	(Serial bit rate)
f1	(Hz)	(Low-frequency specification limit)
fc	(Hz)	(Upper band edge of jitter transfer bandpass)
P	(dB)	(Maximum jitter gain, f1 to fc)
Test signal		(Test signal used for measurement)

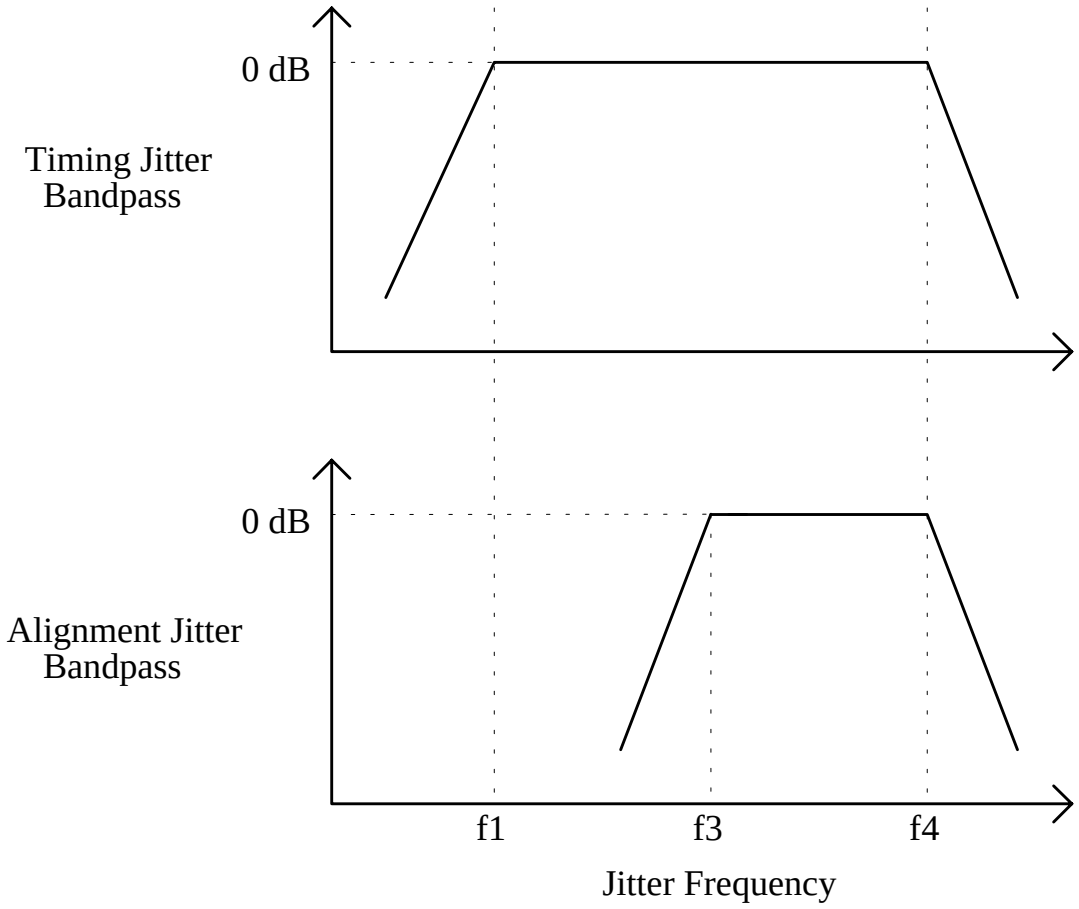

Figure 5 – Intrinsic and output jitter measurement bandpasses

Table 3 – Intrinsic and output jitter

Parameters	Units	Description
Data rate	(bits/s)	(Serial bit rate)
f1	(Hz)	(Timing jitter, lower band edge)
f3	(Hz)	(Alignment jitter, lower band edge)
f4	(Hz)	(Upper band edge)
A1	(UI)	(Timing jitter)
A2	(UI)	(Alignment jitter)
t_m	(s)	(Measurement time)
Test signal		(Test signal used for measurement)
n		(Serial clock divider)
NOTE – A previous version of this practice used B1, B2, and B3 in place of f1, f3, and f4, respectively (see annex A).		

4.3.2.5 A measurement time (tm) may be specified. If this is omitted, then the measurement time will be determined by the characteristics of the measurement system such as discussed in SMPTE RP 192.

4.3.2.6 The test signal used for the measurement shall be specified. For an intrinsic jitter measurement, the test source jitter shall be negligible compared to the intrinsic jitter specification.

4.3.2.7 The serial clock divider, "n", used in the clock extractor should be specified (see SMPTE RP 192 for information on the clock extractor and clock extractor based measurement methods). The ratio of the serial clock frequency to the clock extractor frequency is "n." It is meaningful for clock extractor jitter measurement methods, but may not be applicable to other measurement techniques.

4.3.3 Numerical intrinsic and output jitter values are provided in the appropriate SMPTE standards which reference this practice. The terminology shall comply with 4.3.2

Annex A (informative)
Terminology changes from SMPTE RP 184-1995 to RP 184-1996

The 1995 version of SMPTE RP 184 described specification of output jitter in 3.2. The current version of this practice, in 4.3.2, follows the same specification format, but uses different terminology for the measurement bands. This change was made to follow current jitter specification practice.

The translation of RP 184-1995 to current RP 184 terminology is shown in table A.1. The current RP 184 terminology is preferred and should be used in all new equipment specifications.

Table A.1 – Terminology

Description	RP 184-1995 parameters	Current RP 184 parameters
Timing jitter lower-band edge	B1	f1
Alignment jitter lower-band edge	B2	f3
Upper-band edge	B3	f4