RP 192-2003
Revision of RP 192-1996

SMPTE RECOMMENDED PRACTICE

Jitter Measurement Procedures in Bit-Serial Digital Interfaces

1 Scope

1.1 Scope

This practice describes methods for measuring jitter performance in bit-serial digital interfaces. The techniques are specifically suited for jitter specifications that follow the form described in SMPTE RP 184.

1.2 Introduction

Jitter is one of the most important parameters in the performance of serial digital transmission systems. It can cause errors in the transmission and recovery of digital data, and may degrade analog signal performance if the jitter is transferred through the digital-to-analog conversion process. Characterizing and measuring jitter are important for reliable and predictable serial digital system operation.

2 Normative reference

The following standard contains provisions which, through reference in this text, constitute provisions of this practice. At the time of publication, the edition referenced was valid. All standards are subject to revision, and parties to agreements based on this practice are encouraged to investigate the possibility of applying the most recent edition of the standard indicated below.

SMPTE RP 184-1996, Specification of Jitter in Bit-Serial Digital Systems

3 Definitions

3.1 alignment jitter: Variation in position of a signal's transitions relative to those of a clock extracted from that signal. The bandwidth of the clock extraction process determines the low-frequency limit for alignment jitter.

3.2 clock extractor: A device which is able to extract the serial data clock from a serial data stream, and outputs a clock-related trigger. It may also provide the serial digital data reclocked with the extracted clock.

3.3 DSO: Acronym for digital storage oscilloscope.

3.4 DUT: Acronym for device under test.

3.5 error rate tester: A device that quantifies the error rate of a serial digital signal. Two examples are the classic bit error rate (BER) tester and the field rate CRC method (EDH) described in SMPTE RP 165.

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3.6 input jitter tolerance: Peak-to-peak amplitude of sinusoidal jitter that, when applied to an equipment input, causes a specified degradation of error performance.

3.7 intrinsic jitter: Jitter at an equipment output in the absence of input jitter.

3.8 jitter: Variation of a digital signal's transitions from their ideal positions in time.

3.9 jitter generator: A device which produces a serial digital signal containing sinusoidal jitter of adjustable amplitude and frequency.

3.10 jitter receiver: Demodulates and allows measurement of the jitter present on a serial signal. It commonly provides an output proportional to the demodulated jitter.

3.11 jitter transfer: Jitter on the output of equipment resulting from applied input jitter.

3.12 jitter transfer function: Ratio of the output jitter to the applied input jitter as a function of frequency.

3.13 output jitter: Jitter at the output of equipment that is embedded in a system network. It consists of intrinsic jitter and the jitter transfer of jitter at the equipment input.

3.14 phase demodulator: A device that provides as its output a signal proportional to the phase difference of two input signals.

3.15 SDI: Acronym for serial digital interface, typically referring to an ANSI/SMPTE 259M system.

3.16 timing jitter: Variation in position of a signal's transitions occurring at a rate greater than a specified frequency, typically 10 Hz or less. Variations occurring below this specified frequency are termed wander and are not addressed by this practice.

3.17 unit interval (UI): Abbreviated "UI", it is the period of one clock cycle. It corresponds to the nominal minimum time between transitions of the serial signal.

4 Jitter specification

Four methods are described: The first uses an available reference clock to trigger an oscilloscope; the second uses a clock extractor with defined characteristics to trigger the oscilloscope; the third and fourth are based on a phase demodulator method jitter receiver.

4.1 Oscilloscope measurement by means of triggering on a reference signal

If a reference signal is available, a basic jitter measurement can be done (see figure 1). The oscilloscope is directly triggered by the reference signal. This reference signal could also be a serial digital signal with high stability. The digital data signal is connected to the suitably terminated vertical channel of the oscilloscope and an eye measurement is done. The jitter is typically measured at the eye crossing.

– Presentation of measurement results: The test signal, the jitter amplitude, the parameters of the oscilloscope (bandwidth, etc.), and the measurement time should be indicated.

– Background information: This measurement procedure provides a coarse survey of jitter in an SDI signal. The measurement result depends on the stability of the reference signal (its jitter sets the measurement floor), the type of oscilloscope, and the measurement time (e.g., when a DSO is used in persistence mode). All of these parameters influence the measurement result and contribute to variability in the result as conditions vary. This method does not allow bandwidth restriction as generally required in jitter specification. This method is not recommended if other jitter measurement methods are available.

4.2 Jitter measurement by means of a clock extractor

The jitter in a signal output can be measured by using a device to extract a clock and then trigger an oscilloscope or other indicating device (see figure 2).

4.2.1 Clock extractor block diagram

The clock extractor typically consists of a wideband clock recovery circuit followed by a second, narrow band PLL (see figure 3). This second PLL can be set to two different loop bandwidths, so that two different jitter transfer functions are available (see figure 4). Clock output 2 is used to trigger the indicating device. The clock extractor shall have the following characteristics:

1) It shall be capable of being put in series with the signal output and provide enough signal level for the indicating device. It shall not modify the output signal characteristics in ways that obscure or modify the jitter on the signal.

2) To measure timing jitter (A1), the clock extractor shall have a clock recovery bandwidth of f1. To measure alignment jitter (A2), the clock extractor shall have a clock recovery bandwidth of f3 (see figure 4). The number of integrations within the clock extractor PLL shall be at least two (TYPE II PLL) to provide at least a 40 dB/decade attenuation to wander or low-frequency jitter in the following jitter indication devices of 4.2.2.

NOTE – A three integrator PLL (TYPE III) is preferred providing 60 dB/decade wander attenuation. However, since these are more difficult to design, a Type II is acceptable.

3) The jitter transfer function of the clock extractor shall roll-off at 20 dB/decade or greater and have a minimum phase response unless otherwise specified. Ripple within the pass band shall be less than ± 1 dB (see figure 4).

4) The extracted clock frequency shall be the serial clock frequency divided by n, where n is defined in 4.3.2 of SMPTE RP 184.

5) The clock extractor may have an optional clock output 1, which has a clock recovery bandwidth fcr greater than or equal to f3. It is preferable that fcr equal 14.

4.2.2 Indicating device specifications

The indicating device used to observe the jitter shall have the following characteristics:

1) The horizontal and/or trigger bandwidth of the indicating device shall not attenuate the observed jitter. The trigger bandwidth shall be at least f3.

2) The indicating device shall not create intersymbol interference at the zero-crossing point. This requires a vertical system step response that transitions and settles in less than 1 UI.

3) The indicating device shall acquire sufficient samples so that peak-to-peak jitter can be determined. This requires sampling until the shape of the jitter distribution is known. If the jitter specification includes a measurement time, this shall be the minimum acquisition time. The maximum acquisition time will depend on the device sample rate and the type of jitter distribution. For example, a sinusoidal distribution will typically be determined with fewer samples than will a gaussian-like distribution.

NOTE – The minimum required measurement time depends on how quickly the measurement device collects samples. For digital storage oscilloscopes (DSOs), this is determined by the acquisition rate and the number of samples per acquisition. While the latter term is related to the advertised DSO sample rate, the former is not. DSOs with identical sample rates may take very different amounts of time to build a sufficient sample record to make a measurement.

The minimum measurement for a given oscilloscope may be determined as follows: First, have the scope acquire for a very long time to establish the jitter level. Then, successively shorter measurements are taken until the results start showing unacceptable error or variation. This establishes the minimum measurement time for the scope. Experienced users often have an intuitive feeling for this value based on how the sample distribution is filling in.

4) If the indicating device is an oscilloscope, the jitter measurement is usually made at the eye crossing. A digital storage oscilloscope with infinite persistence is recommended.

4.2.3 Measurement of timing jitter

The clock extractor is set to bandwidth f1. The clock output 2 is connected to the trigger channel of the oscilloscope. The signal connected to the oscilloscope vertical channel depends on the jitter amplitude being measured. For jitter amplitudes less than 1 UI, the loop-through signal is used (see figure 2). For jitter amplitudes greater than 1 UI, two different connections are possible:

1) (Preferred) If the clock extractor has a clock 1 output (figure 3), this signal is applied to the oscilloscope vertical channel (see figure 5). This connection will ensure jitter between frequencies f1 and fcr, where fcr is the bandwidth of the wideband clock recovery circuit.

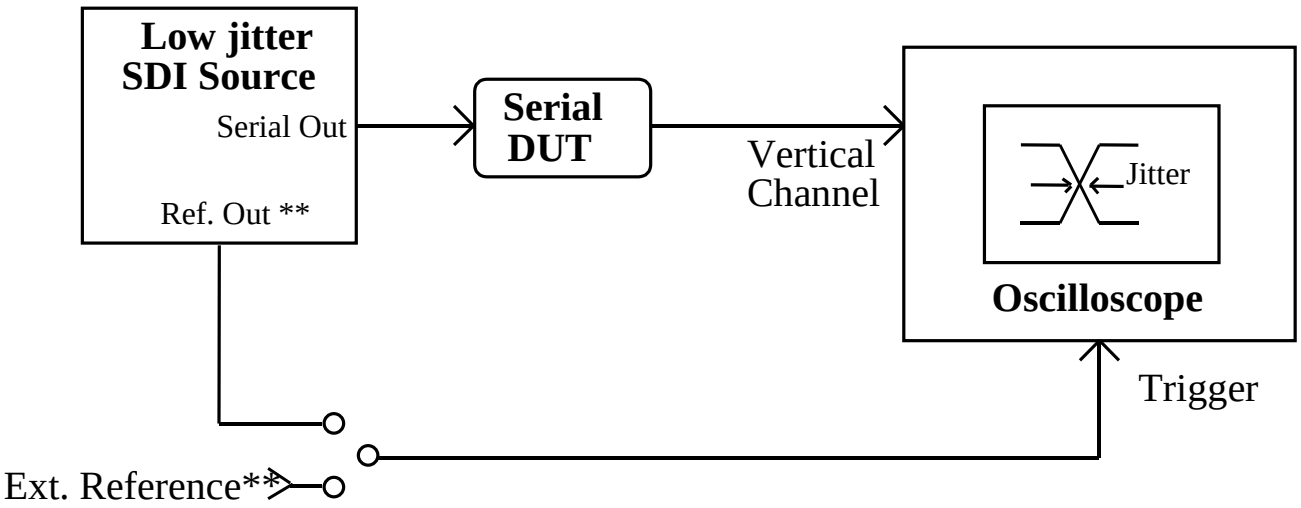
2) If the clock extractor has simultaneous outputs at bandwidths f1 and f3, one output is connected to the vertical channel and the second to the trigger. This connection measures jitter between frequencies f1 and f3.

– Presentation of measurement results: The test signal, the type of oscilloscope, the measurement time, and the jitter amplitude measured at the eye crossing should be documented. A screen plot of the eye pattern is recommended.

4.2.4 Measurement of alignment jitter

The clock extractor is set to bandwidth f3. The clock output 2 is connected to the trigger channel of the oscilloscope. The loop-through signal is connected to the oscilloscope vertical channel (see figure 2).

– Presentation of measurement results: The test signal, the type of oscilloscope, the measurement time, and the jitter amplitude measured at the eye crossing should be documented. A screen plot of the eye pattern is recommended.



**Reference examples for 270 Mb/s SMPTE 259M signal:
(1) 27 MHz parallel clock
(2) 270 MHz serial clock
(3) SMPTE 259M serial signal

Figure 1 – Oscilloscope jitter measurement by means of a reference signal

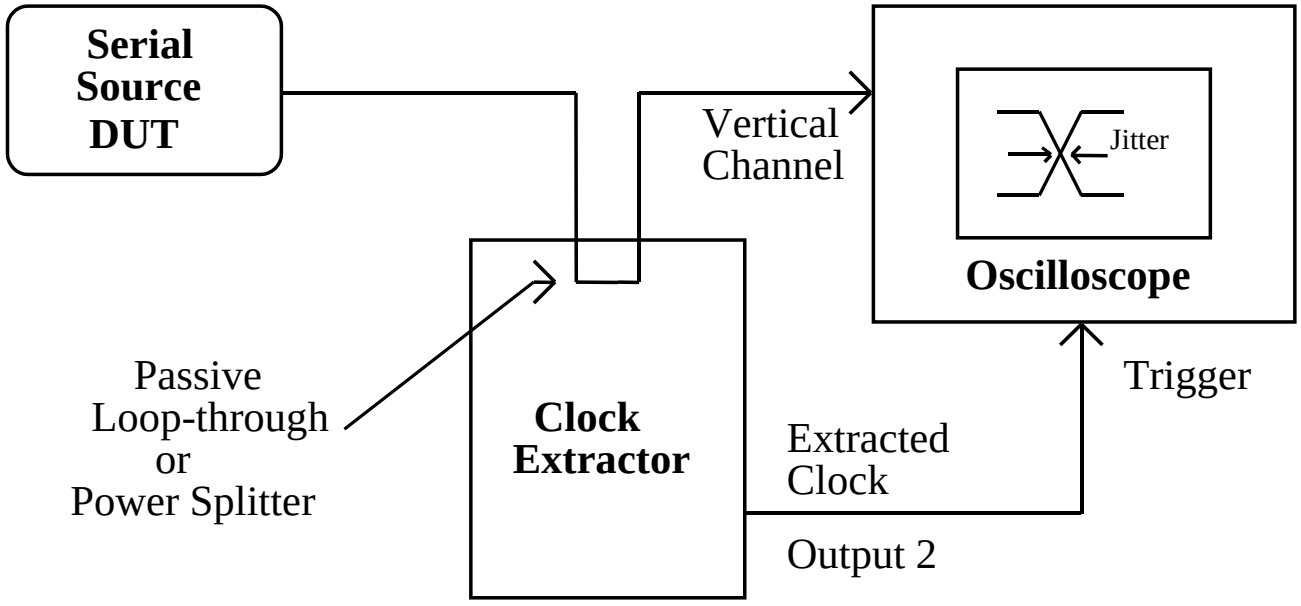


Figure 2 – Jitter measurement less than 1 UI using a clock extractor

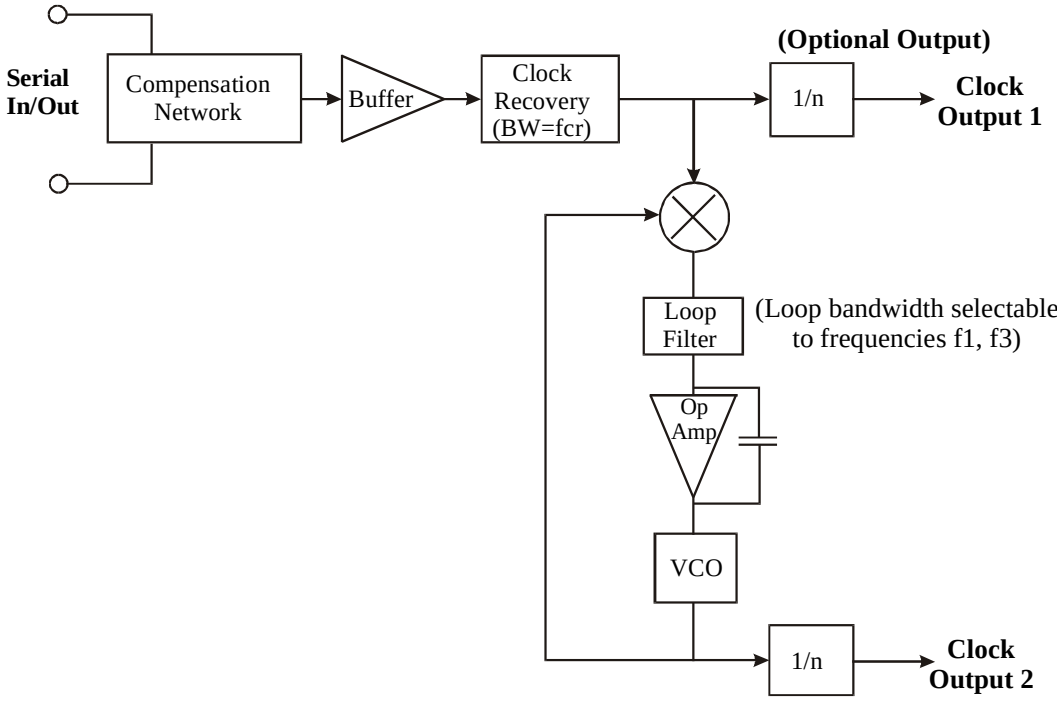


Figure 3 – Clock extractor block diagram

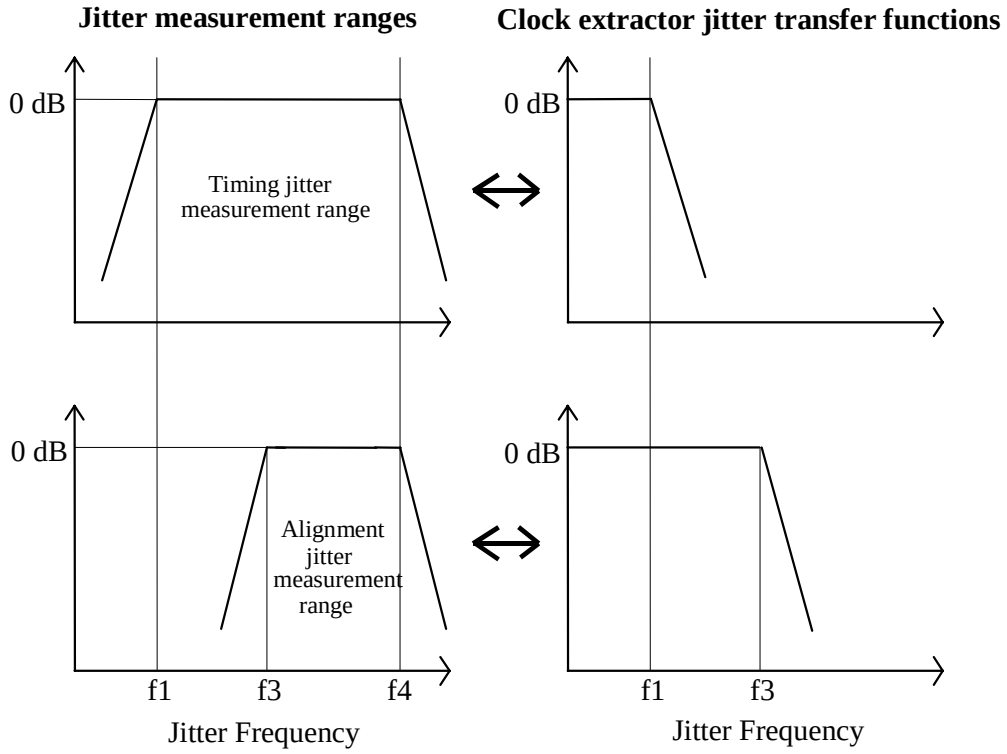


Figure 4 – Jitter measurement bandwidths and corresponding clock extractor jitter transfer function

NOTE – The band-pass slope for f1 and f3 shall be equal to, or greater than, 40 dB/decade.

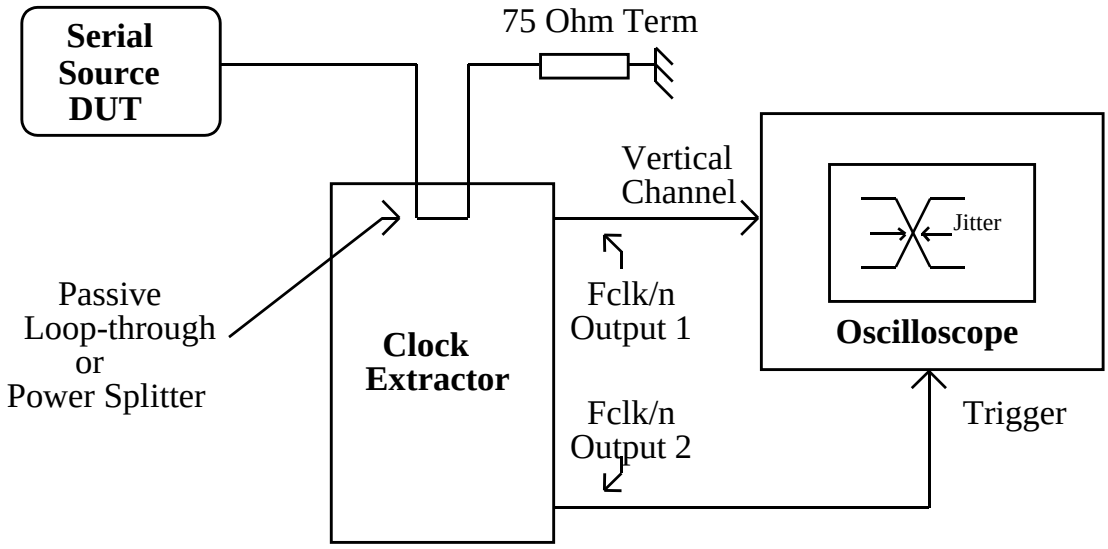


Figure 5 – Measuring jitter greater than 1 UI using a clock extractor and an oscilloscope

4.2.5 Phase noise measurement by means of a clock extractor

This clause describes a simple method for making a phase noise measurement on the extracted clock using a spectrum analyzer. This technique allows an examination of the side bands of the clock signal, which correspond with the jitter frequencies in the SDI signal (see figure 6).

The output 1 of the clock extractor is connected to a spectrum analyzer. The spectrum analyzer is switched to phase noise measurement and the phase noise of the clock under test is examined.

– Presentation of measurement results: The test signal, the clock extractor PLL bandwidth, the resolution bandwidth and span of the spectrum analyzer, and a plot of the spectrum should be indicated.

4.3 Jitter measurements using a phase demodulator

Jitter can be conveniently observed and measured if the phase modulation sidebands are heterodyned down to dc. One popular method is to recover two clocks from the signal, one with a very wide clock recovery bandwidth and the second with a narrow bandwidth, and apply them to a phase demodulator (see figure 7). The output signal is then applied through selectable bandpass filters to a peak reading voltmeter. The output can also be applied to a spectrum analyzer to observe the jitter frequency terms (see figure 8). Jitter receivers typically use the phase demodulator method.

4.3.1 A jitter receiver shall be capable of measuring peak-to-peak jitter over the jitter measurement bandpasses described in 4.3.2 of SMPTE RP 184.

4.3.2 The jitter spectrum can be observed by connecting the phase demodulator output to a spectrum analyzer or an oscilloscope with fast Fourier transform (FFT) option (see figure 8).

– Presentation of measurement results: The test signal, measurement time, measured jitter level and measurement bandpass, and a description of the measurement equipment should be documented.

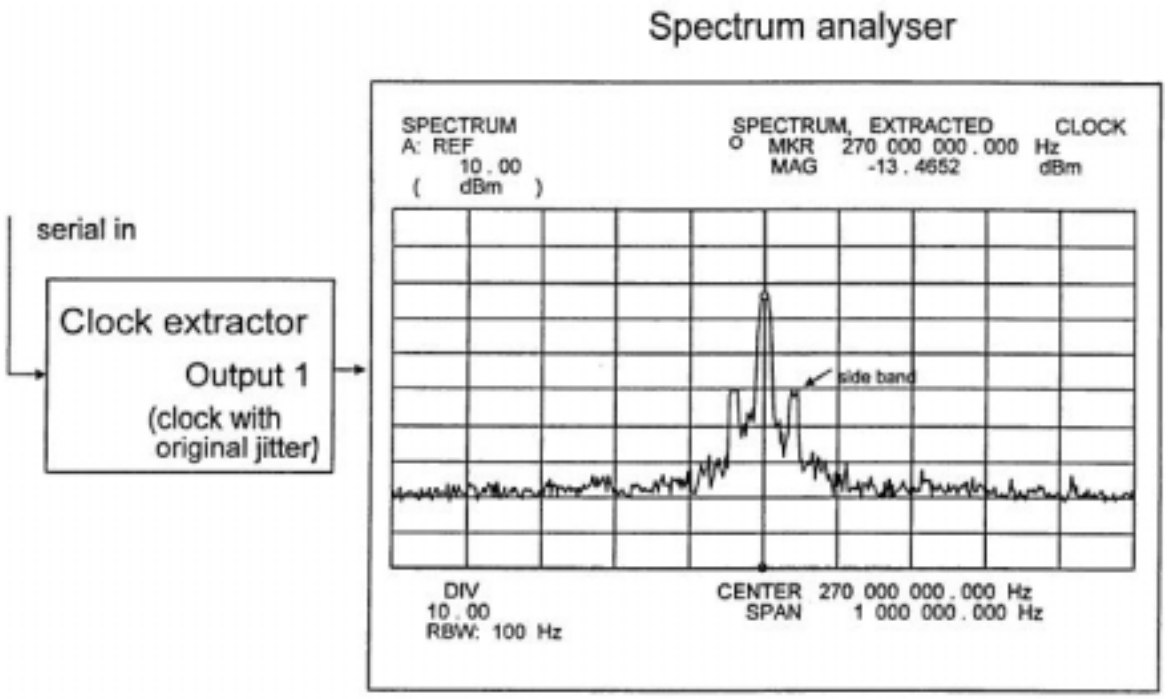


Figure 6 – Jitter measurement by means of a clock extractor and a spectrum analyzer

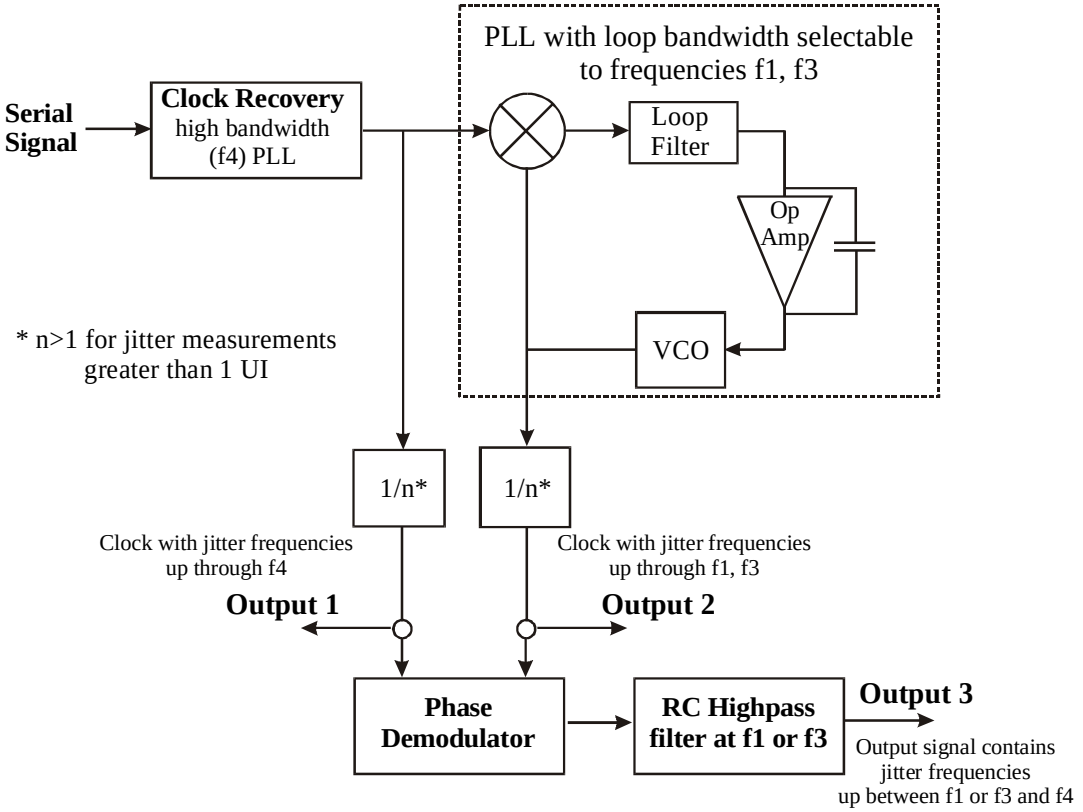


Figure 7 – Block diagram of a jitter receiver (clock extractor, high-quality PLL, demodulator)

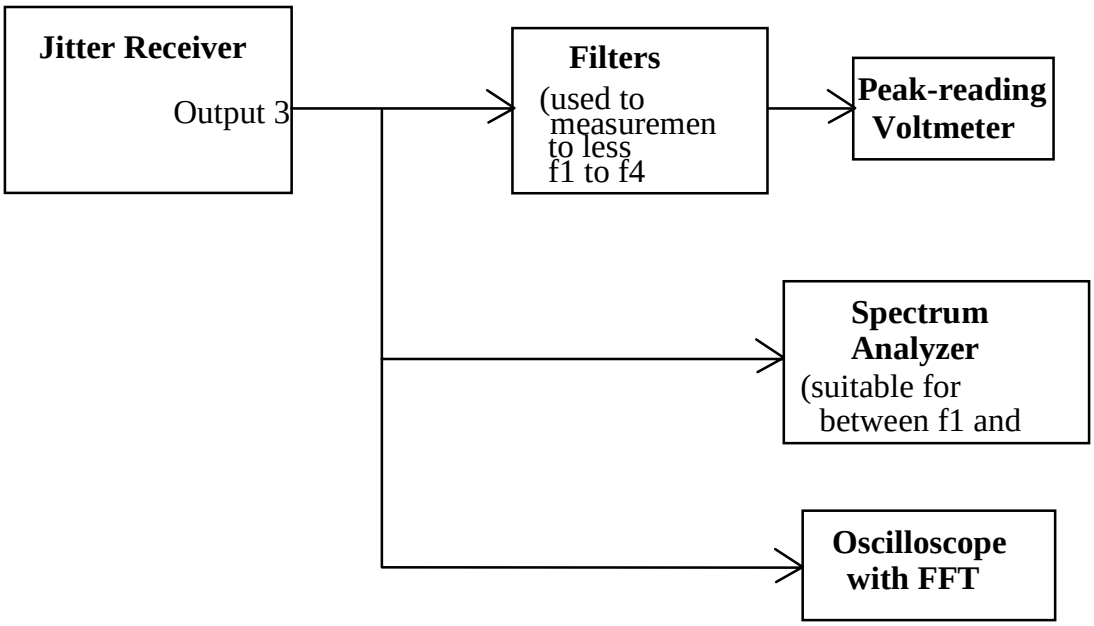


Figure 8 – Jitter receiver output connections

4.4 Phase demodulator measurement with an available reference signal

If a reference signal is available, then a demodulated jitter measurement may be made using the set-up shown in figure 9. The reference and data signals are connected to the two inputs of a digital phase demodulator. The output of the demodulator may be processed in several ways. The output may be filtered to establish the lower and upper band edges and then passed to an oscilloscope for display of the jitter results (note that the vertical scale of the oscilloscope now represents the jitter amplitude). Alternatively, the demodulated jitter waveform may be captured and then digitally filtered to establish the upper and lower band edges. Finally, the jitter spectrum may be obtained either by performing an FFT on a captured waveform, or by connecting the demodulator output to a spectrum analyzer.

– Presentation of measurement results: The test signal type, the upper and lower band edges, the measurement time, and the peak-to-peak jitter amplitude should be recorded.

– Background information: This measurement method is sensitive to any pattern dependent jitter introduced by the phase detector in the jitter demodulator. The phase detector shall be of a type to avoid introducing pattern dependent jitter. The method also requires that the phase demodulator be calibrated so that the vertical indication on the oscilloscope may be related to the jitter amplitude. This may be accomplished by providing a frequency shift between the reference and the data signal and noting the slope of the phase demodulator output. Finally, this technique is only able to resolve jitter less than 1 UI in magnitude in the limit, and in practice less than 1 UI because of nonlinearities in the demodulator transfer function near the limits of its range.

5 Jitter tolerance measurement

Jitter tolerance measurements require a calibrated jitter generator and an error rate measurement device (see figure 10).

– Procedure

1) Connect the equipment as shown in figure 10. With the generator jitter amplitude set to 0 UI pp, verify error-free operation.

2) Set the generator jitter frequency as desired, and increase the jitter amplitude until the onset of errors criterion is reached. Note the jitter amplitude and frequency.

3) Repeat step 2) for a sufficient number of frequencies to determine the jitter tolerance curve.

To verify compliance with a jitter tolerance template:

1) Set the jitter amplitude and frequency to a template point. Verify that the onset of errors criterion is not reached.

2) Repeat step 1) for a sufficient number of template points between frequencies f1 and f3. Template form is described in SMPTE RP 184, 4.1.1).

NOTE – A calibrated jitter receiver can be used to establish the jitter amplitude of an uncalibrated jitter generator.

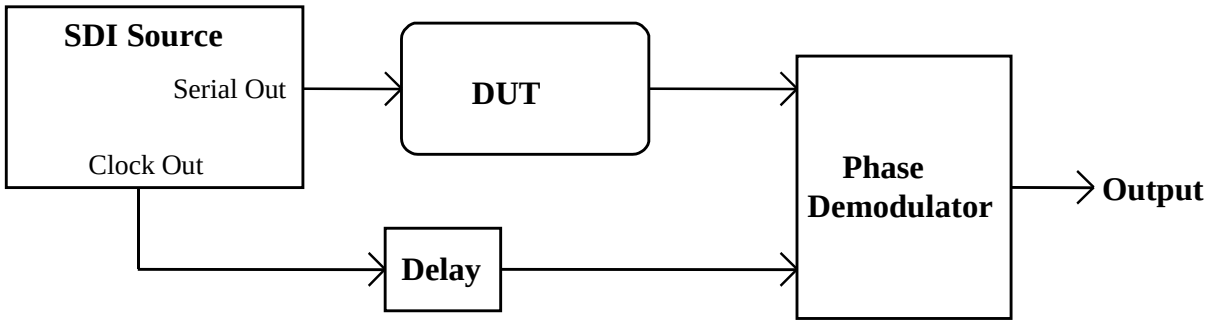


Figure 9 – Phase demodulator measurement with an available reference signal

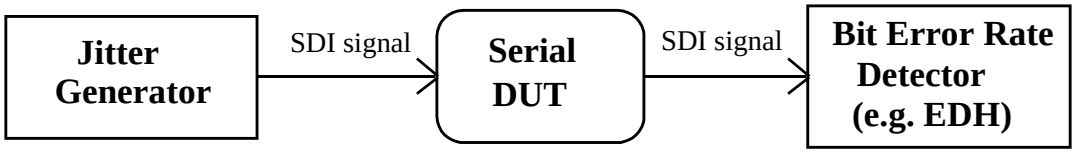


Figure 10 – Jitter tolerance measurement

6 Jitter transfer measurement

Jitter transfer measurements require a calibrated jitter generator and a calibrated jitter receiver (see figure 11). An enhanced method requires a jitter generator with an external jitter input, a jitter receiver, and a spectrum analyzer with a tracking oscillator output (see figure 12).

– Basic technique:

1) Perform a jitter tolerance measurement of the DUT over the desired frequency range.

2) Connect the equipment as shown in figure 11. Set the jitter generator level so that it is less than the measured jitter tolerance over the band of interest, yet large enough for good measurement accuracy.

3) Note the jitter receiver reading and the jitter frequency.

4) Divide the jitter receiver reading by the jitter generator level to obtain the jitter gain at this frequency.

5) Repeat step 3) for a sufficient number of frequencies to determine the jitter transfer function.

NOTE – If the jitter generator or the jitter receiver frequency response is not flat, connect the generator and receiver directly together to establish a deviation table.

– Enhanced technique:

1) Perform a jitter tolerance measurement of the DUT over the desired frequency range.

2) Connect the equipment as shown in figure 12, bypassing the DUT. Verify linear, error-free operation of the jitter receiver.

3) Set the tracking generator output amplitude so that the jitter generator level is less than the measured jitter tolerance over the desired frequency range. Select an appropriate resolution bandwidth on the spectrum analyzer. Save the trace on the analyzer.

4) Connect the DUT. Subtract the stored trace from the display trace. The difference is the DUT jitter transfer function.

NOTE – A network analyzer can be used in place of the spectrum analyzer and tracking generator combination. A vector network analyzer permits measurement of both the phase and magnitude of the jitter transfer function.

To verify compliance with a jitter transfer template: Using either the basic or enhanced technique, verify that the jitter transfer is less than the template requirement, from f1 to 10(fc) (template form is described in SMPTE RP 184, 4.2.1).

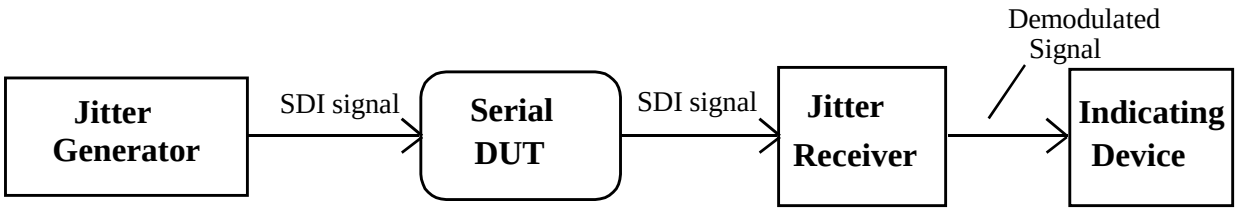


Figure 11 – Jitter transfer function measurement (basic method)

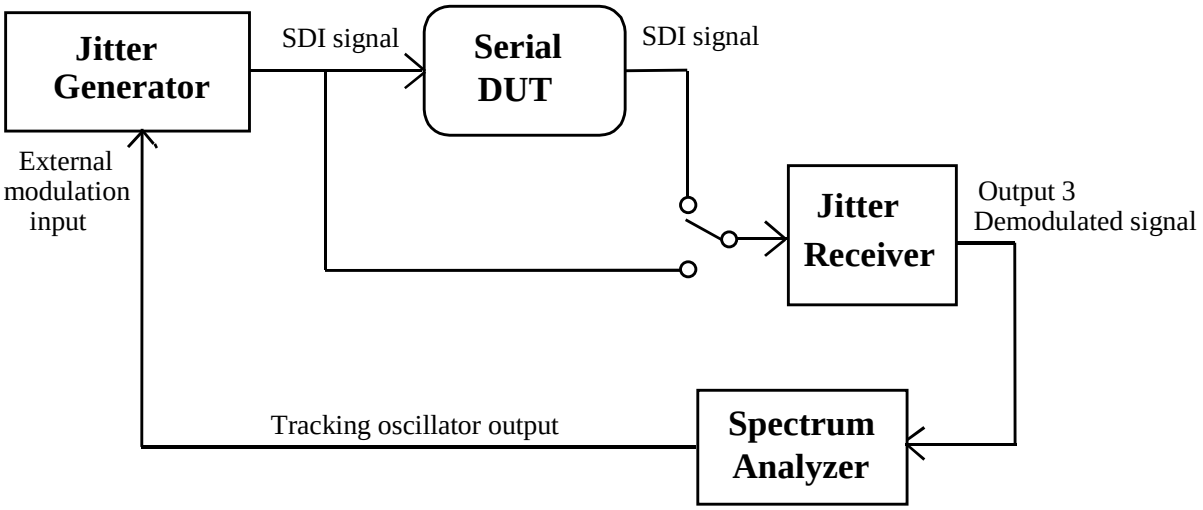


Figure 12 – Jitter transfer function measurement (enhanced method)

Annex A (informative)
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