SMPTE RP 192:2015
Revision of RP 192-2003

SMPTE RECOMMENDED PRACTICE

Jitter Measurement Procedures In Bit-Serial Digital Interfaces

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Approved
September 1, 2015

Foreword

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SMPTE RP 192 was prepared by Technology Committee 32NF.

Intellectual Property

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Introduction

This section is entirely informative and does not form an integral part of this Engineering Document.

Jitter is one of the most important parameters in the performance of serial digital transmission systems. It can cause errors in the transmission and recovery of digital data, and may degrade analog signal performance if the jitter is transferred through the digital-to-analog conversion process. Characterizing and measuring jitter are important for reliable and predictable serial digital system operation.

1 Scope

This Recommended Practice describes methods for measuring jitter performance in bit-serial digital interfaces. The techniques are specifically suited for jitter specifications that follow the form described in SMPTE RP 184.

2 Conformance Notation

Normative text is text that describes elements of the design that are indispensable or contains the conformance language keywords: "shall", "should", or "may". Informative text is text that is potentially helpful to the user, but not indispensable, and can be removed, changed, or added editorially without affecting interoperability. Informative text does not contain any conformance keywords.

All text in this document is, by default, normative, except: the Introduction, any section explicitly labeled as "Informative" or individual paragraphs that start with "Note:"

The keywords "shall" and "shall not" indicate requirements strictly to be followed in order to conform to the document and from which no deviation is permitted.

The keywords, "should" and "should not" indicate that, among several possibilities, one is recommended as particularly suitable, without mentioning or excluding others; or that a certain course of action is preferred but not necessarily required; or that (in the negative form) a certain possibility or course of action is deprecated but not prohibited.

The keywords "may" and "need not" indicate courses of action permissible within the limits of the document.

The keyword “reserved” indicates a provision that is not defined at this time, shall not be used, and may be defined in the future. The keyword “forbidden” indicates “reserved” and in addition indicates that the provision will never be defined in the future.

A conformant implementation according to this document is one that includes all mandatory provisions ("shall") and, if implemented, all recommended provisions ("should") as described. A conformant implementation need not implement optional provisions ("may") and need not implement them as described.

Unless otherwise specified, the order of precedence of the types of normative information in this document shall be as follows: Normative prose shall be the authoritative definition; Tables shall be next; followed by formal languages; then figures; and then any other language forms.

3 Normative References

The following document contains provisions which, through reference in this text, constitute provisions of this recommended practice. At the time of publication, the edition indicated was valid. All documents are subject to revision, and parties to agreements based on this recommended practice are encouraged to investigate the possibility of applying the most recent edition of the document indicated below.

SMPTE RP 184:2015, Specification of Jitter in Bit-Serial Digital Systems

4 Definitions

4.1 Alignment jitter

Variation in position of a signal's transitions relative to those of a clock extracted from that signal. The bandwidth of the clock extraction process determines the low-frequency limit for alignment jitter.

4.2 BER

Acronym for Bit Error Ratio. BER indicates the ratio of errors to total bits received. This is a measure of the integrity of the transmission link.

4.3 Clock extractor

A device which is able to extract the serial data clock from a serial data stream, and outputs a clock-related trigger. It may also provide the serial digital data reclocked with the extracted clock.

4.4 DSO

Acronym for digital storage oscilloscope.

4.5 DUT

Acronym for device under test.

4.6 Error rate tester

A device that quantifies the error rate of a serial digital signal. Two examples are the classic bit error ratio (BER) tester and the field rate CRC method (EDH) described in SMPTE RP 165.

4.7 Independent Samples

For band-limited systems, samples are only independent if they are not over-sampled. By the Nyquist criteria this means that for a given bandwidth in Hz, the maximum number of independent samples per second is approximately twice the bandwidth. Any higher rate of samples will be just giving more information about the same signal components.

4.8 Input jitter tolerance

Peak-to-peak amplitude of sinusoidal jitter that, when applied to an equipment input, causes a specified degradation of error performance.

4.9 Intrinsic jitter

Jitter at an equipment output in the absence of input jitter.

4.10 Jitter

Variation of a digital signal's transitions from their ideal positions in time.

4.11 Jitter generator

A device that produces a serial digital signal containing sinusoidal jitter of adjustable amplitude and frequency.

4.12 Jitter receiver

Demodulates and allows measurement of the jitter present on a serial signal. It commonly provides an output proportional to the demodulated jitter.

4.13 Jitter transfer

Jitter on the output of equipment resulting from applied input jitter.

4.14 Jitter transfer function

Ratio of the output jitter to the applied input jitter as a function of frequency.

4.15 Output jitter

Jitter at the output of equipment that is embedded in a system network. It consists of intrinsic jitter and the jitter transfer of jitter at the equipment input.

4.16 Phase demodulator

A device that provides as its output a signal proportional to the phase difference of two input signals.

4.17 Probabilistic Peak-to-Peak Jitter (p-p-p, Stated as Jitter at 1 in 10^x)

This is an estimate of the most likely p-p jitter in unit intervals when measured over 10^x independent jitter samples. See SMPTE RP 184 for derivation.

4.18 SDI

Acronym for Serial Digital Interface.

4.19 Timing jitter

Variation in position of a signal's transitions occurring at a rate greater than a specified frequency, typically 10 Hz or less. Variations occurring below this specified frequency are termed wander and are not addressed by this practice.

4.20 Unit interval (UI)

Abbreviated "UI", it is the period of one clock cycle. It corresponds to the nominal minimum time between transitions of the serial signal.

5 Common Guidelines for Indicating Device Specifications

For all the measurement types and methods in this Recommended Practice, the following guidelines should be observed for optimal results:

1) All high-speed signals, especially SDI signals, shall be terminated in the appropriate impedance. For SDI signals this means to terminate in 75 ohms with return loss that meets the relevant SMPTE specification.

2) All SDI measurement inputs shall have sufficient bandwidth to prevent a significant degradation in the signal. For the time domain methods, the measuring device shall cause no more than a 20% increase in the risetime relative to a measurement with unlimited bandwidth. For frequency domain methods the measuring device shall be able to display signals up to the serial rate plus the jitter frequency limit f4 in order to observe the jitter sidebands.

3) For the time-domain methods, the horizontal and/or trigger bandwidth of the indicating device shall not attenuate the observed jitter. The trigger bandwidth shall be at least f3.

4) For the time-domain methods, the indicating device shall not create inter-symbol interference at the zero-crossing point. This requires a vertical system step response that transitions and settles in less than 1 UI.

5) The indicating device shall acquire sufficient samples so that peak-to-peak jitter can be determined. This requires sampling until the shape of the jitter distribution is known. If the jitter specification includes a measurement time, this shall be the minimum acquisition time. The maximum acquisition time will depend on the device sample rate and the type of jitter distribution. For example, a sinusoidal distribution will typically be determined with fewer samples than will a Gaussian-like distribution. If the jitter specification includes a sample size or probability at which the jitter must be satisfied then the indicating device shall collect samples to meet those specifications. If a probability is specified then the indicating device shall indicate if the jitter measurement at that probability is directly measured or extrapolated from a smaller sample set.

6) The minimum measurement time “tm” shall be as specified in SMPTE RP 184. Depending on the type of indicating device, the actual measurement time may be significantly longer than the minimum in order to collect required number of samples or p-p-p threshold.

7) If the indicating device is an oscilloscope, the jitter measurement is usually made at the eye crossing. A digital storage oscilloscope with infinite persistence is recommended.

6 Intrinsic and Output Jitter Measurement

Seven methods are described and each of these methods has advantages and disadvantages. The particular characteristics of each method are discussed in the individual sections. The implementer can choose the method which is most appropriate for a particular application. The method described in Section 6.2 is considered the preferred reference method.

The first of the seven methods uses an available reference clock to trigger an oscilloscope; the second and third use a clock extractor with defined characteristics to trigger the oscilloscope; the fourth uses a spectrum analyzer; the fifth and sixth are based on a phase demodulator method jitter receiver; the seventh method uses a clock extractor and a Bit Error Ratio Tester (BERT).

6.1 Oscilloscope Measurement by Means of Triggering on a Reference Signal

If a reference signal is available, a basic jitter measurement can be done (see Figure 1). The oscilloscope is directly triggered by the reference signal. This reference signal could also be a serial digital signal with high stability. The digital data signal is connected to the suitably terminated vertical channel of the oscilloscope and an eye measurement is done. The jitter is typically measured at the eye crossing.

– Presentation of measurement results: The test signal, the jitter amplitude, the parameters of the oscilloscope (bandwidth, etc.), and the measurement time should be indicated.

– Background information: This measurement procedure provides a coarse survey of jitter in an SDI signal. The measurement result depends on the stability of the reference signal (its jitter sets the measurement floor), the type of oscilloscope, and the measurement time (e.g., when a DSO is used in persistence mode). All of these parameters influence the measurement result and contribute to variability in the result as conditions vary. This method does not allow bandwidth restriction as generally required in jitter specification. This method is not recommended if other jitter measurement methods are available. The frequency of the reference should not be closely related to the word rate. This will avoid masking word rate jitter. For example, the reference frequency should not be the serial rate divided by 10 or 20.

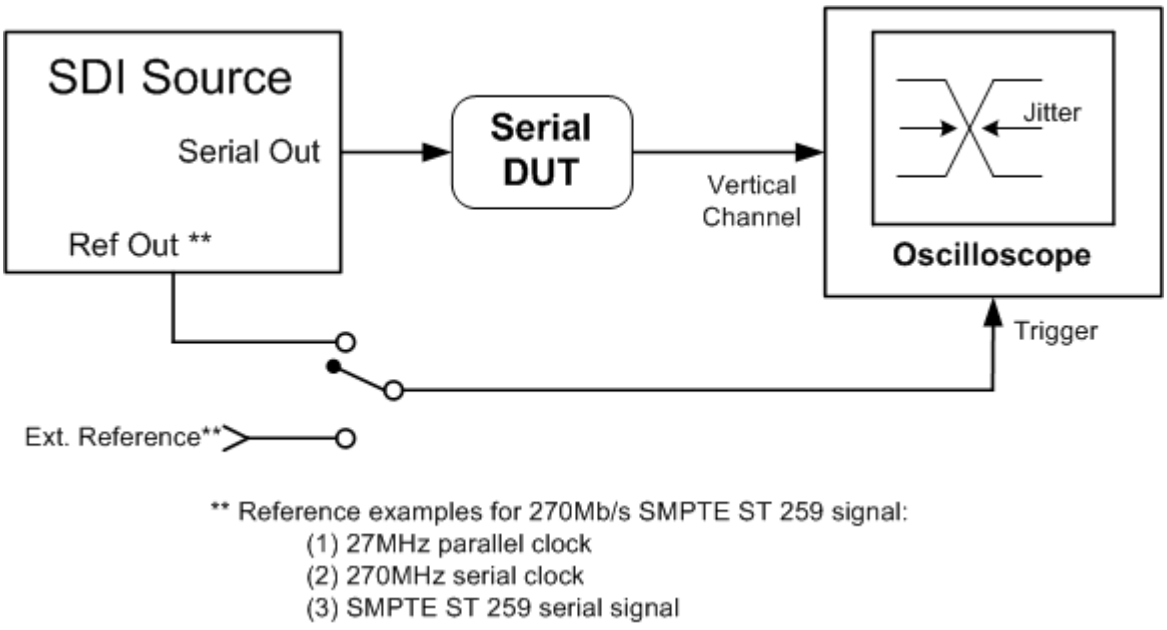

Figure 1 – Jitter measurement by means of an external reference signal

6.2 Jitter Measurement by Means of a Clock Extractor – Reference Method

The jitter in a signal output can be measured by using a device to extract a clock and then trigger an oscilloscope or other indicating device. The exact connection necessary depends on the amount of jitter in the signal to be measured. Whenever possible, the connection in Figure 2 should be used. If the jitter is greater than 1 UI, then the connection of Figure 2 no longer works, so the connection in Figure 5 is recommended. With the Figure 5 connection, the upper bandwidth of the jitter measurement is typically limited to less than the f4 value. These methods are explained in detail in Section 6.2.1 for timing jitter and Section 6.2.2 for alignment jitter.

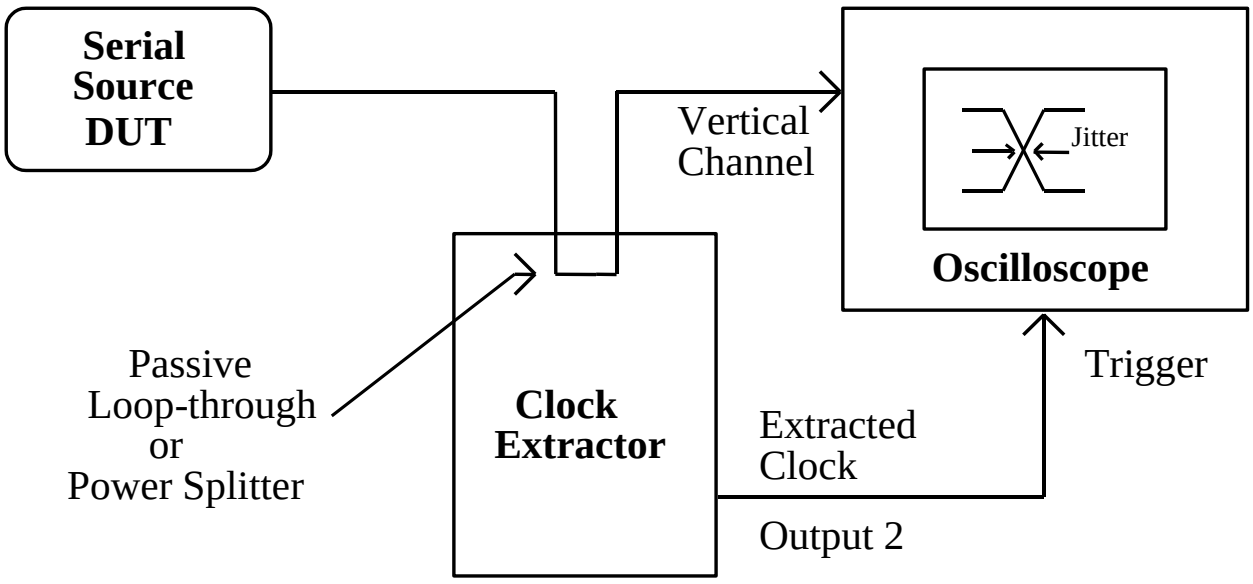

Figure 2 – Jitter measurement less than 1 UI using a clock extractor

The clock extractor typically consists of a wideband clock recovery circuit followed by a second, narrow band PLL (see Figure 3). This second PLL can be set to two different loop bandwidths, so that two different jitter transfer functions are available (see Figure 4). Clock output 2 is used to trigger the indicating device. The clock extractor shall have the following characteristics:

1) It shall be capable of being put in series with the signal output and provide enough signal level for the indicating device. It shall not modify the output signal characteristics in ways that obscure or modify the jitter on the signal.

2) To measure timing jitter (A1), the clock extractor shall have a clock recovery bandwidth of f1. To measure alignment jitter (A2), the clock extractor shall have a clock recovery bandwidth of f3 (see Figure 4). The number of integrations within the clock extractor PLL shall be at least two (TYPE II PLL) to provide at least a 40 dB/decade attenuation to wander or low-frequency jitter in the jitter indication devices.

Note: When set to f1, a three-integrator PLL (TYPE III) is preferred providing 60 dB/decade wander attenuation. However, since these are more difficult to design, a Type II is acceptable. When set to f3, it is preferable that only one integrator be active so the roll-off is 20dB/decade near the f4 frequency. In rare circumstances a higher order roll-off can differentiate jitter and increase the observed p-p value. For diagnostic purposes it may be useful to set the HPF to a lower frequency and note the difference in the measured jitter.

3) The jitter transfer function of the clock extractor shall roll-off at 20 dB/decade or greater and have a minimum phase response unless otherwise specified. Ripple within the pass band shall be less than ± 1 dB (see Figure 4).

4) The extracted clock frequency shall be the serial clock frequency divided by n, where n should be chosen to display jitter that is related to common parallel clock frequencies.

5) The clock extractor may have an optional clock output 1, which has a clock recovery bandwidth fcr greater than or equal to f3. It is preferable that fcr equal f4.

Note: The wide-band clock recovery block with a bandwidth of f4 is difficult if not impossible to implement if the specification puts f4 at a significant fraction of the bit rate. This difficulty is inherent in the nature of the scrambling used in SDI signals and is especially difficult when processing the EAV/SAV headers and the pathological signals. Because of this limit on the upper frequency for the clock recovery, some methods based on recovered clock as per Figure 5 often provide only a partial result for timing and alignment jitter.

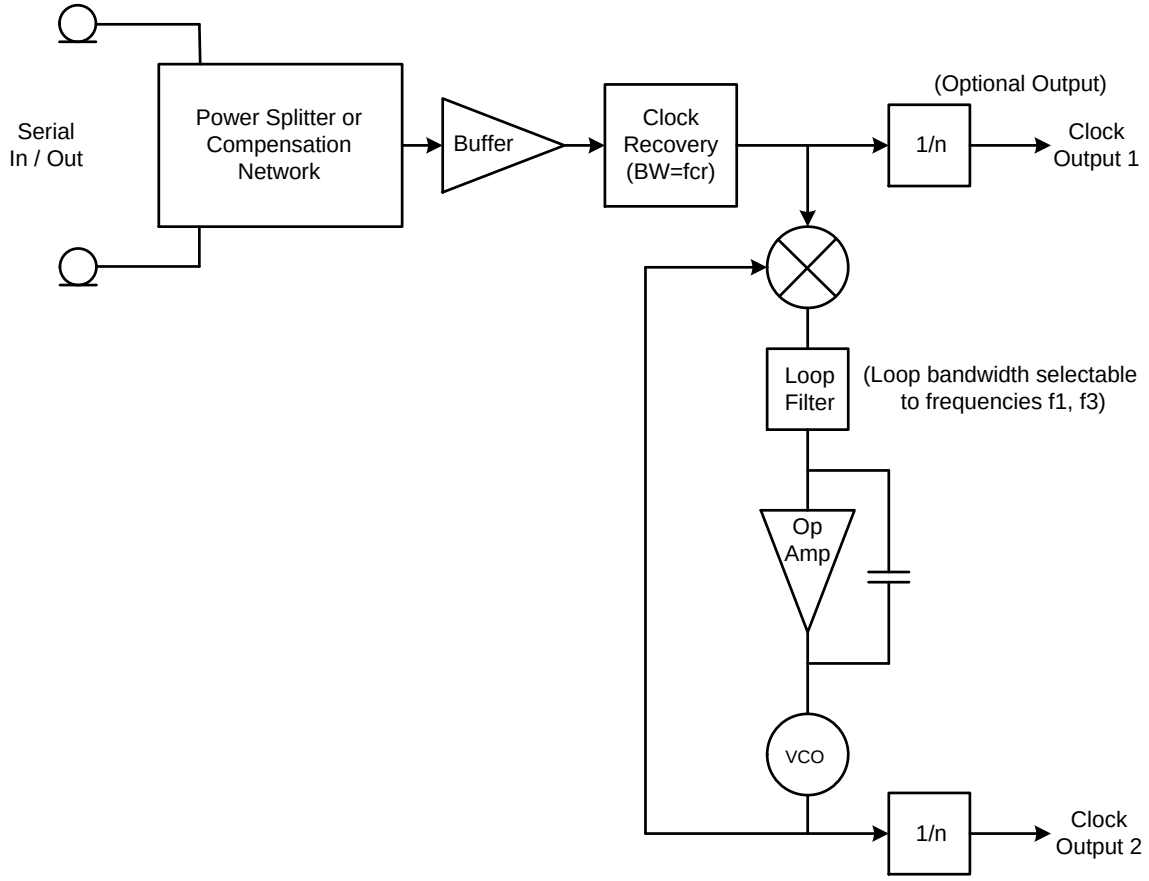

Figure 3 – Clock extractor block diagram

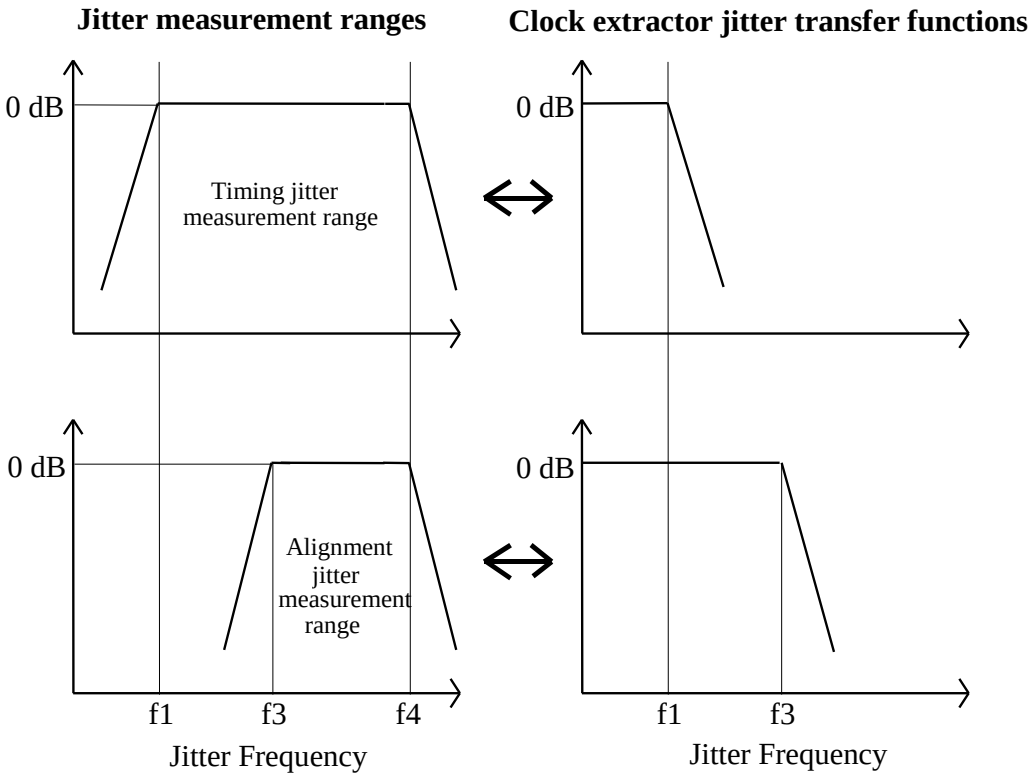

Figure 4 – Jitter measurement bandwidths and corresponding clock extractor jitter transfer function

6.2.1 Measurement of timing jitter

The clock extractor is set to bandwidth f1. The clock output 2 is connected to the trigger channel of the oscilloscope. The signal connected to the oscilloscope vertical channel depends on the jitter amplitude being measured. For jitter amplitudes less than 1 UI, the loop-through signal is used (see Figure 2). For jitter amplitudes greater than 1 UI, two different connections are possible:

1) (Preferred) If the clock extractor has a clock 1 output (Figure 3), this signal is applied to the oscilloscope vertical channel (see Figure 5). This connection will ensure jitter between frequencies f1 and fcr, where fcr is the bandwidth of the wideband clock recovery circuit.

2) If the clock extractor has simultaneous outputs at bandwidths f1 and f3, one output is connected to the vertical channel and the second to the trigger. This connection measures jitter between frequencies f1 and f3.

– Presentation of measurement results: The test signal, the type of oscilloscope, the measurement time, and the jitter amplitude measured at the eye crossing should be documented. A screen plot of the eye pattern is recommended. If the jitter is measured as p-p-p jitter, then the probability at which it is measured must be displayed. In addition, if the value is extrapolated from a smaller sample size then it must be marked as extrapolated. For example, p-p-p jitter might look like: Timing jitter = 43ps at 1 in 10^6 (Direct), 75ps at 1 in 10^{12} (Extrapolated)

6.2.2 Measurement of alignment jitter

The clock extractor is set to bandwidth f3. The clock output 2 is connected to the trigger channel of the oscilloscope. The loop-through signal is connected to the oscilloscope vertical channel (see Figure 2).

– Presentation of measurement results: The test signal, the type of oscilloscope, the measurement time, and the jitter amplitude measured at the eye crossing should be documented. A screen plot of the eye pattern is recommended. If the jitter is measured as p-p-p jitter, then the probability at which it is measured must be displayed. In addition, if the value is extrapolated from a smaller sample size then it must be marked as extrapolated. Alignment jitter = 33ps at 1 in 10^6 (Direct), 65ps at 1 in 10^{12} (Extrapolated).

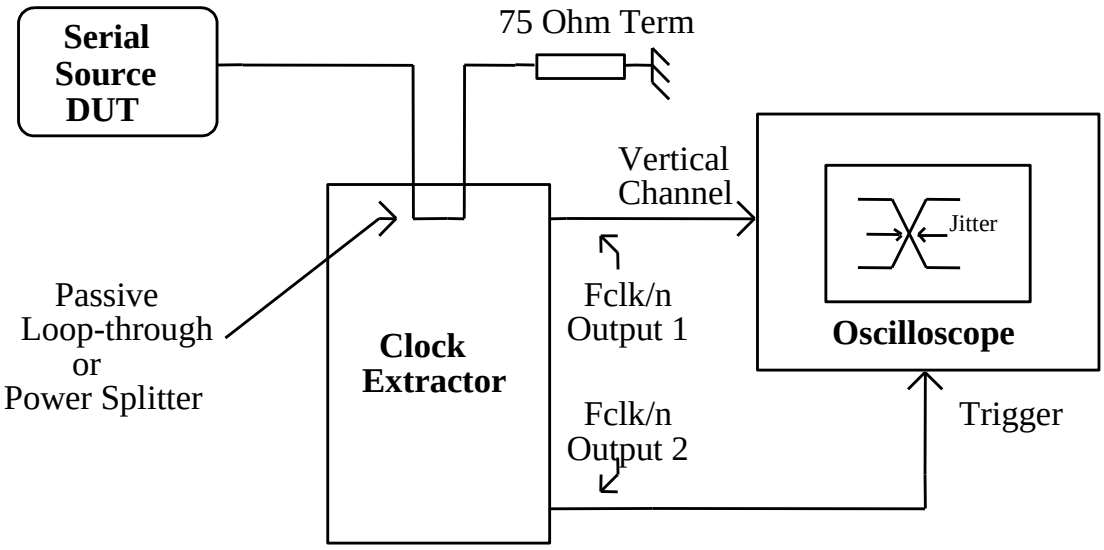

Figure 5 – Measuring jitter greater than 1 UI using a clock extractor and an oscilloscope

6.3 Jitter Measurement by Means of a Digital Sampling Oscilloscope and a Software (SW) Based Clock Extractor

Some Oscilloscopes can implement the jitter measurement clock-extractor in SW. Given a real-time acquisition with sufficient sample rate and memory depth, the correct SW can calculate the clock position for each unit interval and use that to determine the jitter. This is equivalent to Figure 2 and Figure 3, except that the clock extractor is SW inside the oscilloscope. Typically the SW can be configured to implement the high-pass filters as needed for Timing and Alignment jitter. This method can handle more than one UI of jitter, and can display jitter up to the bandwidth limit inherent in the SDI data density. To work well, the sample rate should be set to get at least 2 samples on each rising and falling edge. So for a 70-ps edge, one might need to sample at 50-ps intervals (Sample rate of 20Gs/s). The record needs to be longer than the period of the lowest jitter frequency of interest. For Alignment jitter at 100 kHz, this implies a sample window of at least 10 us. Generally 1.5 times this is needed to allow filters to settle. So reasonable sample windows and record lengths for 3 Gb/s SDI are shown below:

- 100-kHz Alignment jitter, 15us window, 300k record length with the scope sampling at 20Gs/s;
- 10-Hz Timing Jitter, 150-ms window, 3G record length with the scope sampling at 20Gs/s.

Other SDI rates scale from these values depending on the specified filter bandwidths and the sample rate needed to oversample the rise time of the signal. If it is desired to capture Alignment jitter over the entire video frame, then a longer record is needed.

This method will typically report the jitter in a variety of formats, including Tie at BER, both measured and extrapolated to 10^{-12}. This number may be related to the p-p-p jitter as indicated in SMPTE RP 184.

While this method is excellent at measuring the jitter on each acquisition, the time to calculate the jitter from each acquisition may be several seconds. During the calculation, the system is not acquiring samples, so the percentage of the time when jitter samples are taken is typically quite low.

6.4 Phase Noise Measurement by Means of a Clock Extractor

This section describes a simple method for making a phase noise measurement on the extracted clock using a spectrum analyzer. This technique allows an examination of the side bands of the clock signal, which correspond with the jitter frequencies in the SDI signal (see Figure 6).

The output 1 of the clock extractor is connected to a spectrum analyzer. The spectrum analyzer is switched to phase noise measurement and the phase noise of the clock under test is examined.

The primary use of this technique is for identification of jitter components. It is also possible to convert phase noise amplitudes to RMS jitter but the methods to accomplish that are outside the scope of this document.

– Presentation of measurement results: The test signal, the clock extractor PLL bandwidth, the resolution bandwidth and span of the spectrum analyzer, and a plot of the spectrum should be indicated.

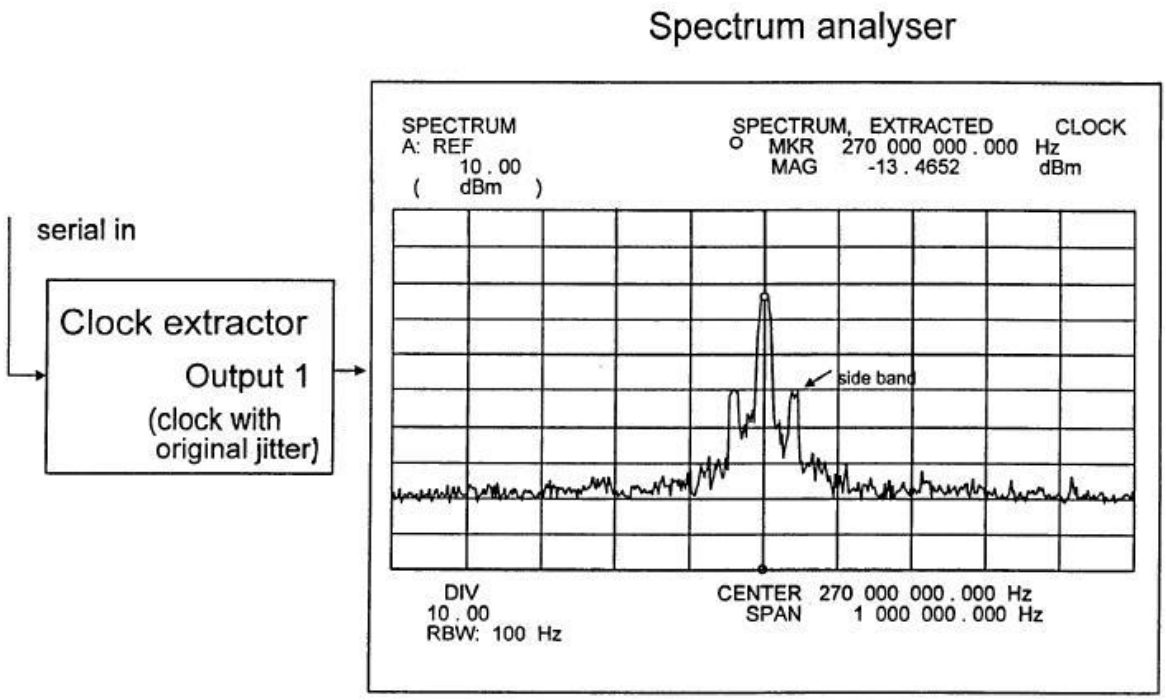

Figure 6 – Jitter measurement by means of a clock extractor and a spectrum analyzer

6.5 Jitter Measurement Using a Phase Demodulator

Jitter can be conveniently observed and measured if the phase modulation sidebands are heterodyned down to dc. One popular method is to recover two clocks from the signal, one with a very wide clock recovery bandwidth and the second with a narrow bandwidth, and apply them to a phase demodulator (see Figure 7). The output signal is then applied through selectable bandpass filters to a peak reading voltmeter. The output can also be applied to a spectrum analyzer to observe the jitter frequency terms (see Figure 8). Jitter receivers typically use the phase demodulator method.

A jitter receiver shall be capable of measuring peak-to-peak jitter over the jitter measurement bandpasses described in SMPTE RP 184 in both Figure 5 and Table 3.

Note: The wide-band clock recovery block with a bandwidth of f4 is difficult if not impossible to implement if the specification puts f4 at a significant fraction of the bit rate. This difficulty is inherent in the nature of the scrambling used in SDI signals especially when processing the EAV/SAV headers as well as the pathological signals. Because of this limit on the upper frequency for the clock recovery, the method in Figure 7 works well for large low-frequency jitter, but often provides only a partial result for timing and alignment jitter.

The jitter spectrum can be observed by connecting the phase demodulator output to a spectrum analyzer or an oscilloscope with fast Fourier transform (FFT) option (see Figure 8).

– Presentation of measurement results: The test signal, measurement time, measured jitter level and measurement bandpass, and a description of the measurement equipment should be documented.

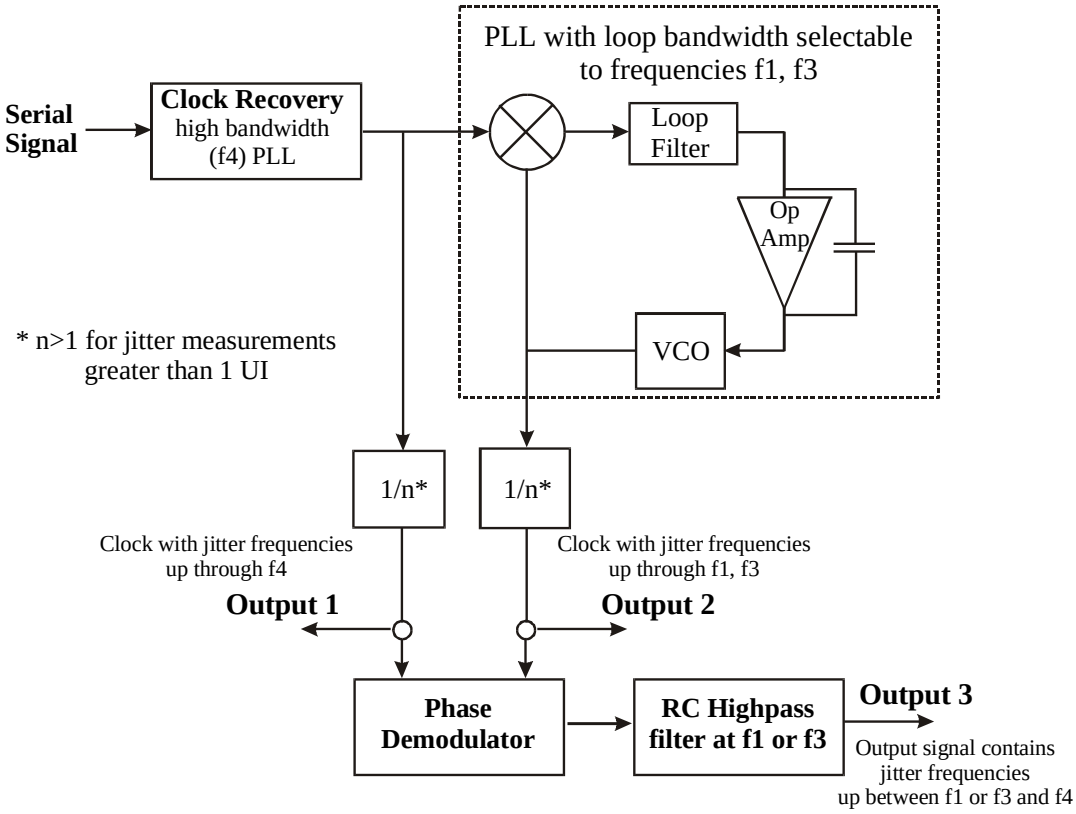

Figure 7 – Block diagram of a jitter receiver (clock extractor, high-quality PLL, demodulator)

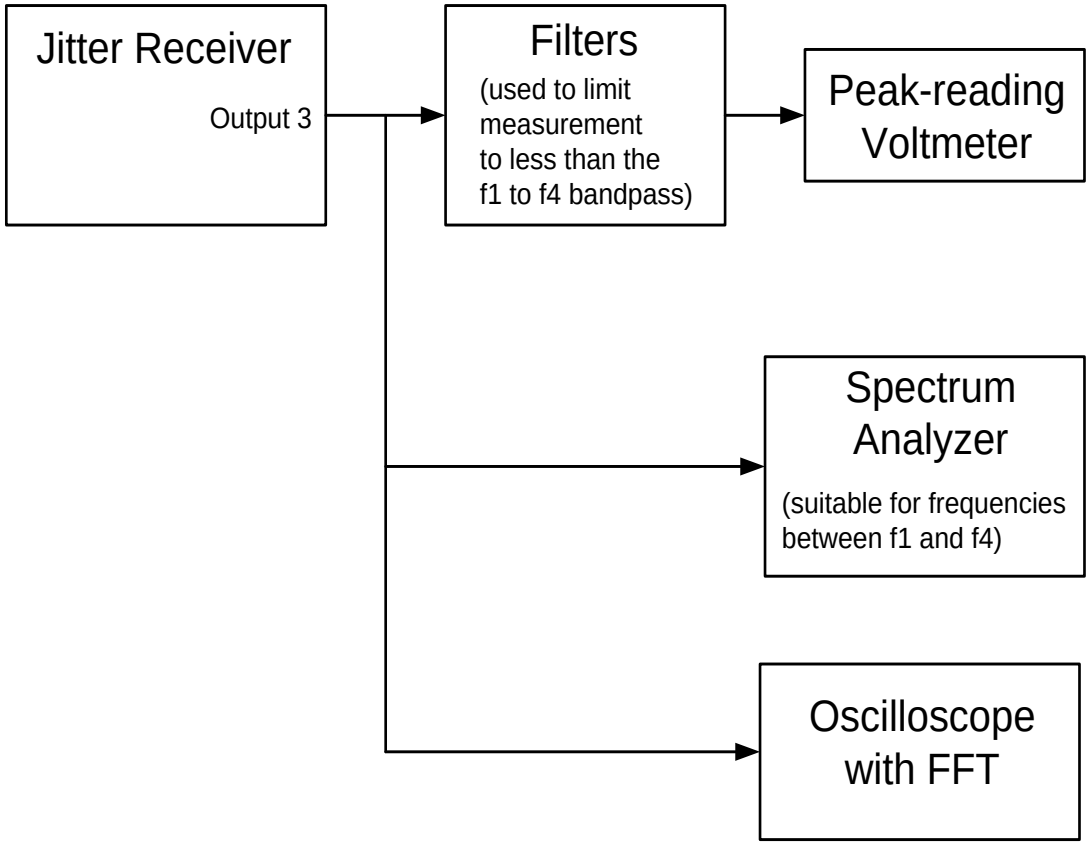

Figure 8 – Jitter receiver output connections

6.6 Phase Demodulator Measurement with an Available Reference Signal

If a reference signal is available, then a demodulated jitter measurement may be made using the set-up shown in Figure 9. The reference and data signals are connected to the two inputs of a digital phase demodulator. The output of the demodulator may be processed in several ways. The output may be filtered to establish the lower and upper band edges and then passed to an oscilloscope for display of the jitter results (note that the vertical scale of the oscilloscope now represents the jitter amplitude). Alternatively, the demodulated jitter waveform may be captured and then digitally filtered to establish the upper and lower band edges. Finally, the jitter spectrum may be obtained either by performing an FFT on a captured waveform, or by connecting the demodulator output to a spectrum analyzer.

– Presentation of measurement results: The test signal type, the upper and lower band edges, the measurement time, and the peak-to-peak jitter amplitude should be recorded.

– Background information: This measurement method is sensitive to any pattern dependent jitter introduced by the phase detector in the jitter demodulator. The phase detector shall be of a type to avoid introducing pattern dependent jitter. The method also requires that the phase demodulator be calibrated so that the vertical indication on the oscilloscope may be related to the jitter amplitude. This may be accomplished by providing a frequency shift between the reference and the data signal and noting the slope of the phase demodulator output. Finally, this technique is only able to resolve jitter less than 1 UI in magnitude in the limit, and in practice less than 1 UI because of nonlinearities in the demodulator transfer function near the limits of its range.

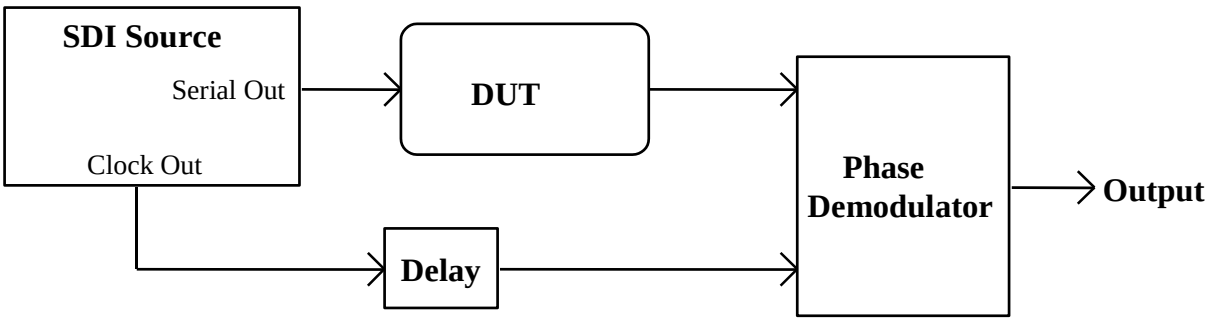

Figure 9 – Phase demodulator measurement with an available reference signal

6.7 Jitter Measurement with a Bit Error Ratio Tester (BERT)

Some BERTs have the ability to display an eye pattern and measure jitter. The BERT works by having two comparators that look at each bit interval. The voltage and sample time for each comparator can be adjusted. Typically the two comparators are programmed to look at two closely spaced points on the eye. If the outputs of the comparators are different on a given sample then the input signal must have passed through that portion of the eye. A counter keeps track of the hits at each point and the result is plotted to create an eye. To measure jitter the two comparators are moved across the eye crossing to create a histogram of the jitter.

The main advantage of the BERT method is that a measurement is made on each transition of the input signal, so the jitter can be directly measured to a lower probability. Even with this method it will take many hours to get a true 1 in 10^{12} probability. BERT testers work best on standard pseudo-random sequences so the receiver can recognize the pattern, but they can work on arbitrary data such as SDI signals with some limitations. BERT testers typically need an external clock recovery just like many of the oscilloscope methods, so Figure 2 is appropriate with the BERT in place of the oscilloscope.

Note: Some BERTs are intended for telecom applications and may not have a clock recovery with the ability to implement the 10-Hz HPF needed for timing measurements. In this case, an external clock recovery circuit with the 10-Hz bandwidth may allow the BERT to achieve the desired measurement characteristics.

7 Jitter Tolerance Measurement

Jitter tolerance measurements require a calibrated jitter generator and an error rate measurement device (see Figure 10).

Procedure:

1) Connect the equipment as shown in Figure 10. With the generator jitter amplitude set to 0 UI pp, verify error-free operation.

2) Set the generator jitter frequency as desired, and increase the jitter amplitude until the onset of errors criterion is reached. Note the jitter amplitude and frequency.

3) Repeat step 2 for a sufficient number of frequencies to determine the jitter tolerance curve.

To verify compliance with a jitter tolerance template:

1) Set the jitter amplitude and frequency to a template point. Verify that the onset of errors criterion is not reached.

2) Repeat step 1 for a sufficient number of template points between frequencies f1 and f3. (Template form is described in Section 5.1 of SMPTE RP 184.)

Note: A calibrated jitter receiver can be used to establish the jitter amplitude of an uncalibrated jitter generator.

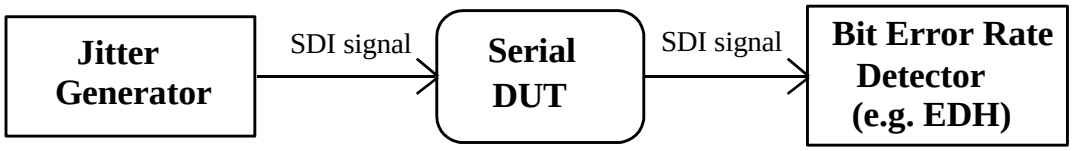

Figure 10 – Jitter tolerance measurement

8 Jitter Transfer Measurement

Jitter transfer measurements require a calibrated jitter generator and a calibrated jitter receiver (see Figure 11). An enhanced method requires a jitter generator with an external jitter input, a jitter receiver, and a spectrum analyzer with a tracking oscillator output (see Figure 12).

Basic technique:

1) Perform a jitter tolerance measurement of the DUT over the desired frequency range.

2) Connect the equipment as shown in Figure 11. Set the jitter generator level so that it is less than the measured jitter tolerance over the band of interest, yet large enough for good measurement accuracy.

3) Note the jitter receiver reading and the jitter frequency.

4) Divide the jitter receiver reading by the jitter generator level to obtain the jitter gain at this frequency.

5) Repeat step 3 for a sufficient number of frequencies to determine the jitter transfer function.

Note: If the jitter generator or the jitter receiver frequency response is not flat, connect the generator and receiver directly together to establish a deviation table.

Enhanced technique:

1) Perform a jitter tolerance measurement of the DUT over the desired frequency range.

2) Connect the equipment as shown in Figure 12, bypassing the DUT. Verify linear, error-free operation of the jitter receiver.

3) Set the tracking generator output amplitude so that the jitter generator level is less than the measured jitter tolerance over the desired frequency range. Select an appropriate resolution bandwidth on the spectrum analyzer. Save the trace on the analyzer.

4) Connect the DUT. Subtract the stored trace from the display trace. The difference is the DUT jitter transfer function.

Note: A network analyzer can be used in place of the spectrum analyzer and tracking generator combination. A vector network analyzer permits measurement of both the phase and magnitude of the jitter transfer function.

To verify compliance with a jitter transfer template: Using either the basic or enhanced technique, verify that the jitter transfer is less than the template requirement, from f1 to 10(fc) (template form is described in SMPTE RP 184, Section 5.2).

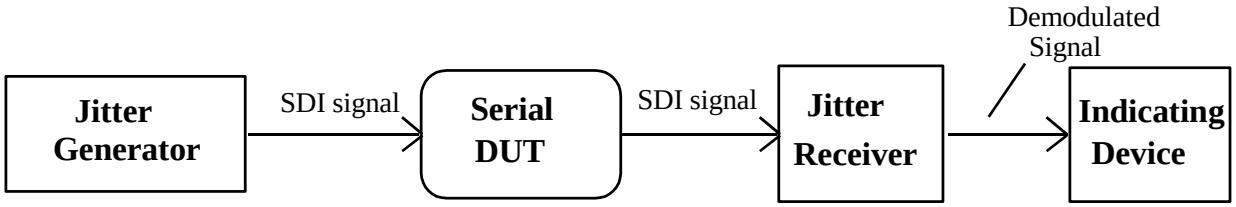

Figure 11 – Jitter transfer function measurement (basic method)

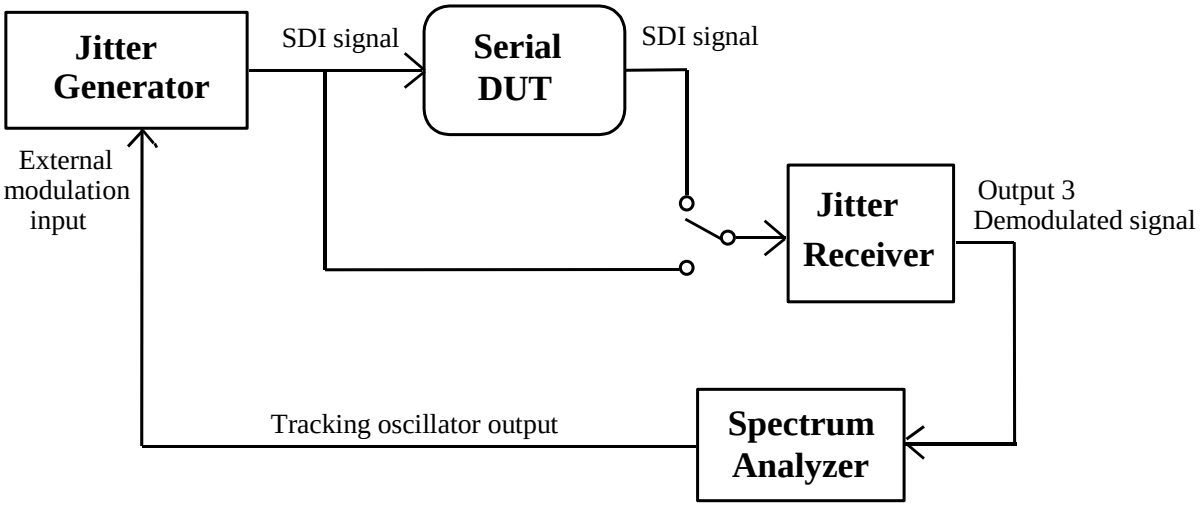

Figure 12 – Jitter transfer function measurement (enhanced method)

9 Jitter Measurements on Optical Systems (Informative)

Jitter measurements on optical interface signals requires translating the optical signal back to an electrical one. Careful choice of the conversion equipment is necessary. The translation process has the potential to add jitter, or reduce the jitter if it contains reclocking or other processing. After optical to electrical conversion, the other portions of this document are applicable.

Annex A Bibliography (Informative)

Note: All references in this document to other SMPTE documents use the current numbering style (e.g. SMPTE ST 259:2008) although, during a transitional phase, the document as published (printed or PDF) may bear an older designation (such as SMPTE 259M-2008). Documents with the same root number (e.g. 259) and publication year (e.g. 2008) are functionally identical.

SMPTE RP 165:1994, Error Detection Checkwords and Status Flags for Use in Bit-Serial Digital Interfaces for Television

SMPTE ST 259:2008, Television — SDTV Digital Signal/Data — Serial Digital Interface

SMPTE ST 292-1:2012, 1.5 Gb/s Signal/Data Serial Interface

SMPTE ST 297:2015, Serial Digital Fiber Transmission System for SMPTE ST 259, SMPTE ST 344, SMPTE ST 292-1/2, SMPTE ST 424, SMPTE ST 2081-1 and SMPTE ST 2082-1 Signals

SMPTE ST 344:2000, Television — 540 Mb/s Serial Digital Interface

SMPTE ST 424:2012, 3 Gb/s Signal/Data Serial Interface

SMPTE ST 435-3:2012, 10 Gb/s Serial Signal/Data Interface — Part 3: 10.692 Gb/s Optical Fiber Interface

SMPTE ST 2036-4:2015, Ultra-High Definition Television – Multi-link 10Gb/s Signal/Data Interface Using 12-bit width Container

SMPTE ST 2081-1:2015, 6 Gb/s Signal/Data Serial Interface — Electrical

SMPTE ST 2082-1:2015, 12 Gb/s Signal/Data Serial Interface — Electrical

EBU Tech. 3267 (1992), EBU Interfaces for 625-Line Digital Video Signals at the 4:2:2 Level of Recommendation ITU-R BT.601 (2nd Edition)

EBU Tech. 3283 (1996), Measurement of Digital Component Television Studios — 625-Line Systems at the 4:2:2 and 4:4:4 Levels Using Parallel and Serial Interfaces (SDI)

ITU-R BT.656-5 (12/2007), Interface for Digital Component Video Signals in 525-Line and 625-Line Television Systems Operating at the 4:2:2 Level of Recommendation ITU-R BT.601 [Part A]