RP 198-1998

SMPTE RECOMMENDED PRACTICE

Bit-Serial Digital Checkfield for Use in High-Definition Interfaces

1 Scope

This practice specifies digital test signals suitable for evaluating the low-frequency response of equipment handling high-definition serial digital video signals as defined in ANSI/SMPTE 292M. Although a range of signals will produce the desired low-frequency effects, two specific signals are defined to test cable equalization and phase locked loop (PLL) lock-in, respectively. In the past, these two signals have been colloquially called "pathological signals."

2 General considerations

Stressing of the automatic equalizer is accomplished by using a signal with the maximum number of ones or zeros, with infrequent single clock period pulses to the opposite level. Stressing of the phase locked loop is accomplished by using a signal with a maximum low-frequency content; that is, with a maximum time between level transitions.

2.1 Channel coding of the serial digital signal defined by ANSI/SMPTE 292M utilizes scrambling and encoding into NRZI (nonreturn to zero, inverted) accomplished by a concatenation of the two following functions:

$$G_1(X) = X^9 + X^4 + 1 \qquad G_2(X) = X + 1$$

As a result of the channel coding, long runs of zeros in the G_2 (X) output data can be obtained when the scrambler, G_1 (X), is in a certain state at the time when the specific words arrive. That certain state will be present on a regular basis; therefore, continuous application of the specific data words will regularly produce the low-frequency effects (see annex A).

2.2 Although the longest run of parallel data zeros (40 consecutive zeros) will occur during the EAV/SAV TRS words, the frequency with which the scrambling of the TRS words coincide with the required scrambler state to permit either stressing condition is low. In the instances where this coincident occurs, the generation of the stressing condition is so time limited that equalizers and phase locked loops are not maximally stressed.

2.3 In the data portions of digital video signals (excluding TRS words in EAVs or SAVs, and ANC data flag words), the sample values are restricted to exclude data levels 0 to 3 and 1020 to 1023 (000_h to 003_h and $3FC_h$ to $3FF_h$ in 10-bit hexadecimal representation and 00.0 to 00.C and FF.0 to FF.C, in 8.2 hexadecimal notation). The result of this restriction is that the longest run of zeros, at the scrambler input, is 16 (bits), occurring when a sample value of 200_h is followed by a value between 004_h and 007_h. This situation can produce up to 26 consecutive zeros at the NRZI output, which is (also) not a maximally stressed case.

2.4 Other specific data words in combination with specific scrambler states can produce a repetitive low-frequency serial output signal until the next EAV or SAV affects the scrambler state. It is these combinations of data words that form the basis of the test signals defined by this practice.

2.5 Because of the Y/C interleaved nature of the component digital signal, it is possible to obtain nearly any permutation of word pair data values over the entire active picture area by defining a particular flat color field in a noise-free environment. Certain of these permutations of word pair data values will produce the desired low-frequency effects.

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3 Checkfield data

3.1 Receiver equalizer testing is accomplished by producing a serial digital signal with maximum dc content. Applying the sequence 300_h, 198_h (C0.0, 66.0) continuously to the C and Y samples (respectively) during the active line will produce a signal of 19 consecutive high (low) states followed by one low (high) state in a repetitive manner, once the scrambler attains the required starting condition. Either polarity of the signal can be realized, indicated by the level of the 19 consecutive states. By producing approximately half of a field of continuous lines containing this sequence, the required scrambler starting condition will be realized on several lines, and this will result in the generation of the desired equalizer testing condition.

3.2 Receiver phase locked loop testing is accomplished by producing a serial digital signal with maximum low-frequency content and minimum high-frequency content (i.e., lowest frequency of level transitions). Applying the sequence 200_h, 110_h, (80.0, 44.0) continuously to the C and Y samples (respectively) during the active line will produce a signal of 20 consecutive high (low) states followed by 20 low (high) states in a repetitive manner, once the scrambler attains the required starting condition. By producing approximately half of a field of continuous lines containing this sequence, the required scrambler starting condition will be realized on several lines, and this will result in the generation of the desired phase locked loop testing condition.

3.3 Because the equalizer test works by producing a serial digital signal with a dc bias, steps must be taken to ensure that both polarities of dc bias are realized. To change the polarity of the dc bias from one frame to the next, the sum total of all the bits in all the data words in all the lines in a video field must be odd.

To ensure that the polarity of the bias can change often, a single Y sample data word in the signal is changed from 198_h to 190_h (a net change of 1 data bit), once every other frame. This causes the bias polarity to alternate at a frame rate regardless of whether the original frame bit sum is even or odd. The data word in which the value substitution is made is the first Y sample in the first active picture line of every other frame. The specific word and line for each signal format is listed in table 1 as the polarity control word.

3.4 The sequence 300_h, 198_h (C0.0, 66.0) and 200_h, 110_h (80.0, 44.0) applied to C and Y samples results in shades of purple and gray, respectively. Reversing the C and Y ordering for each of these two sequences results in lighter and darker shades of green, respectively. Table 1 illustrates one ordering of each of the two sequences, but either ordering of the data values for each sequence is permitted by this practice.

If the ordering described in 3.1 is reversed, then the polarity control word described in 3.3 is changed to 200_h (80.0). The polarity control word in either case is located at the first Y sample in the first active picture line in the field(s) specified in 3.3.

4 Serial digital interface (SDI) checkfield

Distribution of data in the SDI checkfield is shown in figure 1 for the signal standards referenced in annex A. Specific distributions of sample values are shown in table 1. In each field, the line where the signal transitions from the equalizer test signal data pattern to the phase locked loop test signal data pattern is specified as a range of lines, rather than as a single specific line. Although the specific line selected within the specified range in not technically significant, the transition point should be consistent from frame to frame and from field to field (in the case of interlaced signal formats).

Table 1 – SDI checkfield sample values

		60/59.94 Hz 1920 × 1035 interlaced	Non-50 Hz 1920 × 1080 interlaced	50 Hz 1920× 1080 interlaced	Non-50 Hz 1920 × 1080 progressive	50 Hz 1920× 1080 progressive	1280 × 720 progressive
equalizer test signal	first line	41 (field 2) 603 (field 2)	21 (field 1) 584 (field 2)	81 (field 1) 706 (field 2)	42	161	26
	last line (range)	295-302 (field 1)	287-293 (field 1)	347-504 (field 1)	578-585	696-703	382-389
		858-865 (field 2)	850-856 (field 2)	972-979 (field 2)			
	data values[1]	samples	samples	samples	samples	samples	samples
	300_h C_b	0 ... 3836	0 ... 3836	0 ... 3836	0 ... 3836	0 ... 3836	0 ... 2556
	198_h Y	1 ... 3837	1 ... 3837	1 ... 3837	1 ... 3837	1 ... 3837	1 ... 2557
	300_h C_r	2 ... 3838	2 ... 3838	2 ... 3838	2 ... 3838	2 ... 3838	2 ... 2558
	198_h Y	3 ... 3839	3 ... 3839	3 ... 3839	3 ... 3839	3 ... 3839	3 ... 2559
	polarity control word data value[1),2)] 190_h Y	(every other frame) line 41 sample 1	(every other frame) line 21 sample 1	(every other frame) line 81 sample 1	(every other frame) line 42 sample 1	(every other frame) line 161 sample 1	(every other frame) line 26 sample 1
phase locked loop test signal	first line (range)[3]	296-303 (field 1)	288-294 (field 1)	348-505 (field 1)	579-586	697-704	383-390
		859-866 (field 2)	851-857 (field 2)	973-980 (field 2)			
	last line	557 (field 1)	560 (field 1)	620 (field 1)			
		1120 (field 2)	1123 (field 2)	1245 (field 2)	1121	1245	745
	data values[1]	samples	samples	samples	samples	samples	samples
	200_h C_b	0 ... 3836	0 ... 3836	0 ... 3836	0 ... 3836	0 ... 3836	0 ...2556
	110_h Y	1 ... 3837	1 ... 3837	1 ... 3837	1 ... 3837	1 ... 3837	1 ...2557
	200_h C_r	2 ... 3838	2 ... 3838	2 ... 3838	2 ... 3838	2 ... 3838	2 ... 2558
	110_h Y	3 ... 3839	3 ... 3839	3 ... 3839	3 ... 3839	3 ... 3839	3 ... 2559

[1] The ordering of data values for each of the pairs of sample values may be reversed. If the ordering of the samples is reversed from the ordering in this table, then the polarity control word value is (200_h Y). (See 3.4.)

[2] The polarity change word is a substitution of the first active picture area Y sample, made in the first active picture line of every other frame (see 3.3).

[3] A range of line numbers for transitioning between the two test patterns is provided. The transition point within these ranges must be consistent across all fields (see clause 4).

<table>
<tr><td></td><td>vertical blanking interval</td></tr>
<tr><td rowspan="2">eav sav

horizontal blanking interval</td><td>first line of active picture

1st half of active field
300_h, 198_h
for equalizer testing [1)]</td></tr>
<tr><td>2nd half of active field
200_h, 110_h
for phase locked loop testing [1)]

last line of active picture</td></tr>
</table>

[1)] The ordering of data values for each of the pairs of sample values may be reversed (see 3.4).

Figure 1 – Serial digital interface checkfield

Annex A (informative)
Bibliography

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