RP 2006-2006

SMPTE RECOMMENDED PRACTICE

Solid State Media (SSM) Card Specification

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Approved
September 15, 2006

Foreword

SMPTE (the Society of Motion Picture and Television Engineers) is an internationally-recognized standards developing organization. Headquartered and incorporated in the United States of America, SMPTE has members in over 80 countries on six continents. SMPTE's Engineering Documents, including Standards, Recommended Practices and Engineering Guidelines, are prepared by SMPTE's Technology Committees. Participation in these Committees is open to all with a bona fide interest in their work. SMPTE cooperates closely with other standards-developing organizations, including ISO, IEC and ITU.

SMPTE Engineering Documents are drafted in accordance with the rules given in Part XIII of its Administrative Practices.

SMPTE Recommended Practice 2006 was prepared by Technology Committee V16.

1 Scope

This document defines the specification of the Solid State Media (SSM) Card. The physical specification provides the physical characteristics of the Card and the connector. The electrical interface between a host and the Card is a high performance bus and this document specifies the signal description, the electrical characteristics, and the bus operations. The register specification defines the registers for configuration and also defines the specific registers related to interrupt signals or commands. The command specification defines the commands for the bus master data transfer and the sensing log information written in the SSM Card in addition to the ATA commands. To guarantee the performance of the SSM Card, requirements for writing and reading speed are specified. The file system for the SSM Card is the FAT system.

2 Normative references

The following standards contain provisions, which, through reference in this text, constitute provisions of this standard. At the time of publication, the editions indicated were valid. All standards are subject to revision, and parties to agreements based on this standard are encouraged to investigate the possibility of applying the most recent edition of the standards indicated below.

ANSI INCTIS 361-2002, AT Attachment with Packet Interface -6 (ATA/ATAPI-6)

PCI Local Bus Specification Revision 3.0 (Note: The Bylaws of PCI-SIG (section 15) limit the RAND licensing terms to members.)

FAT: ISO/IEC 9293, Second Edition, 1994-1 l-l 5, Information Technology — Volume and File Structure of Disk Cartridges for Information Interchange

3 Symbols and abbreviations

For symbol definition and abbreviations, the reader is encouraged to study the PCI and ATA specifications. This document uses same terms defined in the mentioned standards and in other referenced documents.

ATA	AT Attachment
ATAPI	AT Attachment with Packet Interface
FAT	File Allocation Table
PCI	Peripheral Component Interconnect
PCI SIG	PCI Special Interest Group

The following symbols and abbreviations are defined in the Physical specification.

N	Newton
WPS	Write Protect Switch

The following symbols and abbreviations are defined in the Electrical specification.

LV	Low Voltage
Vcc	Power
Vpp	Programming and peripheral voltages
GND	Ground
Agent	All devices which relates to a data transfer on the bus
Master	Device which drives the address bus and sends a command
Slave	Device which receives a command and responses to it
Assert	Set a signal active
Negate	Set a signal inactive
CCD	(SSM) Card Card Detect
CVS	(SSM) Card Voltage Sense
CCLK	(SSM) Card Clock which provides timing for all transactions
CAD	(SSM) Card Address and Data multiplexed bus - During the address phase, CAD contain a byte address. During the data phase CAD contain data.
CCBE	(SSM) Card Command and Bus Enables multiplexed bus — During the address phase CCBE are defined as bus Command. During the data phase, CCBE are used as Byte Enables.
CCLKRUN#	(SSM) Card Clock Request/Status
CDEVSEL#	(SSM) Card Device Select
CFRAME#	(SSM) Card Cycle Frame - While CFRAME# is asserted, data transfers continue.
CGINT	(SSM) Card Grant
CINT#	(SSM) Card Interrupt request
CIRDY#	(SSM) Card Initiator Ready
CPAR#	(SSM) Card Even Parity
CPERR#	(SSM) Card Parity Error
CREQ#	(SSM) Card Request
CRST#	(SSM) Card Reset
CSERR#	(SSM) Card System Error
CSTOP#	(SSM) Card Stop transaction
CTRDY#	(SSM) Card Target ready
Transaction	Bus cycle which is initiated by an address phase and is followed by data phases.

NOTE – The acronym “C” stands for (SSM) Card.

The following symbols and abbreviations are defined in the Register specification.

ABRT	Abort – Indicates the requested command has been aborted
BIST	Built-in Self Test
BSY	Busy – Indicates if a device is busy
DEV	Device select
DRDY	Device Ready
DRQ	Data Request – Indicates if data transfer is ready between a device and a host
EOT	End of Table
ERR	Error – Indicates an error occurred during execution of the previous command
IDNF	ID not found
INTA#	Interrupt A – used to request an interrupt
IRQ	Interrupt request bit which represents an INTRQ signal
IRQE	Interrupt request enable bit for IRQ
INTRQ	Interrupt request signal
nIEN	Enable bit for INTRQ signal
LBA	Logical Block Addressing – Addressing by the linear mapping of sectors
PIO	Programmed Input/Output
RO	Read only
Res	Reserved
R/W	Read/Write
WO	Write only
scatter/gather	Gathering scattered data from memory for transmission
SRST	Software Reset
UNC	Uncorrectable

The following symbols and abbreviations are defined in the Command specification.

CID	Card ID
CSD	Card Specific Data
DMA	Direct Memory Access

4 Introduction

Figure 4.1 shows the overall structure of the SSM Card specification and the relationship between the other reference documents and this document.

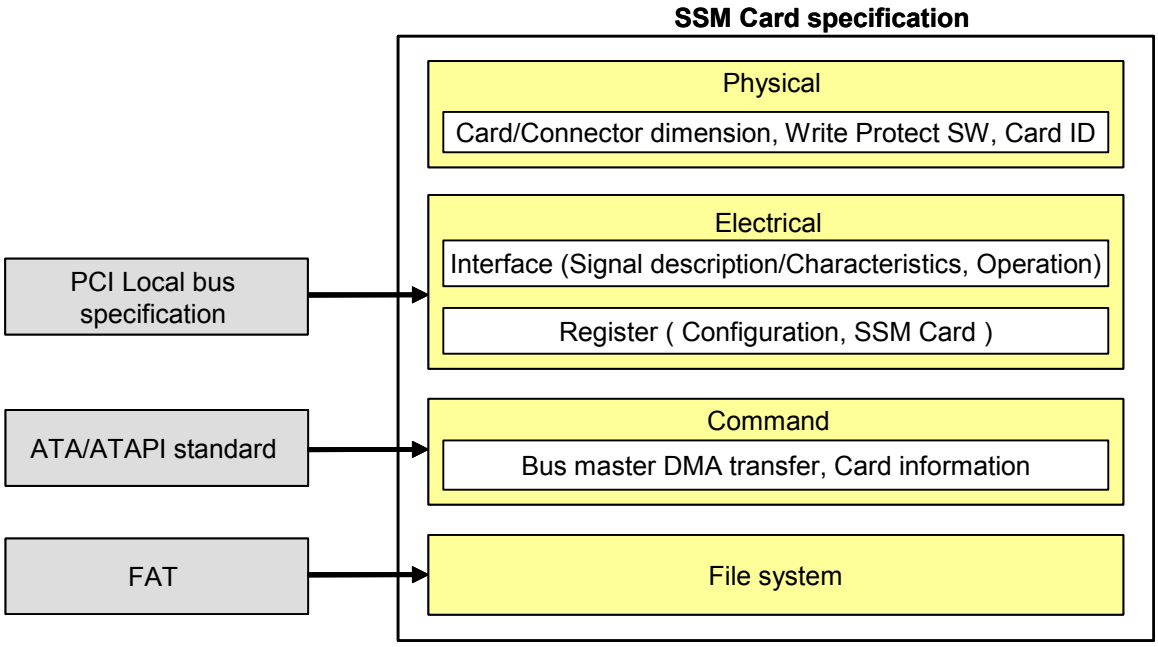


Figure 4.1 – Structure of SSM Card specification and relation between Reference documents

The physical specification defines the Card package dimensions, the Card connector, the write protect switch for protection of files stored on the SSM Card and the Card ID to identify the SSM Card.

The electrical interface of the SSM Card is a high performance 32 bit bus with multiplexed address and data lines. This document specifies the signal descriptions, the electrical characteristics and the bus operations of this SSM Card.

The register specification defines the Configuration space registers to identify or control the SSM Card and also defines the specific registers related to interruption or commands.

The command specifications define the commands required for the SSM Card. Write protection and power management are performed using ATA commands as unique functions for the SSM Card. Data transmission between a SSM Card and a host is performed using the Bus Master DMA transfer commands. After a read or write command is issued from the host, the SSM Card takes initiative of bus control and performs data transfers as the bus master. Furthermore, the commands for sensing log information written in the SSM Card are specified.

To guarantee the performance of the SSM Card, the writing and reading speeds required for the SSM Card are specified.

The SSM Card uses the FAT file system.

5 Physical specification

5.1 Card dimensions, socket configuration and pin numbering

Figure 5.1 specifies Card package dimensions. Figure 5.2 defines configuration of Card socket contacts and a relative pin contact locations, Figure 5.3 defines the pin connector layout and Figure 5.4 defines the pin connector dimensions.

5.2 Write Protect Switch and Card ID

The SSM Card shall be equipped with a Write Protect Switch (WPS) and Card Identification (Card ID).

The Write Protect Switch shall be located at the approximate position as shown in Figure 5.1. The status of the Write Protect Switch should be sensed by a host with the IDENTIFY DEVICE command (See 8.2) so that the host can perform the write protection functionality depending on the status of the Write Protect Switch.

The Card ID shall be located at the approximate position as shown in Figure 5.1.

5.3 Card Connector

The socket contacts on the SSM Card shall be located as specified in Figure 5.2.

The Card connector socket layout shall match the host pin-connector layout as shown in Figure 5.3.

The Card connector shall contain a top side planer, electrically conductive, ground plate with eight raised dimples 0.5 mm height as shown in Figure 5.4.

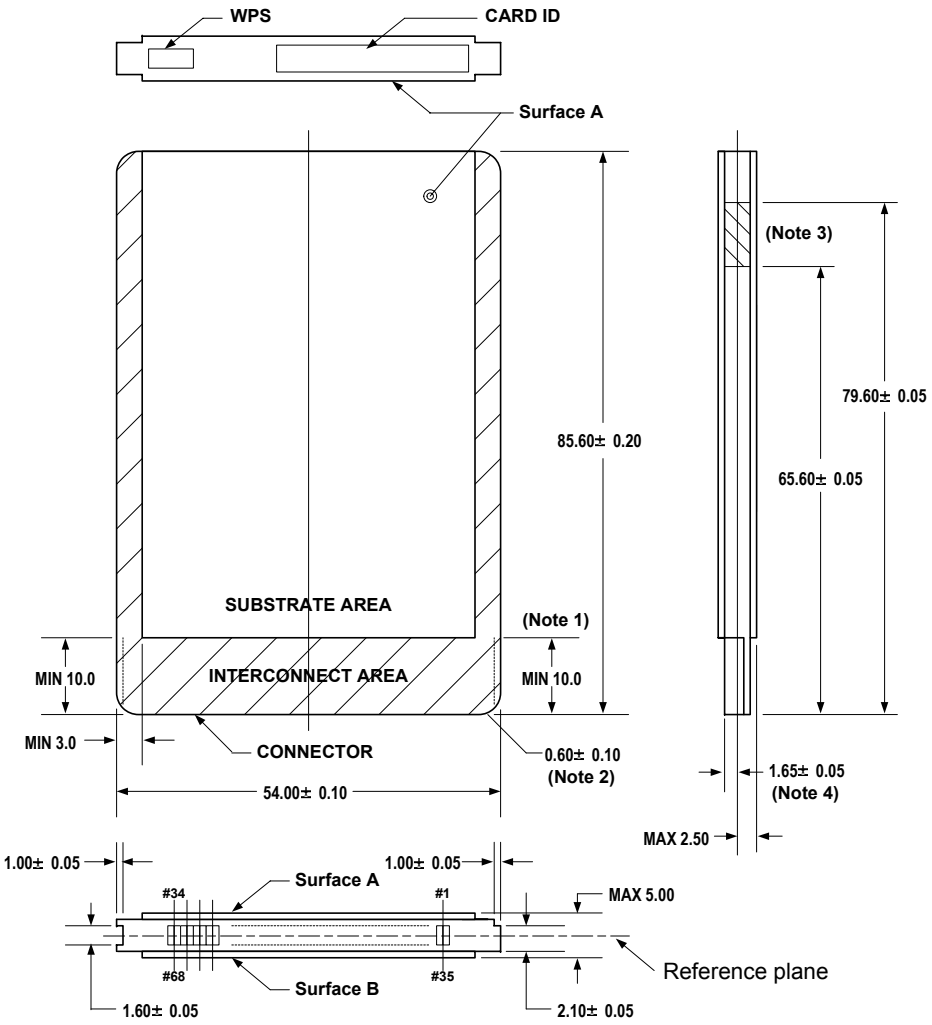
The mechanical and electrical performance of the Card connector shall be as specified in Table 5.1.

Table 5.1 – Mechanical and electrical performance

Item	Specification
Insertion Force	39.2 N maximum at speed of 25 mm/minute
Pulling Force	6.67 N minimum and 39.2 N maximum at speed of 25 mm/minute
Contact Resistance	Initially 40 mΩ maximum and 20 mΩ maximum change at voltage of 20 mV and current of 1 mA

5.4 Labeling

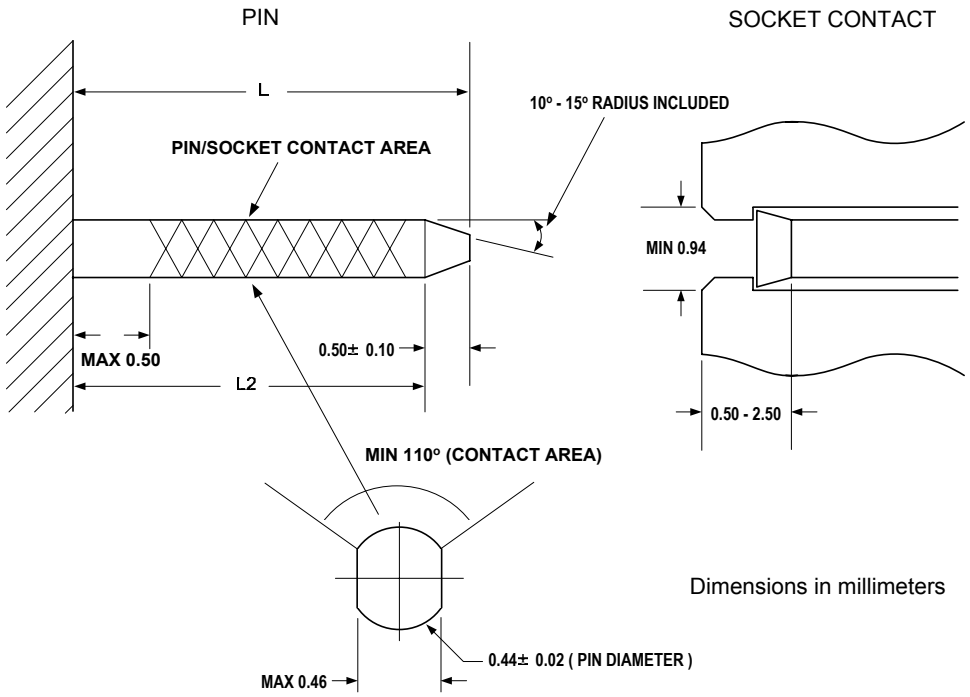
If a label is attached on surface A and/or surface B of a SSM Card, the thickness of the Card including the labels shall not exceed the thickness specified in Figure 5.1.



Dimensions in millimeters

Note 1 - Polarization key length
Note 2 - Dimension R corner radius
Note 3 - Ground clip location
Note 4 - Dimension is increased by 0.50± 0.05 mm over dimples

Figure 5.1 – SSM Card Package Dimensions



	L	L2
Power	5.00± 0.1	REF 4.50
General	4.25± 0.1	REF 3.75
Detect	3.50± 0.1	REF 3.00

Figure 5.2 – SSM Card Socket Configuration

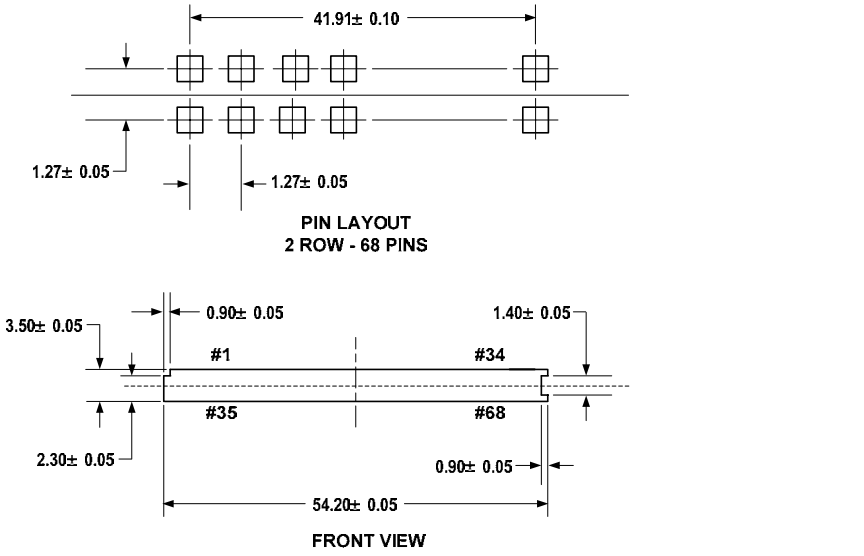


Figure 5.3 – SSM Card Pin Connector layout

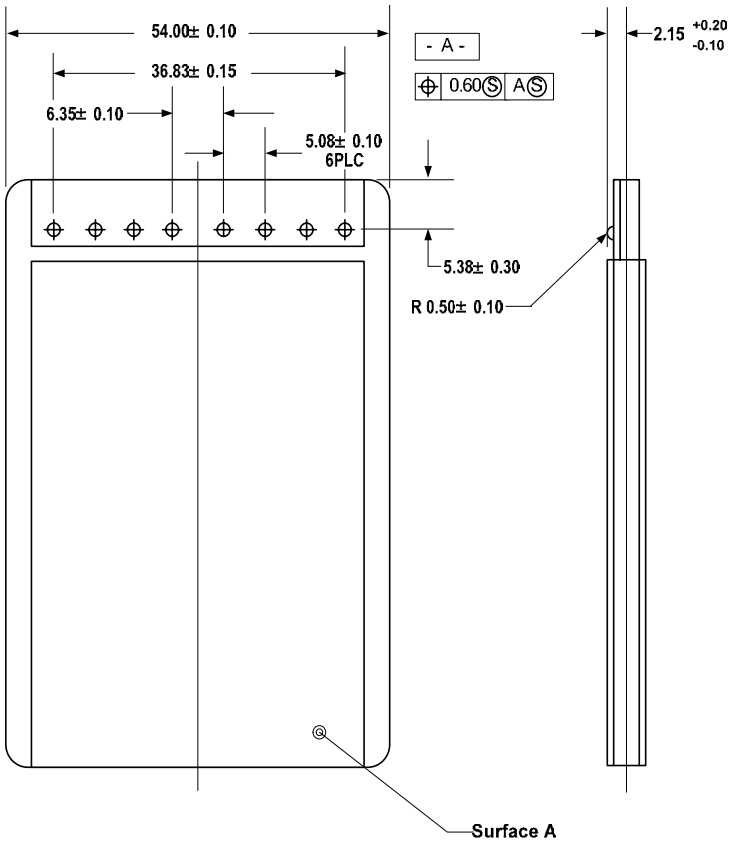


Figure 5.4 – SSM Card Pin Connector Dimensions

6 Electrical specification

6.1 Overview

This section defines the electrical specification of the SSM Card. The electrical interface of the SSM Card is a 32 bit high performance bus (SSM Card bus) with multiplexed address and data lines. The SSM Card bus specifies Card pin assignment and its signal definitions, Card detection mechanism, Electrical characteristics, Timing parameters and Bus operations.

NOTE – The bit order of the 32 bit bus shall follow the convention where bit 0 is LSB and bit 31 is MSB. Multi byte values are represented with little endian, the least significant byte first.

6.2 Signal Description

6.2.1 Pin assignment

The pin assignment of the SSM Card bus shall be as defined in Table 6.1.

Note: The name of the pins is the same as the PCI bus signal name when the first character "C" is deleted. The differences in the signals are summarized as follows:

- Card Detect pins and Voltage Sense pins are added.
- There is no IDSEL (Initialization Device Select) pin.
- There is only one interrupt pin (CINT#).
- A clock control signal (CCLKRUN#) is added.

Table 6.1 – SSM Card pin assignment

Pin	Signal	I/O	Signal type	Pin	Signal	I/O	Signal type
1	**GND**	**DC**		35	**GND**	**DC**	
2	**CAD[0]**	**I/O**	**h/z**	36	**CCD1#**	**Output**	
3	**CAD[1]**	**I/O**	**h/z**	37	**CAD[2]**	**I/O**	**h/z**
4	**CAD[3]**	**I/O**	**h/z**	38	**CAD[4]**	**I/O**	**h/z**
5	**CAD[5]**	**I/O**	**h/z**	39	**CAD[6]**	**I/O**	**h/z**
6	**CAD[7]**	**I/O**	**h/z**	40	**Reserved**		
7	**CCBE[0]#**	**I/O**	**h/z**	41	**CAD[8]**	**I/O**	**h/z**
8	**CAD[9]**	**I/O**	**h/z**	42	**CAD[10]**	**I/O**	**h/z**
9	**CAD[11]**	**I/O**	**h/z**	43	**CVS[1]**	**I/O**	
10	**CAD[12]**	**I/O**	**h/z**	44	**CAD[13]**	**I/O**	**h/z**
11	**CAD[14]**	**I/O**	**h/z**	45	**CAD[15]**	**I/O**	**h/z**
12	**CCBE[1]#**	**I/O**	**h/z**	46	**CAD[16]**	**I/O**	**h/z**
13	**CPAR**	**I/O**	**h/z**	47	**Reserved**		
14	**CPERR#**	**I/O**	**s/h/z**	48	**Reserved**		
15	**CGNT#**	**Input**		49	**CSTOP#**	**I/O**	**s/h/z**
16	**CINT#**	**Output**	**0/d**	50	**CDEVSEL#**	**I/O**	**s/h/z**
17	**Vcc**	**DC in**		51	**Vcc**	**DC in**	
18	**Vpp**	**DC in**		52	**Vpp**	**DC in**	
19	**CCLK**	**Input**		53	**CTRDY#**	**I/O**	**s/h/z**
20	**CIRDY#**	**I/O**	**s/h/z**	54	**CFRAME#**	**I/O**	**s/h/z**
21	**CCBE[2]#**	**I/O**	**h/z**	55	**CAD[17]**	**I/O**	**h/z**
22	**CAD[18]**	**I/O**	**h/z**	56	**CAD[19]**	**I/O**	**h/z**
23	**CAD[20]**	**I/O**	**h/z**	57	**CVS[2]**	**I/O**	
24	**CAD[21]**	**I/O**	**h/z**	58	**CRST#**	**Input**	
25	**CAD[22]**	**I/O**	**h/z**	59	**CSERR#**	**Output**	**o/d**
26	**CAD[23]**	**I/O**	**h/z**	60	**CREQ#**	**Output**	**h/z**
27	**CAD[24]**	**I/O**	**h/z**	61	**CCBE[3]#**	**I/O**	**h/z**
28	**CAD[25]**	**I/O**	**h/z**	62	**Reserved**		
29	**CAD[26]**	**I/O**	**h/z**	63	**Reserved**		
30	**CAD[27]**	**I/O**	**h/z**	64	**CAD[28]**	**I/O**	**h/z**
31	**CAD[29]**	**I/O**	**h/z**	65	**CAD[30]**	**I/O**	**h/z**
32	**Reserved**			66	**CAD[31]**	**I/O**	**h/z**
33	**CCLKRUN#**	**I/O**	**o/d**	67	**CCD[2]#**	**Output**	
34	**GND**	**DC**		68	**GND**	**DC**	

I/O: Input/Output, h/z: Tri-state, s/h/z :Sustained Tri-State, o/d : Open drain, # : Low active

NOTE – Sustained Tri-State is an active low tri-state signal owned and driven by one and only one agent at a time. The detailed information is described in the PCI Local Bus Specification section 2.1.

6.2.2 Signal/Pin Description

6.2.2.1 Power and Ground pins

· Vcc

Vcc of the SSM Card shall be 3.3V ± 0.3V Voltage.

· Vpp

The voltage of the **Vpp** pin shall be the same voltage as the **Vcc** pin.

6.2.2.2 Interface Configuration pins

· CCD[2::1]#

CCD[2::1]# are the Card Detect pins that provide a means for sockets to detect the Card insertion and removal events. **CCD[2::1]#** pins are at opposite ends of the connector to ensure a valid insertion.

· CVS[2::1]#

CVS[2::1]# are in conjunction with **CCD[2::1]#** and used to encode card type information.

NOTE – See section 6.3 for details.

6.2.2.3 System pins

· CCLK

CCLK provides timing for all transactions on the SSM Card bus interface and is an input to every SSM Card bus device. All other SSM Card bus signals, except **CRST#** (upon assertion), **CCLKRUN#**, **CINT#**, **CCD[2::1]#**, and **CVS[2::1]**, are sampled on the rising edge of **CCLK**, and all timing parameters are defined with respect to this edge. The maximum frequency of **CCLK** shall be 33MHz. The clock may be stopped in the low state.

· CCLKRUN#

CCLKRUN# is a signal to control the clock and is used by Cards to request starting (or speeding up) the SSM Card bus clock, **CCLK**. **CCLKRUN#** also indicates the clock status. For SSM Cards, **CCLKRUN#** is an open drain output and also an input. For the host system, **CCLKRUN#** is a Sustained High-Z state I/O signal. The SSM Card does not support **CCLKRUN#**.

· CRST#

CRST# is used to bring SSM Card bus specific registers, sequencers, and signals to a consistent state. **CRST#** affects the reset states of required SSM Card configuration registers. Anytime **CRST#** is asserted, all SSM Card bus output signals shall be a High-Z state. **CSERR#**, **CINT#**, and **CCLKRUN#** (open drain) are floated. **CREQ#** shall be in a High-Z state (it cannot be driven low or high during reset). **CGNT#** must be negated. To prevent **CAD[31::00]**, **CCBE[3::0]#**, and **CPAR** signals from floating during reset, the central resource may drive these lines during reset but only to a low voltage level, they may not be driven high. **CVS[2::1]** shall be driven low. The states of **CCD[2::1]#** are not affected by **CRST#**. Negation of **CRST#** is synchronous to **CCLK**, but assertion of **CRST#** is not synchronous to **CCLK.**

NOTE – See section 6.2.3 for clock and signal timing details.

6.2.2.4 Address and Data pins

- **CAD[31::00]**

  Address and Data are multiplexed in **CAD[31::00]** on the same SSM Card bus pins. A bus transaction shall consist of an address phase followed by one or more data phases. The SSM Card bus shall support both read and write bursts. The address phase is the clock cycle in which **CFRAME#** is asserted. During the address phase, **CAD[31::00]** contain a byte address for I/O and contain a 4 byte address for configuration and memory. During data phases, **CAD[07::00]** contain the least significant byte (LSB) and **CAD[31::24]** contain the most significant byte (MSB). Write data is stable and valid when **CIRDY#** is asserted. Read data is stable and valid when **CTRDY#** is asserted. Data is transferred during those clocks where both **CIRDY#** and **CTRDY#** are asserted.

- **CCBE[3::0]#**

  Command and Byte Enables are multiplexed in **CCBE[3::0]#** on the same SSM Card bus pins. During the address phase of a transaction, **CCBE[3::0]#** define the bus command (see 6.4.2 for bus command definitions). During the data phase, **CCBE[3::0]#** are used as Byte Enables. The Byte Enables are valid for the entire data phase and determine which byte lanes carry meaningful data. **CCBE[0]#** applies to **CAD[07::00]** (LSB) and **CCBE[3]#** applies to **CAD[31::24]** (MSB).

NOTE – See section 6.4.2 for details.

6.2.2.5 Interface Control Pins

- **CFRAME#**

  CFRAME# is driven by the current master to indicate the beginning and duration of a transaction. **CFRAME#** is asserted to indicate that a bus transaction is beginning. While **CFRAME#** is asserted, data transfers continue. When **CFRAME#** is negated, the transaction is in the final data phase.

- **CIRDY#**

  CIRDY# indicates the initiating agent's (bus master's) ability to complete the current data phase of the transaction. **CIRDY#** is used in conjunction with **CTRDY#**. A data phase is completed on any clock both **CIRDY#** and **CTRDY#** are sampled asserted. During a write, **CIRDY#** indicates that valid data is present on **CAD[31::00]**. During a read, it indicates the master is prepared to accept data. Wait cycles are inserted until both **CIRDY#** and **CTRDY#** are asserted together.

- **CTRDY#**

  CTRDY# indicates the agent's (selected target's) ability to complete the current data phase of the transaction. **CTRDY#** is used in conjunction with **CIRDY#**. A data phase is completed on any clock both **CTRDY#** and **CIRDY#** are sampled asserted. During a read, **CTRDY#** indicates that valid data is present on **CAD[31::00]**. During a write, **CTRDY#** indicates the target is prepared to accept data. Wait cycles are inserted until both **CIRDY#** and **CTRDY#** are asserted together.

- **CSTOP#**

  CSTOP# indicates the current target is requesting the master to stop the current transaction.

- **CDEVSEL#**

  CDEVSEL#, when actively driven, indicates the driving device has decoded its address as the target of the current access. As an input, **CDEVSEL#** indicates whether any device on the bus has been selected.

NOTE – The timing parameters are defined in section 6.4.2.1 and 6.4.2.2.

6.2.2.6 Arbitration Pins (Bus Masters Only)

- **CREQ#**

  CREQ# indicates to the arbiter that this agent desires use of the bus. Every master has its own **CREQ#**.

- **CGNT#**

  CGNT# indicates to the agent that access to the bus has been granted. Every master has its own **CGNT#**.

6.2.2.7 Error Reporting Pins

- **CPAR**

  CPAR is even parity across **CAD[31::00]** and **CCBE[3::0]#**. Parity generation is required by all SSM Card bus agents. **CPAR** is stable and valid one clock after the address phase. For the data phases **CPAR** is stable and valid one clock after either **CIRDY#** is asserted on a write transaction or **CTRDY#** is asserted on a read transaction. Once **CPAR** is valid, it remains valid until one clock after the completion of the current data phase. (**CPAR** has the same timing as **CAD[31::00]** but delayed by one clock.) The master drives **CPAR** for address and write data phases; the target drives **CPAR** for read data phases.

- **CPERR#**

  CPERR# is used for reporting of data parity errors during all SSM Card bus transactions. The **CPERR#** pin is sustained tri-state and shall be driven active by the agent receiving data two clocks following the data when a data parity error is detected. The minimum duration of **CPERR#** is one clock for each data phase that a data parity error is detected. If sequential data phases each have a data parity error, the **CPERR#** signal asserts for more than a single clock. **CPERR#** shall be driven high for one clock before being tri-stated as with all sustained tri-state signals. There are no special conditions when a data parity error may be lost or when reporting of an error may be delayed. An agent cannot report a **CPERR#** until it has claimed the access by asserting **CDEVSEL#** and completed a data phase.

- **CSERR#**

  CSERR# is used for reporting system errors where the result could be catastrophic. **CSERR#** is a pure open drain and is actively driven for a single SSM Card bus clock by the agent reporting the error. The assertion of **CSERR#** is synchronous to the clock and meets the setup and hold times of all bused signals. However, the restoring of **CSERR#** to the negated state is accomplished by a weak pull-up (same value as used for s/h/z) which is provided by the system designer and not by the signaling agent or central resource. This pull-up may take two to three clock periods to fully restore **CSERR#**. The agent that reports **CSERR#**s to the operating system does so anytime **CSERR#** is sampled asserted.

NOTE – See section 6.4.3 for details.

6.2.2.8 Interrupt Request Pin

- **CINT#**

  CINT# is an optional signal which is defined as level sensitive, and asserted low (negative true), using an open drain output driver. The assertion and negation of **CINT#** is asynchronous to **CCLK**. The device driver may not make any assumptions about interrupt sharing. All SSM Card bus device drivers shall be able to share an interrupt (chaining) with any other logical device, including functions on the same multifunction card.

NOTE – See section 7.3.1 and 7.3.2 for details.

6.2.3 Electrical Characteristics and Timing Parameters

6.2.3.1 Clock Specification

The clock specification of the SSM Card bus is given in Figure 6.1 and Table 6.2.

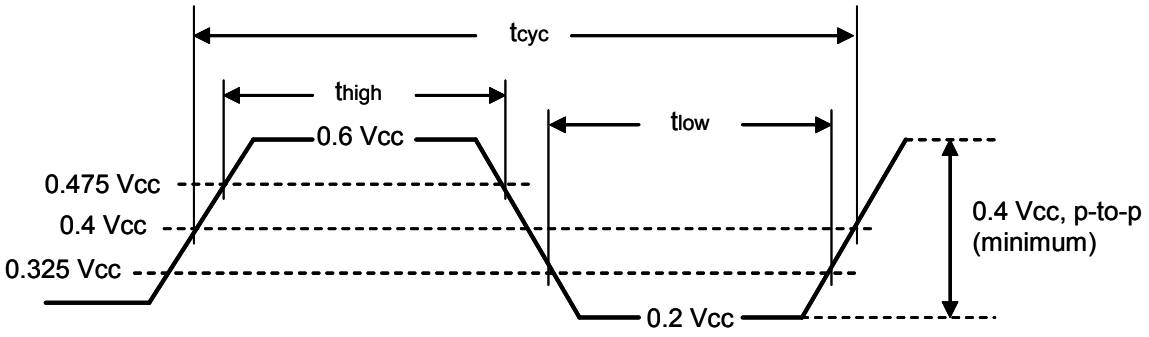


Figure 6.1 – Clock Waveform

Table 6.2 – SSM Card Clock Specification

Symbol	Parameter	Min	Max	Units
tcyc	CCLK Cycle Time	30		ns
thigh	CCLK High Time	12		ns
tlow	CCLK Low Time	12		ns
-	CCLK Slew Rate	1	4	V/ns

6.2.3.2 Timing Parameter

The input and output timing between CCLK and signals are illustrated in Figure 6.2 and Figure 6.3. Timing parameters and condition parameters are given in Table 6.3 and Table 6.4 respectively.

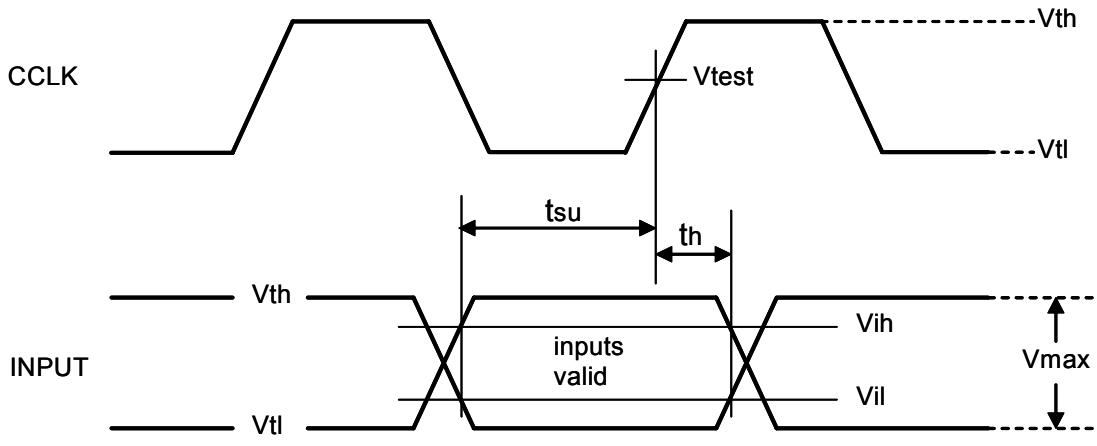


Figure 6.2 – Input signal Timing

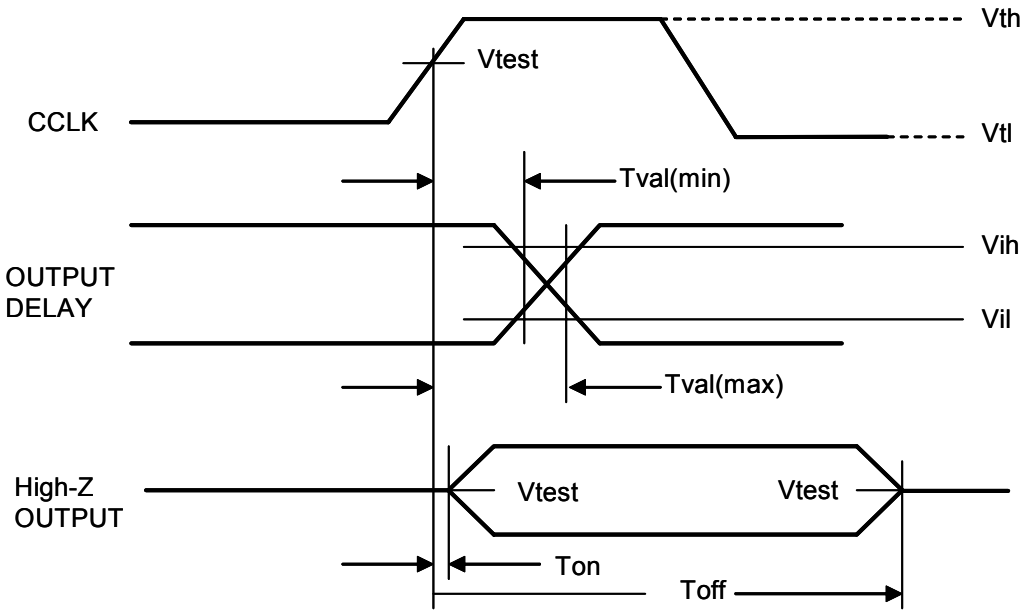


Figure 6.3 – Output signal Timing

Table 6.3 – Timing Parameters

Symbol	Parameter	Min	Max	Units
tval	CCLK to signal valid delay	2	18	ns
ton	Float to active delay	2		ns
toff	Active to float delay		28	ns
tsu	Input set up time to CCLK	7		ns
th	Input hold time from CCLK	0		ns
trst	Reset active time after power stable	1		ms
trst-clk	Reset active time after CCLK stable	100		clocks
trst-off	Reset active to output float delay		40	ns

Table 6.4 – 3.3V Condition parameters

Symbol	3.3 V Signaling	Units
Vth	0.6 Vcc	V
Vtl	0.2 Vcc	V
Vih	0.475 Vcc	V
Vil	0.325 Vcc	V
Vtest	0.4 Vcc	V
Vmax	0.4 Vcc	V

6.3 Card Type Detection Mechanism

The card type shall be detected before the socket notifies Card Services of an insertion event. Card Detect and Voltage Sense Connections for the SSM Card shall be as defined in Table 6.5. The Card type of the SSM Card shall be determined by detecting that CCD2# is connected to Ground, CVS2 is open, and CCD1# is connected to CVS1.

Table 6.5 – Card Detect and Voltage Sense Connections

CCD2# (pin 67)	CCD1# (pin 36)	CVS2 (pin 57)	CVS1 (pin 43)	Card Type		
				Interface	Vcc	Vpp
Ground	Connect to CVS1	Open	connect to CCD1#	SSM Card bus	3.3 V	3.3 V

A valid SSM Card insertion shall be detected when both **CVS[2::1]** pins are low. Therefore, sockets shall always drive their **CVS[2::1]** outputs low when a SSM Card is removed. Once a valid insertion is detected and before power is applied, the socket shall interrogate the SSM Card to detect if **CCD[1]#** pin is connected to **CVS[1]** pin by alternately driving each **CVS[2::1]** output high and monitoring what happens to the **CCD[2::1]#** and **CVS[2::1]** inputs. At the completion of this interrogation, the socket shall again drive the **CVS[2::1]** pins low.

6.4 SSM Card bus operation

6.4.1 Bus Command

Bus Commands shall be encoded on the **CCBE[3::0]#** lines during the address phase. The Bus Command encodings and types shall be as given in Table 6.6, where "1" indicates a high voltage and "0" indicates a low voltage. Byte Enables shall be asserted when their value is 0.

Table 6.6 – Bus Commands

CCBE[3::0]#	Command type
0 0 0 0	Allocated
0 0 0 1	Special cycle
0 0 1 0	I/O Read
0 0 1 1	I/O Write
0 1 0 0	Reserved
0 1 0 1	Reserved
0 1 1 0	Memory Read
0 1 1 1	Memory Write
1 0 0 0	Reserved
1 0 0 1	Reserved
1 0 1 0	Configuration Read
1 0 1 1	Configuration Write
1 1 0 0	Memory Read multiple
1 1 0 1	Allocated
1 1 1 0	Memory Read Line
1 1 1 1	Memory Write and Invalidate

The SSM Card shall respond as a target to the Configuration read and the Configuration write commands. Responses to the other commands are optional.

- **Allocated**

  This command shall not be used.

- **Special Cycle command**

  The Special Cycle command shall be used to send the same message to multiple devices on the bus and provides a simple message broadcast mechanism on the SSM Card bus. It is designed to be used as an alternative to physical signals when sideband communication is necessary.

NOTE – The detailed specification of the Special Cycle is described in the PCI Local Bus Specification section 3.6.2.

- **I/O Read command**

  The I/O Read command shall be used to read data from an agent mapped in I/O address space. **CAD[31::00]** provide the read address and all 32 bits shall be decoded to create the read address value. The Byte Enables indicate the size of the transfer and shall be consistent with the byte address.

- **I/O Write command**

  The I/O Write command shall be used to write data to an agent mapped in I/O address space. **CAD[31::00]** provide the write address and all 32 bits shall be decoded to create the write address value. The Byte Enables indicate the size of the transfer and shall be consistent with the byte address.

- **Reserved command**

  These commands are reserved for future use.

- **Memory Read command**

  The Memory Read command shall be used to read data from an agent mapped in the memory address space. The target is free to do an anticipatory read for this command only if it can guarantee that such a read has no side effects. Furthermore, the target must ensure the coherency (which includes ordering) of any data retained in temporary buffers after this SSM Card bus transaction is completed. Such buffers must be invalidated before any synchronization events (e.g., updating an I/O Status register or memory flag) are passed through this access path.

- **Memory Write command**

  The Memory Write command shall be used to write data to an agent mapped in the memory address space. When the target returns "ready," it has assumed responsibility for the coherency (which includes ordering) of the subject data. This can be done either by implementing this command in a fully synchronous manner, or by insuring any software transparent posting buffer may be flushed before synchronization events (e.g., updating an I/O Status register or memory flag) are passed through this access path. This implies that the master is free to create a synchronization event immediately after using this command.

- **Configuration Read command**

  The Configuration Read command shall be used to read the configuration space of each agent. An agent shall be selected when its **CFRAME#** signal is asserted and **CAD[1::0]** are 00. During the address phase of a configuration cycle, **CAD[7::2]** address one of the 64 4-byte-registers (where ‘byte enables’ address the byte(s) within each 4 byte group) in the configuration space of each device and **CAD[31::11]** are logical don't cares. **CAD[10::08]** indicate which device of a multi-function agent is being addressed.

- **Configuration Write command**

  The Configuration Write command is used to transfer data to the configuration space of each agent. An agent is selected when the **CFRAME#** signal is asserted and **CAD[1::0]** are 00. During the address phase of a configuration cycle, the **CAD[7::2]** address one of the 64 4-byte-registers (where byte enables address the byte(s) within each 4 byte group) in the configuration space of each device and **CAD[31::11]** are logical don't cares. **CAD[10::08]** indicate which device of a multi-function agent is being addressed.

- **Memory Read Multiple command**

  The Memory Read Multiple command shall be semantically identical to the Memory Read command except that it additionally indicates that the master may intend to fetch more than one cache line before disconnecting. The memory controller should continue pipelining memory requests as long as **CFRAME#** is asserted. This command is intended for use with bulk sequential data transfers where the memory system (and the requesting master) might gain some performance advantage by sequentially reading ahead an additional cache line when a software transparent buffer is available for temporary storage.

- **Memory Read Line command**

  The Memory Read Line command shall be semantically identical to the Memory Read command except that it additionally indicates that the master intends to complete more than two SSM Card bus data phases. This command is intended for use with bulk sequential data transfers where the memory system (and the requesting master) might gain some performance advantage by reading up to a cache line boundary in response to the request rather than a single memory cycle. As with the Memory Read command, pre-fetched buffers must be invalidated before any synchronization events are passed through this access path.

- **Memory Write and Invalidate command**

  The Memory Write and Invalidate command shall be semantically identical to the Memory Write command except that it additionally guarantees a minimum transfer of one complete cache line; i.e., the master intends to write all bytes within the addressed cache line in a single SSM Card bus transaction. The master may allow the transaction to cross a cache line boundary only if it also intends to transfer the entire next line. This command requires implementation of a configuration register in the master indicating the cache line size. A target containing memory that might be cacheable by the host system is also required to implement the Cache Line Size register. The target containing cacheable memory must accept a full cache line before disconnecting the transaction if it completes the first data phase. This command allows a memory performance optimization by invalidating a dirty line in a write-back cache without requiring the actual write-back cycle, thus shortening access time.

6.4.2 Bus Transactions

Bus transactions shall be initiated by an address phase and followed by data phases.

NOTE – The detailed specification of Bus transactions is described in the PCI Local Bus Specification section 3.3

6.4.2.1 Read Transaction

Figure 6.4 illustrates the timing diagram of read transaction. The read transaction shall start with the address phase which occurs when **CFRAME#** is asserted for the first time. During the address phase **CAD[31::00]** contain a valid address and **CCBE[3::0]#** contain a valid bus command.

The first clock of the first data phase shall be clock 3. During the data phase, **CCBE#** indicates which byte lanes are involved in the current data phase. A data phase may consist of a data transfer and wait cycles. The **CCBE#** output buffers shall remain enabled from the first clock of the data phase through the end of the transaction. This ensures **CCBE#** pins are not left floating for long intervals.

The first data phase on a read transaction requires a turnaround-cycle (enforced by the target via **CTRDY#**) to avoid contention when one agent stops driving a signal and another agent begins driving the signal. In this case the address is valid on clock 2 and then the master stops driving **CAD**. The earliest the target can provide valid data is clock 4. The target shall drive the **CAD** lines following the turnaround cycle when **CDEVSEL#** is asserted. Once enabled, the output buffers shall stay enabled through the end of the transaction.

In the data phase, data shall be transferred when both **CIRDY#** and **CTRDY#** are asserted on the same clock edge. (**CTRDY#** cannot be driven until **CDEVSEL#** is asserted.) When either is negated, a wait cycle is inserted and no data shall be transferred. As illustrated in the diagram, data should be successfully transferred on clocks 4, 6, and 8, and wait cycles are inserted on clocks 3, 5, and 7. The first data phase completes in the minimum time for a read transaction. The second data phase shall be extended on clock 5 because **CTRDY#** is negated. The last data phase shall be extended because **CIRDY#** was negated on clock 7.

The master knows at clock 7 that the next data phase is the last. However, because the master is not ready to complete the last transfer (**CIRDY#** is negated on clock 7), **CFRAME#** stays asserted. Only when **CIRDY#** is asserted can **CFRAME#** be negated, which occurs on clock 8.

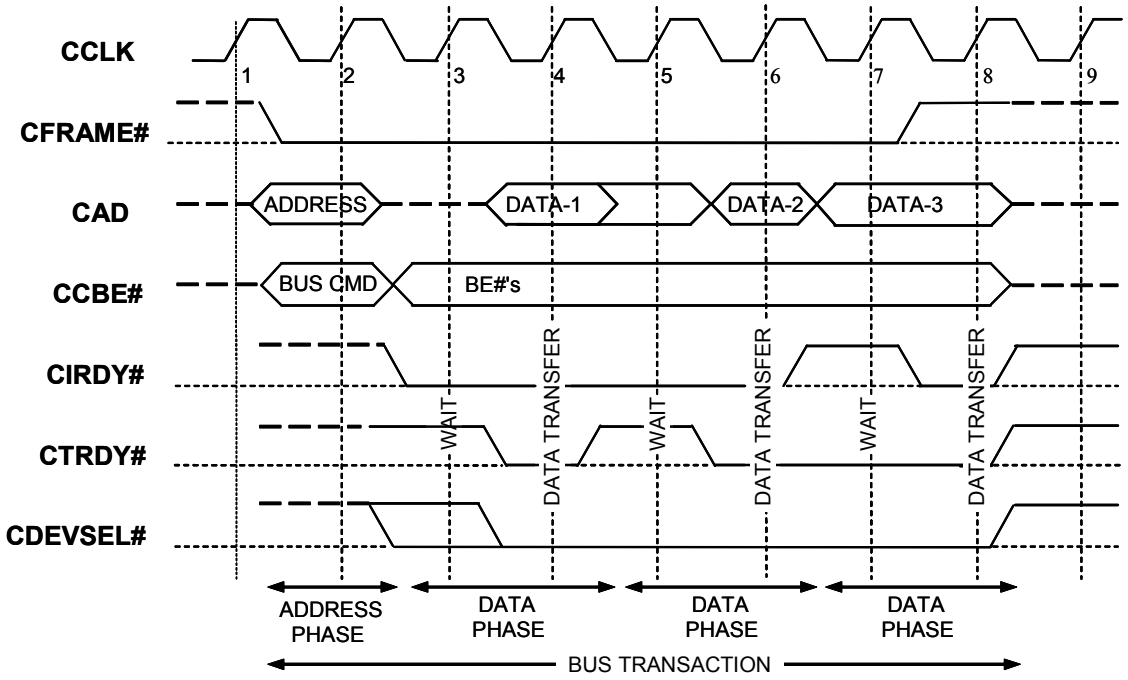


Figure 6.4 – Timing of Read Transaction

6.4.2.2 Write Transaction

Figure 6.5 illustrates the timing diagram of write transaction. The write transaction shall start when **CFRAME#** is asserted for the first time which occurs on clock 2. The write transaction shall be the same as the read transaction except no turnaround cycle is required following the address phase because the master provides both address and data. Data phases shall be the same for both read and write transactions.

The first and second data phases complete with zero wait cycles. However, the third data phase has three wait cycles inserted by the target. **CIRDY#** shall be asserted when **CFRAME#** is negated indicating the last data phase. The data transfer was delayed by the master on clock 5 because **CIRDY#** was negated. Although this allowed the master to delay data, it did not allow the byte enables to be delayed. The last data phase is signaled by the master on clock 6, but does not complete until clock 8.

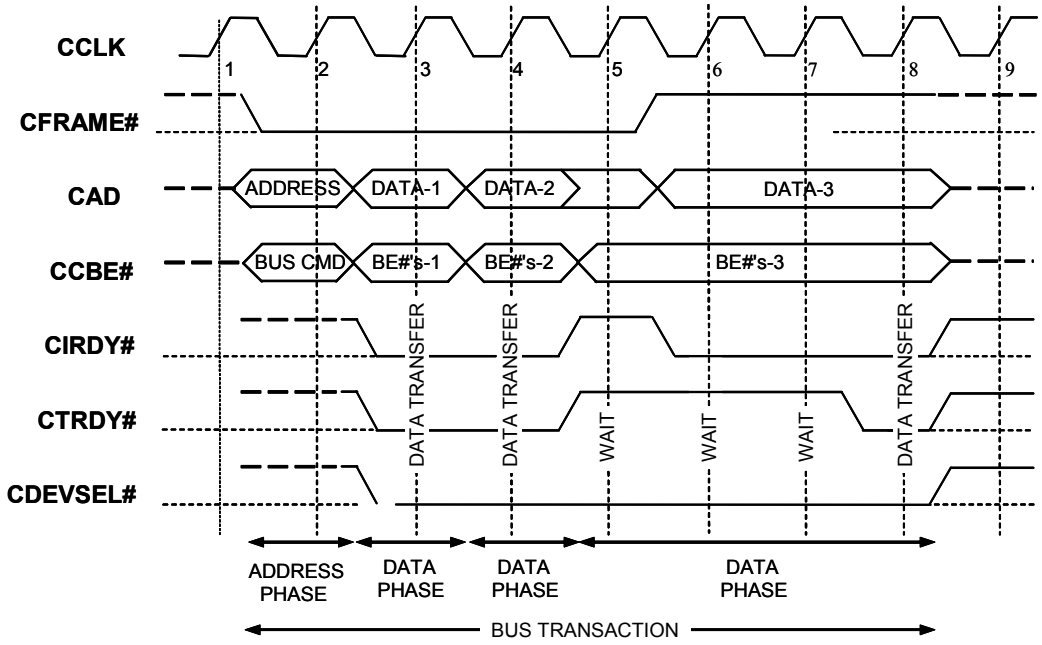


Figure 6.5 – Timing of Write Transaction

6.4.3 Error Functions

Figure 6.6 illustrates a read and write transaction with parity. The master shall drive **CPAR** for the address phases on clock 3 and 7. The target shall drive **CPAR** for the data phase on the read transaction (clock 5) while the master drives **CPAR** for the data phase on the write transaction (clock 8). **CPAR** should be stable and valid one clock after either **CIRDY#** is asserted on the write transaction or **CTRDY#** is asserted on the read transaction.

If the Parity error bit in the Command Register (See 7.2.3) is set to '1', the agent shall assert **CPERR#** when a parity error is detected. **CPERR#** is driven one clock after **CPAR** is driven.

CSERR# shall be used to report system errors where the result could be catastrophic. The assertion of **CSERR#** shall be synchronous to the clock, but the timing is not specified.

NOTE – The detailed specification of Error Functions is defined in the PCI Local Bus Specification section 3.7.

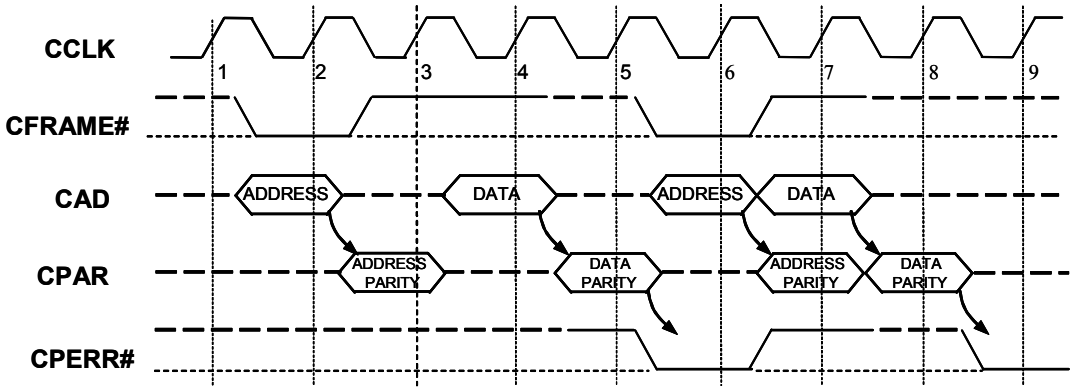


Figure 6.6 – Timing of Parity Operation

7 Register Specification

7.1 Overview

The content of the SSM Card register is defined in this section. The SSM Card shall support the Configuration space register including the Vendor and Device ID registers and additional function specific SSM Card registers.

7.2 Configuration Space Register

The SSM Card Configuration space shall be a 256 byte memory region which is accessed during a Configuration cycle. The access to the Configuration space shall be performed using the bus commands as described in section 6.4.1. A 64 byte predefined header region of the Configuration space registers for the SSM Card is described in Table 7.1. Device ID, Vendor ID, Class Code, Revision ID, Maximum latency, Minimum Grant and Interrupt Line items are allocated in this document, but are defined in the PCI Local Bus Specification.

Table 7.1 – Configuration Space

Items								Configuration Address
31	24	23	16	15	8	7	0	
Device ID				Vendor ID				00h
Status				Command				04h
Class code						Revision ID		08h
BIST		Header type		Latency timer		Cache line size		0Ch
Base address register #1 (a: IO)								10h
Base address register #2(not for use)								14h
Base address register #3 (not for use)								18h
Base address register #4 (not for use)								1Ch
Base address register #5 (not for use)								20h
Base address register #6 (not for use)								24h
Reserved								28h
Reserved				Reserved				2Ch
Extended ROM address (not for use)								30h
Reserved								34h
Reserved								38h
Maximum Latency		Minimum Grant		Interrupt pin		Interrupt line		3Ch

7.2.1 Vendor ID Register (Configuration: 00-01h)

The Vendor ID Register is a read only register that shall identify the manufacturer of a device. The vendor ID shall be assigned to each vendor by the PCI-SIG. Vendors without a vendor ID are encouraged to obtain a registered ID from the PCI-SIG.

Table 7.2 – Vendor ID Register

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Register field	Vendor ID															
An example	0	0	0	1	0	0	0	0	1	1	1	1	0	1	1	1
R/W	RO															

NOTE – The detailed specification is defined in the PCI Local Bus Specification section 6.2.1.

7.2.2 Device ID Register (Configuration: 02-03h)

The Device ID Register is a read only register that shall identify a particular device. This field shall be set to a specific value freely depending on a device by each vendor.

Table 7.3 – Device ID Register

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Register field	Device ID															
An example	1	0	0	0	0	0	1	0	0	0	0	0	0	1	1	0
R/W	RO															

NOTE – The detailed specification is defined in the PCI Local Bus Specification section 6.2.1.

7.2.3 Command Register (Configuration: 04-05h)

The Command Register shall specify a function's ability to generate and respond to the different access cycles possible for the SSM Card. When this register is set to '0', the function shall accept only configuration accesses. The configuration accesses shall be supported as a minimum level of functionality.

The field layout of the Command register is shown in Table 7.4.

Table 7.4 – Command Register

	D15	D14	D13	D12	D11	D10	D9	D8
Register field	Reserved						Fast Back to Back Enable	SERR# Enable
Initial value	0	0	0	0	0	0	0	0
R/W	RO						R/W	

	D7	D6	D5	D4	D3	D2	D1	D0
Register field	Reserved	Parity Error Response	VGA Platte Snoop	Invalidate	Special Cycle	Bus Master	Memory Space	I/O Space
Initial value	0	0	0	0	0	0	0	0
R/W	R /W							

- **D9 : Fast Back-to-Back Enable**

  This field controls whether a master can do fast back-to-back transactions to different devices or not. This field may be set by system software if the adapter and the card are fast back-to-back capable. If this field is reset to '0', the fast back-to-back transactions shall only be allowed to operate on the same agent. If this field is set to '1', the master shall be allowed to generate the fast back-to-back transactions to different agents.

NOTE – The detailed specification of the fast back to back transactions is described in the PCI Local Bus Specification section 3.4.2.

- **D8 : SERR# Enable**

  This field shall control whether the CSERR# output buffer is enabled or not. Implementation of this field is mandatory. If this field is reset to '0', the CSERR# output buffer shall be disabled. If this field is set to '1', the CSERR# output buffer shall be enabled. This field and the Parity Error Response field shall both be set to '1' in order for address parity errors to be reported.

- **D7 : Reserved**

  This field shall be set to '0'.

- **D6 : Parity Error Response**

  This field shall specify how a function responds to parity errors. Implementation of this field is mandatory. If this field is reset to '0', the function shall ignore any parity error detected and shall continue normal operations. If this field is set to '1', the function shall take whatever action that is defined in the event when a parity error is detected. Functions shall generate parity even if their parity checking mechanism is disabled.

- **D5 : VGA Palette Snoop**

  This field shall specify how palette registers are handled by VGA compatibles. If this field is reset to '0', a function should treat palette accesses like all other accesses. If this field is set to '1', special palette snooping behavior is enabled. This field shall be set to '0' in the SSM Card.

NOTE – The detailed specification of the VGA Palette Snoop is described in the PCI Local Bus Specification section 3.10.

- **D4 : Memory Write and Invalidate Enable**

  This field shall specify whether this master may generate the Memory Write and Invalidate command and shall be supported by masters that can generate the Memory Write and Invalidate command. If this field is reset to '0', the Memory Write shall be used. If this field is set to '1', masters may generate the command. This field shall be implemented by masters that can generate the Memory Write and Invalidate command.

- **D3 : Special Cycles**

  This field shall specify whether a function responds to Special Cycle operations or not. If this field is reset to '0', the function shall ignore all the Special Cycle operations. If this field is set to '1', the function may monitor the Special Cycle operations.

- **D2 : Bus Master**

  This field shall specify whether a function can act as a master on the bus or not. If this field is reset to '0', the function may not generate bus accesses. If this field is set to '1', the function may behave as a bus master.

· D1 : Memory Space

This field shall specify whether a function responds to memory space accesses or not. If this field is reset to '0', the function shall not respond to the memory space accesses. If this field is set to '1', the function shall respond to the memory space accesses. If the I/O Space field is reset to '0' and this field is reset to '0', then the Card shall accept only configuration accesses.

· D0 : I/O Space

This field shall specify whether a function responds to I/O space accesses. If this field is reset to '0', the function does not respond to the I/O space accesses. If this field is set to '1', the function responds to the I/O space accesses. If the Memory Space field is reset to '0' and this field is reset to '0', then the Card accepts only configuration accesses.

7.2.4 Status Register (Configuration: 06-07h)

The Status Register is intended to hold run-time status information for bus related events. The field layout of the Status Register is described in Table 7.5. Each field should be implemented depending on the presence of functionality. Readings of this register do not cause any side-effects. Writes are slightly different in that fields can be reset, but not set. A field shall be reset whenever the register is written and the data in the corresponding location is one.

After a Card is reset, all implemented fields in this register shall be set to '0', except for the **CDEVSEL#** Timing and the Fast Back-to-Back Capable bit fields which are read-only. When a specific event occurs, the corresponding field in this register shall be set to '1'.

Table 7.5 – Status Register

	D15	D14	D13	D12	D11	D10	D9	D8
Register field	Detected Parity Error	Signaled System Error	Received Master Abort	Received Target Abort	Signaled Target Abort	**CDEVSEL#** Timing		Data Parity Detected
Initial value	0	0	0	0	0	0	1	0
R/W	R/W							

	D7	D6	D5	D4	D3	D2	D1	D0
Register field	Fast B-to-B Capable	Reserved						
Initial value	0	0	0	0	0	0	0	0
R/W	R/W	RO						

· D15 : Detected Parity Error

This field shall be set to '1' by a function whenever a parity error is detected even if parity error handling is disabled.

· D14 : Signaled System Error

This field shall be set to '1' by a master whenever **CSERR#** is asserted. All masters shall implement this field.

· D13 : Received Master Abort

This field shall be set to '1' by a master whenever its transaction, except for Special Cycles, is terminated with master-abort. All masters shall implement this field.

- **D12 : Received Target Abort**

  This field shall be set to '1' by a master whenever its transaction is terminated with target-abort. All masters shall implement this field.

- **D11 : Signaled Target Abort**

  This field shall be set to '1' by a target whenever it terminates a transaction with target-abort. Functions that never signal target-abort do not need to implement this field.

- **D9 – D10 : CDEVSEL# Timing**

  This field encodes the timing of **CDEVSEL#**. The three allowable timings are encoded as 00b for fast, 01b for medium, and 10b for slow (11b is reserved). This field is read-only and shall indicate the slowest time in which a card asserts **CDEVSEL#** for any bus command except Configuration Read and Configuration Write.

NOTE – The detailed specification of CDEVSEL# timing is described in the PCI Local Bus Specification section 3.6.1.

- **D8 : Data Parity Detected**

  This field shall be only implemented by bus masters. If this field is set to '1', the following three conditions shall be satisfied: (1) the bus agent asserted **CPERR#** itself or the observed **CPERR#** is asserted; (2) the agent setting the bit field acted as the bus master for the operation in which the error occurred; (3) the Parity Error Response bit field (Command Register) is set.

- **D7 : Fast Back-to-Back Capable**

  This read-only field shall indicate whether or not the target is capable of accepting fast back-to-back transactions when the transactions are not to the same agent. If this field is reset to '0', the function cannot accept these transactions. If this field is set to '1', the function can accept these transactions.

7.2.5 Revision ID Register (Configuration: 08h)

The Revision ID Register is a read only register that shall identify a specific revision of a device. The value shall be set and selectable by a vendor.

Table 7.6 – Revision ID Register

	D7	D6	D5	D4	D3	D2	D1	D0
Register field	Revision ID							
An example	0	0	0	0	0	0	0	1
R/W	RO							

NOTE – The detailed specification is defined in the PCI Local Bus Specification section 6.2.1.

7.2.6 Class Code Register (Configuration: 09-0Bh)

The Class Code Register is a read-only register that shall identify the class and generic function of a device. The Class Code Register classifies three codes; the Basic Class code identifies the function the device performs, the Sub-class code identifies more specific function of the device and the Programming Interface identifies a specific register level programming interface. In the SSM Card, the value shall be set to "018000h".

Table 7.7 – Class Code Register

	D23	D22	D21	D20	D19	D18	D17	D16
Register field	Basic class							
Initial value	0	0	0	0	0	0	0	1
R/W	RO							

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Register field	Sub class								Programming interface							
Initial value	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RO															

NOTE – The detailed specification is defined in the PCI Local Bus Specification section 6.2.1.

7.2.7 Cache Line Size Register (Configuration: 0Ch)

The Cache Line Size Register shall specify the system cache line size in units of 32-bit words. This register shall be implemented by masters that can generate the Memory Write and Invalidate command. Functions participating in the caching protocol use this register to know how to disconnect burst accesses at cache line boundaries. The default value of this register shall be zero when the Card is reset. This register shall be set by Card Services to inform the Card what size is supported by the system. A size of 0 generally indicates that the memory spaces of this function is not cacheable, i.e. software must guarantee coherency if it is cached. Since this register indicates the level of system support, all cacheable functions on a Card have the same value for Cache Line Size, which is defined by the system.

Table 7.8 – Cache Line Size Register

	D7	D6	D5	D4	D3	D2	D1	D0
Register field	Cache Line Size							
Initial value	0	0	0	0	0	0	0	0
R/W	R/W							

7.2.8 Latency Timer Register (Configuration: 0Dh)

The Latency Timer register shall specify, in units of bus clocks, the value of the Latency Timer for this bus master. This register shall be implemented as writable by any master that can burst more than two data phases. This register may be implemented as read-only for Cards that burst two or fewer data phases, but the hardwired value shall be limited to 16 or less. When the Card is reset, the default value of the non-read-only fields of this register shall be zero.

Table 7.9 – Latency Timer Register

	D7	D6	D5	D4	D3	D2	D1	D0
Register field	Latency Timer							
Initial value	0	0	0	0	0	0	0	0
R/W	R/W							

7.2.9 Header Type Register (Configuration: 0Eh)

The Header Type Register shall identify the layout of bytes 10h through 3Fh in the Configuration space and also identifies whether the Card contains multiple functions or not. Bit 7 in this register is used to identify a multi-function Card. If this register is reset, the Bit 7 shall be set to '0' to indicate that the Card has a single function. If this register is set, the Bit 7 shall be set to '1' to indicate that the Card has multiple functions. Implementation of the single function is mandatory.

Bits 6 through bit 0 specify the layout of bytes 10h through 3Fh. The value 00h defines the layout of the pre-defined header space shown in the Configuration space. All other values (01h~7Fh) are reserved for future use.

Table 7.10 – Header Type Register

	D7	D6	D5	D4	D3	D2	D1	D0
Register field	Header Type							
Initial value	0	0	0	0	0	0	0	0
R/W	R/W							

7.2.10 BIST Register (Configuration: 0Fh)

The BIST Register is optional and is used for control and status of BIST (Built-in Self Test). Functions that do not support BIST shall return 00h.

Table 7.11 – BIST Register

	D7	D6	D5	D4	D3	D2	D1	D0
Register field	BIST Capable	Start BIST	Reserved		Completion Code			
Initial value	0	0	0	0	0	0	0	0
R/W	R/W							

· D7 : BIST Capable

If this field is set to '1', the function supports BIST.

· D6 : Start BIST

If this field is reset to '0', the BIST is complete. If this field is set to '1', BIST shall be invoked. The test shall be considered as failed if BIST is not complete within 2 seconds.

· D3 – D0 : Completion Code

A value of '0' means the function has passed its test. Non-zero values mean the test failed. Function-specific failure codes may be encoded in the non-zero values. These are implementation dependent and beyond the scope of this standard.

7.2.11 Base Address Register "a": I/O Space (Configuration: 10-13h)

The Base Address Register "a" indicates the base address "a" of the I/O space. The layout for the Base Address Register for the I/O space mapping shall be as given in Table 7.12. Bits 0-1 are read only fields as specified below and the remaining bits (2-31) represent a Base address.

Table 7.12 – Base Address Register

	D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
Register field	Base address															
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W															

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Register field	Base address														Res	I/O
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R/W	R/W														RO	

- **D31-D2 : Base address**

- **D1 : Res**

  Reserved bit and shall be set to ‘0’.

- **D0 : I/O**

  This field shall be set to ‘1’ to indicate the mapping to I/O space.

7.2.12 Interrupt Line Register (Configuration: 3Ch)

The Interrupt Line Register is an eight-bit register that shall be used to communicate interrupt line routing information. This register is read/write and shall be implemented by any device (or device function) that uses an interrupt pin.

Table 7.13 – Interrupt Line Register

	D7	D6	D5	D4	D3	D2	D1	D0
Register field	Interrupt Line							
Initial value	0	0	0	0	0	1	0	1
R/W	R/W							

NOTE – The detailed specification is defined in the PCI Local Bus Specification section 6.2.4.

7.2.13 Interrupt Pin Register (Configuration: 3Dh)

The Interrupt Pin Register is a read only register that shall indicate which interrupt pin the device uses. In the SSM Card, the value shall be set to ‘01h’ to indicate CINT# which corresponds to INTA# in the PCI specification.

Table 7.14 – Interrupt Pin Register

	D7	D6	D5	D4	D3	D2	D1	D0
Register field	Interrupt pin							
Initial value	0	0	0	0	0	0	0	1
R/W	RO							

NOTE – The detailed specification is defined in the PCI Local Bus Specification section 6.2.4.

7.2.14 Minimum Grant and Maximum Latency (Configuration: 3Eh/3Fh)

The Minimum Grant and Maximum latency registers shall be used to specify the device desired settings for Latency Timer values. For both registers, the value specifies a period of time in units of 1/4 microsecond. Value 0 indicates that the device has no major requirements on setting of a Latency Timer.

The Minimum Grant Register is a read only register that shall specify how long a burst period the device needs to expect a clock rate of 33 MHz.

The Maximum Latency Register is a read only register that shall specify how often the device needs to gain an access to the bus.

Table 7.15 – Minimum Grant Register

	D7	D6	D5	D4	D3	D2	D1	D0
Register field	Minimum Grant							
Initial value	0	0	0	0	0	1	0	1
R/W	RO							

Table 7.16 – Maximum Latency Register

	D7	D6	D5	D4	D3	D2	D1	D0
Register field	Maximum Latency							
Initial value	0	0	0	0	0	1	0	1
R/W	RO							

NOTE – The detailed specification is defined in the PCI Local Bus Specification section 6.2.4.

7.3 SSM Card Specific Register

The SSM Card Specific Register is the register related to interruption and command functions. Items in the SSM Card Specific Register shall be as defined in Table 7.17.

Table 7.17 – SSM Card Specific Register

Items				IO space, base address offset
31 24	23 16	15 8	7 0	
-	-	Interrupt Control	Interrupt status	a+00h
-	-	-	-	a+04h
HOST address				a+08h
-	-	-	-	a+0Ch
LBA Low	Sector Count	Error/Features	Data (note 1)	a+10h
SSM Card Status /Command	Device	LBA High	LBA Mid	a+14h
-				a+18h
-	Alternate /Device	-	-	a+1Ch
Tuple space(128byte)				-

NOTE 1 – for 32-bit PIO only.
NOTE 2 – Items described as "-" shall not be accessed.

7.3.1 Interrupt Status Register (IO: a+00h)

The Interrupt Status Register shall be used to represent the INTRQ signal.

Table 7.18 – Interrupt Status Register

	D7	D6	D5	D4	D3	D2	D1	D0
Register field	Reserved			Reserved	Reserved	IRQ	Reserved	
Initial value	1	0	0	0	0	0	0	0
R/W	RO	RO		RO	RO	R/W	RO	

· D2 : IRQ

IRQ always represents the INTRQ signal, which is defined in the ATA standard and internally generated within the SSM Card. The "High" level of the INTRQ signal shall correspond to an IRQ of "1" and the "Low" level of the INTRQ signal shall correspond to an IRQ of "0". Reading the SSM Card Status Register clears an Interrupt.

NOTE – This register is unique to the SSM Card.

7.3.2 Interrupt Control Register (IO: a+01h)

The Interrupt Control Register shall be used to mask the INTRQ signal, which is represented by the IRQ bit in the Interrupt Status Register and output as the CINT# signal.

Table 7.19 – Interrupt Control Register

	D7	D6	D5	D4	D3	D2	D1	D0
Register field	Reserved			Reserved	Reserved	IRQE	Reserved	
Initial value	0	0	0	0	0	0	0	0
R/W	RO			RO	RO	R/W	RO	

· D2 : IRQE

IRQE shall control the masking of the IRQ bit of the Interrupt Status Register and assert the SSM Card bus CINT# signal. In the case that the IRQE bit is set to "1", the CINT# signal shall be asserted depending on the IRQ bit. In the case that the IRQE bit is set to “0”, the IRQ bit shall be masked.

The interrupt process using the Interrupt Status Register and the Interrupt Control Register is shown in Figure 7.1. The INTRQ signal generated within the SSM Card is internally masked with the nIEN bit in the Device Control Register (see 7.3.14) and then represented as the IRQ bit of the Interrupt Status Register. The IRQ bit representing the masked INTRQ signal is masked with the IRQE bit at the input to the Interrupt Control Register and the CINT# signal is output to the SSM Card bus.

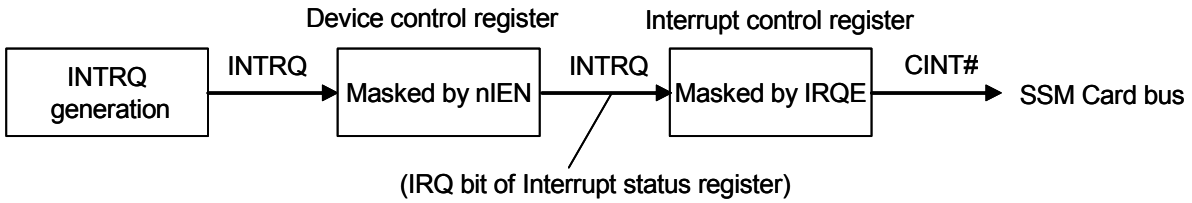


Figure 7.1 – Interrupt process sequence

7.3.3 Host Address Register (IO: a+08h - a+0Bh)

The Host Address Register shall indicate the start address of the descriptor table of scatter/gather, which is set by a host device. The structure of the descriptor table is shown in Figure 7.2. The SSM Card recognizes the memory space, storing data, which should be transferred, by reading from the address specified by this register to EOT.

Table 7.20– Host Address Register

	D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
Register field	HOST Address[31:16]															
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W															

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Register field	HOST Address[15:0]															
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W														RO	

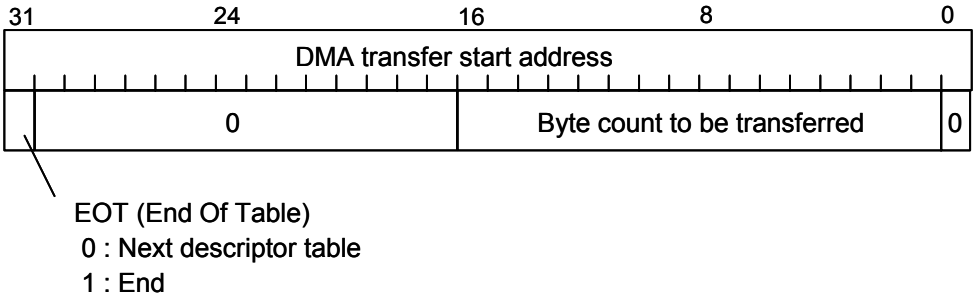


Figure 7.2 – Structure of a Descriptor table

7.3.4 Data Register (IO: a+10h)

The Data register shall be accessed for host PIO data transfer only when DRQ is set to '1'.

PIO data-out transfers are processed by a series of reads to this register, each read transferring the data that follows the previous read. PIO data-in transfers are processed by a series of writes to this register, each write transferring the data that follows the previous write. The results of a read during a PIO in or a write during a PIO out are indeterminate.

The data register shall be 32 bits wide. Field and detailed bit descriptions for the Data register are given in Table 7.21.

Table 7.21 – Data Register

	D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
Register field	Data															
Initial value	unknown															
R/W	R/W															
	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Register field	Data															
Initial value	unknown															
R/W	R/W															

NOTE – This register is defined in the ATA standard as optional, section 7.6.

7.3.5 Features / Error Register (IO: a+11h)

The Feature Register and the Error Register share the same address in memory space. When the host writes this address, the value shall be written in the Features Register. When the host reads this address, the content of the Error register shall be read.

7.3.5.1 Feature Register

The Feature Register shall be written only when BSY and DRQ equal zero. If this register is written when BSY or DRQ is set to one, the result is indeterminate.

The content of this register is command dependent and becomes a command parameter when the Command Register is written.

Field and detailed bit descriptions for this register are given in Table 7.22.

Table 7.22 – Features Register

	D7	D6	D5	D4	D3	D2	D1	D0
Resister field	Features Byte							
HOST R/W	WO							

NOTE – This register is defined in the ATA standard, section 7.10.

7.3.5.2 Error Register

The Error Register indicates additional information about the cause of an error during execution of the previous command. The host has to check this register when D0 (ERR) of Status Register is set to '1', but is not able to write data in this register.

The contents of the Error Register shall be valid when BSY and DRQ are cleared to '0' and ERR is set to '1'. At completion of any command, the contents of this register shall be valid when the ERR bit is set to '1' in the Status Register.

Field and detailed bit descriptions for this register are given in Table 7.23.

Table 7.23 – Error Register

	D7	D6	D5	D4	D3	D2	D1	D0
Register field	-	UNC	-	IDNF	-	ABRT	-	-
Initial value	0	0	0	0	0	0	0	1
HOST R/W	RO							

- **D6 : UNC**

  UNC shall be set to '1', when an error that is not correctable is encountered.

- **D4 : IDNF**

  IDNF shall be set to '1' when the requested sector ID is in error or cannot be found.

- **D2 : ABRT**

  ABRT (command aborted) shall be set to '1' to indicate the requested command has been command aborted because the command code or a command parameter is invalid, the command is not supported, a prerequisite for the command has not been met, or some other error has occurred.

NOTE – This register is defined in the ATA standard, section 7.9.

7.3.6 Sector Count Register (IO: a+12h)

The Sector Count Register shall be written only when both BSY and DRQ are cleared to ‘0’. The contents of this register are only valid when both BSY and DRQ are cleared to ‘0’. If this register is written when BSY or DRQ is set to ‘1’, the result is indeterminate.

The content of this register is command dependent and becomes a command parameter when the Command register is written.

Field and detailed bit descriptions for this register are given in Table 7.24.

Table 7.24 – Sector Count Register

	D7	D6	D5	D4	D3	D2	D1	D0
Register field	Sector Count							
Initial value	0	0	0	0	0	0	0	1
HOST R/W	R/W							

NOTE – This register is defined in the ATA standard, section 7.14.

7.3.7 LBA Low Register (IO: a+13h)

The LBA Low Register defines the low address (A7 to A0) of LBA. The LBA Low Register shall be written only when both BSY and DRQ are cleared to ‘0’. The contents of this register are only valid when both BSY and DRQ are cleared to ‘0’. If this register is written when BSY or DRQ is set to ‘1’, the result is indeterminate.

The content of this register is command dependent and becomes a command parameter when the Command register is written.

Field and detailed bit descriptions for this register are given in Table 7.25.

Table 7.25 – LBA Low Register

	D7	D6	D5	D4	D3	D2	D1	D0
Register field	A7 - A0 (LBA Addressing)							
Initial value	0	0	0	0	0	0	0	1
HOST R/W	R/W							

NOTE – This register is defined in the ATA standard, section 7.12.

7.3.8 LBA Mid Register (IO: a+14h)

The LBA Mid Register defines the middle address (A15 to A8) of LBA. The LBA Mid Register shall be written only when both BSY and DRQ are cleared to ‘0’. The contents of this register are only valid when BSY and DRQ are cleared to ‘0’. If this register is written when BSY or DRQ is set to ‘1’, the result is indeterminate.

The content of this register is command dependent and becomes a command parameter when the Command register is written.

Field and detailed bit descriptions for this register are given in Table 7.26.

Table 7.26 – LBA Mid Register

	D7	D6	D5	D4	D3	D2	D1	D0
Register field	A15 - A8 (LBA Addressing)							
Initial value	0	0	0	0	0	0	0	0
HOST R/W	R/W							

NOTE – This register is defined in the ATA standard, section 7.13.

7.3.9 LBA High Register (IO: a+15h)

The LBA High Register defines the high address (A23 to A16) of LBA. The LBA High Register shall be written only when both BSY and DRQ are cleared to ‘0’. The contents of this register are only valid when BSY and DRQ are set to ‘0’. If this register is written when BSY or DRQ is set to ‘1’, the result is indeterminate.

The content of this register is command dependent and becomes a command parameter when the Command register is written.

Field and detailed bit descriptions for this register are given in Table 7.27.

Table 7.27 – LBA High Register

	D7	D6	D5	D4	D3	D2	D1	D0
Register field	A23 – A16 (LBA Addressing)							
Initial value	0	0	0	0	0	0	0	0
HOST R/W	R/W							

NOTE – This register is defined in the ATA standard, section 7.11.

7.3.10 Device Register (IO: a+16h)

The Device Register shall be used to specify one drive out of a pair of drives sharing one set of register and the address (A27 to A24) of LBA.

This register shall be written only when both BSY and DRQ are cleared to ‘0’. The contents of this register are valid only when BSY is cleared to ‘0’. If this register is written when BSY or DRQ is set to ‘1’, the result is indeterminate. The DEV bit becomes effective when the host writes to this register or the signature is set by the device. All other bits in this register become a command parameter when the Command register is written.

Bit 4, DEV, in this register selects the device. Other bits in this register are command dependent.

Field and detailed bit descriptions for this register are given in Table 7.28.

Table 7.28 – Device Register

	D7	D6	D5	D4	D3	D2	D1	D0
Register field		LBA		DEV	A27	A26	A25	A24
Initial value	1	0	1	0	0	0	0	0
HOST R/W	R/W							

· LBA

LBA shall be set to "1".

NOTE – This register is defined in the ATA standard, section 7.7

7.3.11 SSM Card Command / SSM Card Status Register (IO: a+17h)

The SSM Card Command and the SSM Card Status Register share the same address in memory space. When the host writes this address, the value is written in the SSM Card Command Register. When the host reads this address, the content of the SSM Card Status register is read.

7.3.11.1 SSM Card Command Register

For all commands except DEVICE RESET, the SSM Card Command Register shall only be written when BSY and DRQ are both cleared to '0'. If written when BSY or DRQ is set to '1', the results of writing the SSM Card Command register are indeterminate except for the DEVICE RESET command.

Command processing begins when this register is written. The content of the Command Block register becomes a parameter of the command when this register is written. Writing this register clears any pending interrupt condition.

This register contains the command code being sent to the device. Command execution begins immediately after this register is written.

Field and detailed bit descriptions for this register are given in Table 7.29.

Table 7.29 – SSM Card Command Register

	D7	D6	D5	D4	D3	D2	D1	D0
Register field	Command Code							
HOST R/W	WO							

NOTE – This register is defined in the ATA standard, section 7.4.

7.3.11.2 SSM Card Status Register

The SSM Card Status Register shall indicate the status of the SSM Card. The contents of the Status Register, except for BSY, shall be ignored when BSY is set to '1'.

Reading this register when an interrupt is pending causes the interrupt pending to be cleared. The host should not read the SSM Card Status Register when an interrupt is expected as this may clear the interrupt pending before the INTRQ may be recognized by the host.

This register contains the device status. The contents of this register shall be updated to reflect the current state of the device.

Field and detailed bit descriptions for this register are given in Table 7.30.

Table 7.30 – SSM Card Status Register

	D7	D6	D5	D4	D3	D2	D1	D0
Register field	BSY	DRDY	-	DSC	DRQ	-	-	ERR
Initial value	1	0	0	0	0	0	0	0
HOST R/W	RO							

· BSY(Busy)

BSY is set to '1' to indicate that the device is busy. After the host has written the SSM Card Command Register, the device shall have either the BSY bit set to '1', or the DRQ bit set to '1', until command completion or the device has performed a bus release for an overlapped command.

· DRDY(Device Ready)

This Card can accept a command when this bit is set to '1'. This bit is cleared when first turning on, and remains clear until the command is ready to be received.

· DSC (Device Seek Complete)

This bit is normally set to '1'. It is set to '0' during initialization.

· DRQ(Data Request)

DRQ indicates that the device is ready to transfer data between the host and the device. After the host has written the Command Register, the device shall either set the BSY bit to '1' or the DRQ bit to '1' until command completion or the device has performed a bus release for an overlapped command.

· ERR

ERR indicates that an error occurred during execution of the previous command.

NOTE – This register is defined in the ATA standard, section 7.15.

7.3.12 Device Control / Alternate Status Register (IO: a+1Eh)

The Device Control Register and the Alternate Status Register share the same address in memory space. When the host writes this address, the value is written in the Device Control Register. When the host reads this address, the content of the Alternate Status register is read.

7.3.12.1 Device Control Register

The Device Control Register shall control an interrupt request of the Card and shall be used to order a Software Reset to the Card.

The content of this register shall take effect when written.

This register allows a host to software reset attached devices and to enable or disable the assertion of the INTRQ signal by a selected device. When the Device Control register is written, both devices respond to the write regardless of which device is selected. When the SRST bit is set to '1', both devices shall perform software reset.

Table 7.31 – Device Control Register

	D7	D6	D5	D4	D3	D2	D1	D0
Register field	0	0	0	0	1	SRST	nIEN	0
HOST R/W	WO							

· SRST

SRST is a software reset bit.

· nIEN

nIEN is the enable bit for the device assertion of INTRQ to the host. When the nIEN bit is cleared to '0', and the device is selected, INTRQ shall be enabled through a tri-state buffer and shall be asserted or negated by the device as appropriate. When the nIEN bit is set to '1', or the device is not selected, the device shall release the INTRQ signal.

NOTE – This register is defined in the ATA standard, section 7.8.

7.3.12.2 Alternate Status Register

The register field of the Alternate Status Register contains the same information as the SSM Card Status Register. Data in the Alternate Status Register is stored after reading the data in the register; while data in the SSM Card Status Register is not stored after reading the data in the register.

When the BSY bit is set to '1', the other bits in this register shall not be used.

Reading this register shall not clear a pending interrupt.

Field and detailed bit descriptions for this register are the same as that for the SSM Card Status Register and given in section 7.3.11.2.

NOTE – This register is defined in the ATA standard, section 7.3.

8 Command Specification

8.1 Overview

This section specifies the commands required for the SSM Card. Write protection functionality and Power management are performed using the ATA commands. The Bus Master DMA command is supported for the data transmission between a SSM Card and a host. The commands for sensing log information written in the SSM Card are also specified.

8.2 IDENTIFY DEVICE (ECh)

The IDENTIFY DEVICE command enables the host to receive parameter information from the SSM Card. The description about the IDENTIFY DEVICE command shall be as specified in 8.15 of the ATA Standard. Words 129 to 159 of the IDENTIFY DEVICE information are defined as a Vendor specific area as shown in Table 27 of the ATA standard. Therefore, the SSM Card shall provide the write protection function using this area as defined in Table 8.1.

Table 8.1 – Addition of IDENTIFY DEVICE information

Word (16 bits)	F/V	Description
129-133	X	Vendor specific
134	V	Write protected (Write Protect Switch = H) : 0001h Not write protected (Write Protect Switch = L) : 0000h
135-159	X	Vendor specific

NOTE – V = Variable and may change depending on the state of the device.
X = May be fixed or variable.

8.3 SET FEATURES (EFh)

The SET FEATURES command enables the host to establish parameters that affect the execution of certain device features. The detailed information about the SET FEATURES command shall be as described in 8.46 of the ATA Standard.

The SSM Card shall support the Advanced power management sub command for the setting of low power consumption mode.

The advanced power management level indicates the level of power management. The SSM Card shall support the intermediate power management levels with Standby as shown in Table 8.2.

Table 8.2 – Advanced power management levels

Level	Sector Count value	Support
Maximum performance	FEh	
Intermediate power management levels without Standby	81h-FDh	
Minimum power consumption without Standby	80h	
Intermediate power management levels with Standby	02h-7Fh	Required
Minimum power consumption with Standby	01h	
Reserved	FFh	
Reserved	00h	

In the intermediate power management levels with Standby, Sector count values corresponding to the maximum power consumption are given in Table 8.3.

Table 8.3 – Sector Count values

Sector Count	Maximum power consumption (mA)
7Fh	1000
7Eh	992
:	: incrementing in steps of 8
4Dh	600
:	: incrementing in steps of 8
34h	400
:	: incrementing in steps of 8
03h	8
02h	0

When the SSM Card receives the Enable Advanced power management command, the power consumption of the SSM Card should be set to the maximum level which does not exceed the required level. If the required level is less than the level which the SSM Card operates, the command should be aborted.

The current maximum power consumption of the SSM Card is represented in the Word 91 of IDENTIFY DEVICE.

8.4 Bus Master DMA

The SSM Card shall support the Bus Master DMA transfer protocol to achieve high speed data transfer between a host and a SSM Card. READ MASTER DMA and WRITE MASTER DMA commands shall be used to initiate a data transmission in the Bus Master DMA transfer mode.

8.4.1 READ MASTER DMA (FBh)

The READ MASTER DMA command is the command to start reading with the Bus Master DMA transfer.

Table 8.4 – Command description in case of inputs

Register	7	6	5	4	3	2	1	0
Features	Sector Count A15-A8							
Sector Count	Sector Count A7-A0							
LBA Low	LBA A7-A0							
LBA Mid	LBA A15-A8							
LBA High	LBA A23-A16							
Device	na	1	na	DEV	LBA A27-A24			
Command	Command ”FBh”							

The read block size shall be specified with the Sector Count (number of sectors), each of which is 512 bytes in size. The bit length of the Sector Count is 16 bits and the Features Register is used for the high address (A15-A8) of the Sector Count. The maximum block size shall be limited to 2MB which is identified as 1000h. When the specified value equals to 0000h or exceeds this maximum block size, the command should be aborted.

Table 8.5 – Command description in case of normal outputs

Register	7	6	5	4	3	2	1	0
Error	00h							
Sector Count	na							
LBA Low	na							
LBA Mid	na							
LBA High	na							
Device	na	LBA	na	DEV	na			
Status	BSY	DRDY	0	1	DRQ	0	0	0

Table 8.6 – Command description in case of error outputs

Register	7	6	5	4	3	2	1	0
Error	na	UNC	na	IDNF	na	ABRT	na	na
Sector Count	na							
LBA Low	na							
LBA Mid	na							
LBA High	na							
Device	na	LBA	na	DEV	na			
Status	BSY	DRDY	0	1	DRQ	0	0	ERR

"na" indicates the content of a bit or field is not applicable to the particular command.

8.4.2 WRITE MASTER DMA(FCh)

The WRITE MASTER DMA command is the command to start writing with the Bus Master DMA transfer. The setup parameters shall be the same as those in the READ MASTER DMA command described in section 8.4.1.

8.5 CARD DATA IN(FEh)

8.5.1 Log sense sub command

The CARD DATA IN command shall be supported to read the Log information generated in the SSM Card.

Table 8.7 – Command description in case of inputs

Register	7	6	5	4	3	2	1	0
Features	Sub Command "01h"							
Sector Count	na							
LBA Low	PageCode [7:0]							
LBA Mid	na							
LBA High	na							
Device	na	na	na	DEV	na			
Command	Command "FEh"							

Table 8.8 – Command description in case of normal outputs

Register	7	6	5	4	3	2	1	0
Error	00h							
Sector Count	na							
LBA Low	na							
LBA Mid	na							
LBA High	na							
Device	na	na	na	DEV	na			
Status	BSY	DRDY	0	1	DRQ	0	0	0

Table 8.9 – Command description in case of error outputs

Register	7	6	5	4	3	2	1	0
Error	0	UNC	0	IDNF	0	ABRT	0	0
Sector Count	na							
LBA Low	na							
LBA Mid	na							
LBA High	na							
Device	na	na	na	DEV	na			
Status	BSY	DRDY	0	1	DRQ	0	0	ERR

“na” indicates the content of a bit or field is not applicable to the particular command.

The Sub Command assigned to the Features register shall be set to “01h” to sense the Log information. The PageCode specifies the Log page number. The data length in the PIO data transmission shall be 512 bytes for each Log page.

8.5.2 Log Parameter Page

The data length of the Log Parameter Page shall be 512 bytes and shall contain the following field.

・Page Code

Page Code indicates the type of Log parameter page. The list of PageCodes and definitions of each type of Log page shall be as described in Table 8.10.

Table 8.10 – List of Page Code

Page Code	Definition of Log page
00h	Support Log Page
20h	Card ID page
21h	CSD page
Others	Reserved

・Page Length

Page Length indicates the byte length of valid data after the Page length field. Although the length of the Log parameter page is 512 bytes, a host may read the valid data up to the field given by the Page length.

・Parameter Code

Parameter Code is the data assigned to Log information and defined in each Log page independently.

· Parameter Length

Parameter Length indicates the data length of Log information corresponding to the Parameter Code.

· Reserved

This field is reserved and will be defined in a future extension.

8.5.2.1 Support Log Page

The support Log page specifies the list of log pages which are supported in the SSM Card. The page code of the supported Log pages shall be read using the CARD DATA IN command. It is recommended that a host should first read this page and detect which Log pages are supported in the Card and then access each of the Log pages. Data allocation in the Support Log Page shall be as described in Table 8.11.

Table 8.11 – Allocation of Support Log Page

	7	6	5	4	3	2	1	0
0	Page Code[7:0] (00h)							
1-17	Reserved							
18	Page Length[15:0]							
19								
20	Page code of supported Log page 1 [7:0]							
21	Page code of supported Log page 2 [7:0]							
22	Page code of supported Log page 3 [7:0]							
----	----							
20+n-1	Page code of supported Log page n [7:0]							
20+n-511	Reserved							

8.5.2.2 Card ID page

The Card ID page specifies the device information of the SSM Card. Data allocation in the Card ID page shall be as defined in Table 8.12.

Table 8.12 – Allocation of Card ID page

	7	6	5	4	3	2	1	0
0	Page Code[7:0] (20h)							
1-17	Reserved							
18	Page Length[15:0]							
19								
20	Parameter Code[15:0] (0001h)							
21								
22	Reserved							
23	Parameter Length[7:0] (10h)							
24	CID [127:120] (Card vendor)							
25-30	CID [119:72] (Vendor unique)							
31-39	CID [71:0] (Reserved)							
40-511	Reserved							

- **CID**

  CID shall be used to identify the SSM Card. The values of the Parameter Code and the Parameter Length are given as follows:

  Parameter Code = 0001h

  Parameter Length = 10h

  CID [127:120] : Card vendor

  CID [127:120] shall specify the name of the vendor of the SSM Card. The vendor name is represented with a code using one character which value is “A” to “Z”. Vendors without a vendor code are encouraged to obtain a registered code from the SMPTE Registration Authority.

  CID [119:72] : Vendor unique

  CID [119:72] is defined by each vendor and any value between 00h and FFh is valid.

8.5.3 CSD page

CSD (Card Specific Data) page describes the specification or performance of the SSM Card. Data allocation in the CSD page shall be as defined in Table 8.14.

Table 8.14 – Allocation of CSD page

	7	6	5	4	3	2	1	0
0	Page Code[7:0] (21h)							
1-17	Reserved							
18	Page Length[15:0]							
19								
20	Parameter Code[15:0] (0003h)							
21								
22	Reserved							
23	Parameter Length[7:0] (02h)							
24	Write block size [15:8]							
25	Write block size [7:0]							
26-511	Reserved							

- **Write Block Size**

  The Write Block Size defines the block size for writing to the SSM Card. The Write Block Size represents the number of sectors, each of which is 512 bytes in size. The Write Block Size shall be 2^m (m<=10) sectors. The maximum block size is 512 Kbytes when the Write Block size is set to 400h (=1024d). A host shall sense the Write Block Size written in the CSD page and perform writing the data to the Card using this block size or its multiple. The values of the Parameter Code and the Parameter Length are given as follows:

  Parameter Code = 0003h

  Parameter Length = 02h

9 Performance specification

9.1 Overview

This section specifies the required performance of the SSM Card with regard to the writing and reading speeds. The Card level is defined to classify the performance level of the SSM Card according to required speed.

9.2 Write performance

To guarantee the writing speed in each level, the SSM Card shall satisfy the following writing time specifications.

- The write time to a random address in a unit of 512 Kbytes shall be completed within Tw512.
- The sum of the writing times to a random address in units of 512 Kbytes in 64 time events shall be completed within Tw512a x 64.

Table 9.1 shows the value of Tw512 and Tw512a depending on the Card level. The value of writing time shown in Table 9.1 indicates the time during which the SSM Card receives a command, performs writing, and returns BUSY.

Table 9.1 – Specification of writing time

Card level	Tw512[msec]	Tw512a[msec]
No level	-	-
Level A	160	40
Other levels	Reserved	Reserved

9.3 Read Performance

To guarantee the reading speed, the SSM Card shall satisfy the following reading time specifications.

- Reading time to a random address in a unit of 32 Kbytes shall be completed within Tr32.
- Reading time to a random address in a unit of 512 Kbytes shall be completed within Tr512.
- Reading time to a random address in a unit of (N x 32 Kbytes) shall be completed within (N-1) x (Tr512-Tr32)/15 + Tr32.

Table 9.2 shows the value of Tr32 and Tr512 depending on the Card level.

Table 9.2 – Specification of reading time

Card level	Tr32[msec]	Tr512[msec]
No level	-	-
Level A	2.5	20
Other levels	Reserved	Reserved

10 File system specification

The file system of the SSM Card shall be the FAT (File Allocation Table) system as defined in ISO/IEC 9293.

10.1 File Allocation Table

In the case that the capacity of the SSM Card is less than or equal to 2G bytes, the count of clusters shall be expressed with 16 bits. In the case that the capacity of the SSM Card is more than 2G bytes, the count of clusters shall be expressed with 32 bits.

10.2 Directory

Directory names shall be expressed with a limit of eight characters. The directory name shall be case-sensitive and each character shall be expressed with capital letters [A~Z] or numbers [0~9]. The directory structure for Content on the SSM Card is defined in an individual Content specification.

10.3 File name

File names shall be expressed with a limit of eight characters and extensions shall be expressed with three characters. The file name and the extensions shall be case-sensitive and expressed with capital letters [A~Z] or numbers [0~9]. Naming rules for files contained in Content on the SSM Card are defined in an individual Content specification.

Annex A (informative)
Bibliography

PC Card: PC Card Standard 8.0 (PCMCIA/JEITA, 2001)

SMPTE RP 2002-2006, Content Specification on Solid State Media Card for DV/DV-Based Essence