SMPTE STANDARD

ANSI/SMPTE 125M-1995
Revision of
ANSI/SMPTE 125M-1992

for Television — Component Video Signal 4:2:2 — Bit-Parallel Digital Interface

Table of contents

American National Standard

Approved
September 12, 1995

1 Scope

This standard defines an interface for system M (525/60) digital television equipment based on ITU-R BT.601. The standard has application in the television studio over distances up to 300 m (1000 ft). The characteristics of the interface are summarized below:

1.1 The video signal is transmitted in the form of one luminance (Y) and two color-difference components (scaled version of R--Y and B--Y).

1.2 The video signal is transmitted at the 4:2:2 family level of ITU-R BT.601, with a nominal luminance sampling frequency of 13.5 MHz. Provision is made to convey signals at 8- or 10-bit precision. Because of the existence of both 8- and 10-bit equipment, all synchronizing signals (EAV, SAV, ANC) must be detected by reference to the eight most significant bits only.

1.3 The bits of the digital code words that describe the video signal are transmitted in a parallel arrangement using ten conductor pairs. Each pair carries a multiplexed stream of bits (of the same significance) of each of the component signals. Accordingly, the bit rate used in each pair is nominally 27 Mb/s. An eleventh conductor pair carries a clock signal at 27 MHz.

1.4 The signals on the interface are transmitted using balanced conductor pairs for a distance up to 50 m (160 ft) without equalization and up to 300 m (1000 ft) with appropriate equalization.

1.5 The interface consists of one transmitter and one receiver in a point-to-point connection.

1.6 Parameters of the signal format are chosen to facilitate conversion to and from a serial digital interface format.

1.7 The interface allows the transmission of appropriate ancillary signals that may be multiplexed into the data stream during video blanking intervals.

1.8 Where hexadecimal values are used, they are indicated by a subscript h, such as $3FF_h$; other values are decimal.

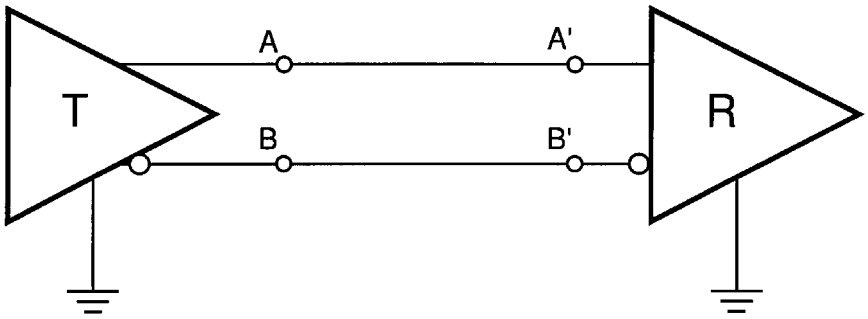
2 General considerations

2.1 Signal convention

The signaling sense of the voltage appearing across the interconnection cable is positive binary and defined as follows (refer to figure 1):

2.1.1 The A terminal of the transmitter shall be negative with respect to the B terminal for a binary 0 (LOW or L or OFF) state.

2.1.2 The A terminal of the transmitter shall be positive with respect to the B terminal for a binary 1 (HIGH or H or ON) state.



T = transmitter
R = receiver
A,A′ = the data line
B,B′ = the return line

Figure 1 — Positive binary signal convention

2.2 Signal names

The data lines are designated DATA 0 through DATA 9. The group of ten signals is identified by placing parentheses around the range of subscripts included, as DATA (0-9). When 8-bit signals are conveyed by the interface, DATA (2-9) shall be used and DATA (0-1) shall be set to zero. DATA 9 is always the most significant bit.

2.3 Sin(x)/x considerations

The characteristics of the data word at the interface are based on the assumption that the location of any required sin(x)/x correction is at the point where the digital signal is converted to an analog format.

2.4 Blanking interval considerations

This standard does not require the device feeding the interface to transmit video data during the entire blanking interval. Therefore, ancillary information may be inserted into the horizontal blanking interval by the user within the constraints specified in 3.4 and 3.5.

The vertical blanking duration is a minimum of nine lines. Ancillary information may be inserted into this nine-line interval by the user within the constraints specified in 3.4 and 3.5.

2.5 Signal specifications

All digital signal time intervals are specified at the half-amplitude points. All transitions are specified between the 20% and 80% amplitude points.

2.6 Electromagnetic interference considerations

Digital apparatus can radiate a significant amount of energy at harmonics of the clock frequency. In the case of 13.5 MHz, clock harmonics lie at 121.5 MHz and 243 MHz, both of which are aeronautical distress frequencies. Equipment and system designers must, therefore, pay particular attention to the provision of adequate screening.

3 Interface format

3.1 General description

The interface consists of a unidirectional, eleven-pair interconnection between a transmitting equipment and a receiving equipment. Video data, timing reference information, and ancillary signals are time multiplexed and transferred on ten data pairs in NRZ form. An eleventh pair provides a synchronous clock.

3.2 Encoding parameters

Table 1 summarizes the encoding parameter values.

3.3 Interface characteristics

Table 2 specifies the interface characteristics.

3.4 Digital blanking relationship

3.4.1 Horizontal sync relationship

Figure 2a shows the relationship between video signals in the digital and analog domain for 525-line systems. Figure 2b shows the multiplex structure.

Transmitted during each active line are 1440 multiplexed luminance and chrominance values (720 luminance, 360 chrominance C_R, and 360 chrominance C_B values).

Eight of the remaining 276 interface clock intervals are used to transmit synchronizing information; the other 268 interface clock intervals may be used to carry ancillary information.

The first of these 1716 interface clock intervals is designated line word 0 for the purpose of reference only. The 1716 sample words per total line are therefore numbered 0 through 1715. Intervals 0 through 1439, inclusive, contain video data. The interface clock intervals occurring during digital blanking are designated 1440 through 1715.

Intervals 1440 through 1443 are reserved for the end-of-active-video (EAV) timing reference described in 3.5.3.

Intervals 1712 through 1715 are reserved for the start-of-active-video (SAV) timing reference described in 3.5.3.

The half-amplitude point of the leading (falling) edge of the analog horizontal sync signal shall be coincident with a sample point which would be conveyed by word 1473 if carried across the interface.

Table 1 — Encoding parameters

Coded signals: These values are obtained from the gamma precorrected signals	$Y = 0.299R + 0.587G + 0.114B$ $C_R = 0.713 (R-Y) = 0.500R - 0.419G - 0.081B$ $C_B = 0.564 (B-Y) = 0.500B - 0.169R - 0.331G$	
Number of samples per line: -- luminance (Y) -- each color-difference signal (C_R, C_B) -- total number of samples	Total 858 429 1716	Active 720 360 1440
Sampling structure:	Orthogonal: line, field, and frame repetitive; C_R and C_B samples are cosited with odd (1st, 3rd, 5th) Y samples in each line	
Sampling frequency: -- luminance (Y) -- each color-difference signal (C_R, C_B)	 13.5 MHz nominal 6.75 MHz nominal	
Form of encoding:	Uniformly quantized, PCM, 10 bits per sample, for the luminance signal and each color-difference signal (for 8-bit encoding see 2.2).	
Correspondence between video signal levels and quantization levels: -- luminance signal (Y) -- each color-difference signal (C_R, C_B)	 877 quantization levels with the black level corresponding to level 64 and the peak white level corresponding to level 940 897 quantization levels symmetrically distributed about level 512, corresponding to the zero signal	

Table 2 — Interface characteristics

Digital format	Parallel: eleven balanced signal pairs carrying clock and ten data bits
Interface clock	27.0 MHz nominal
Voltage levels	Standard ECL (10K or 10KH series)
Driver impedance	Standard ECL (10K or 10KH series)
Receiver impedance	110 ohms nominal, balanced

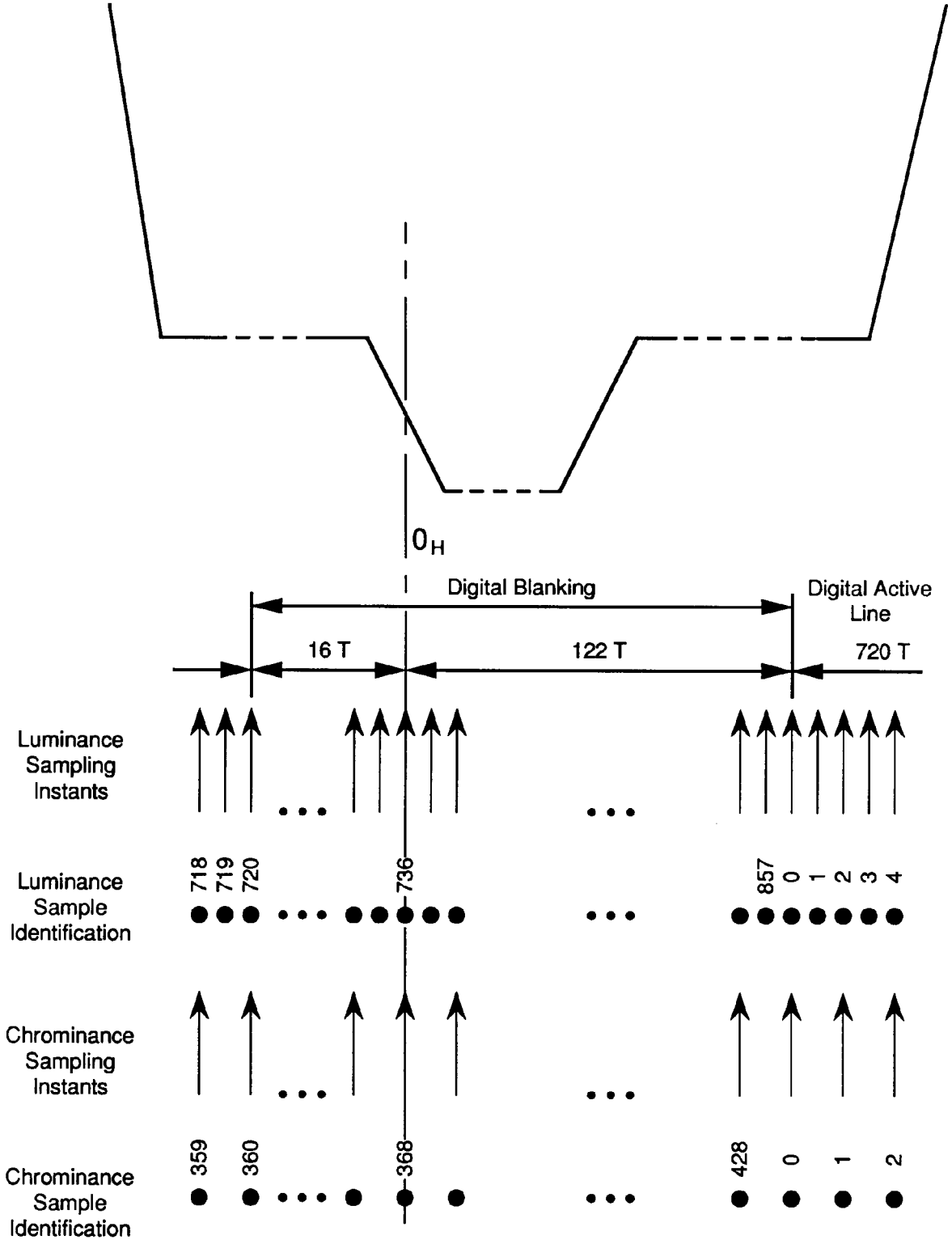


Figure 2a — Horizontal sync relationship

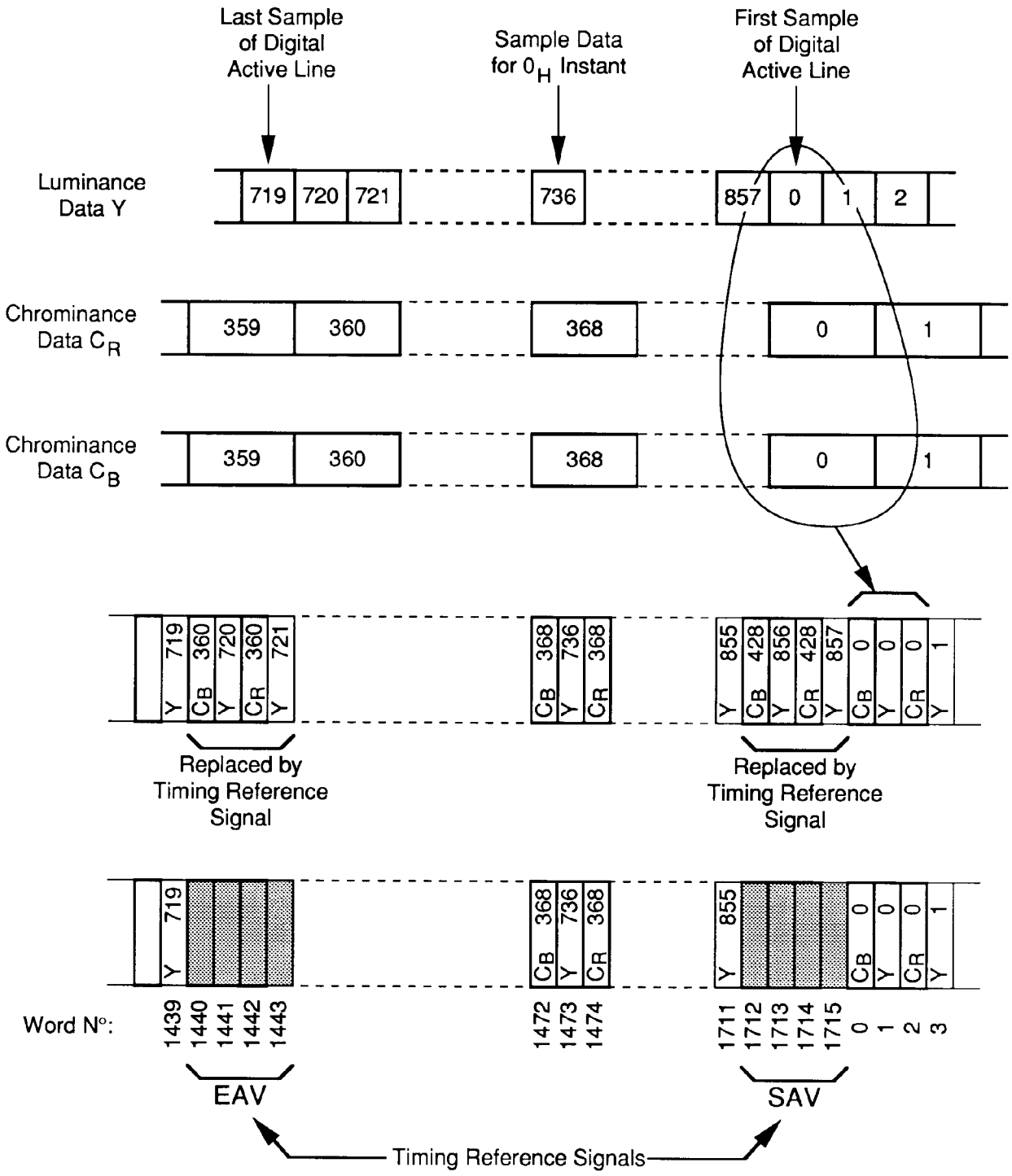


Figure 2b — Multiplex structure

3.4.2 Vertical sync relationship

Figure 3 shows the relationship between video signals in the digital and analog domains for 525-line systems.

3.5 Video data signal format

3.5.1 Data signal format

Data is transmitted across the interface on ten data pairs: DATA 0 through DATA 9. DATA 9 is the most significant bit (MSB). Of the 1024 levels (digital levels 4 through 1019 or 004_h through $3FB_h$ in the hexadecimal representation) of the ten-bit word, 1016 are used to express quantized values.

Data levels 0 to 3 and 1020 to 1023 (000_h to 003_h and $3FC_h$ to $3FF_h$ in the hexadecimal representation) are reserved to indicate timing references.

3.5.2 Multiplex structure

The video data words shall be conveyed as a 27 megaword/s multiplex in the following order:

C_B Y C_R [Y] C_B ...

where the three words C_B Y C_R refer to cosited samples, the following word [Y] being an isolated luminance only sample. The C_B and C_R samples are cosited with the first and subsequent alternate Y samples (0, 2, 4 ...) on each line (see figure 2B). The first video data word in each active line period shall be C_B.

3.5.3 Timing reference signals -- Video

Figure 2a shows the position of the timing reference signals with respect to horizontal blanking in the multiplexed data stream. It is implicit that the timing reference signals are contiguous with the video data, when present, and continue through the vertical blanking interval.

Each timing reference signal consists of a four-word sequence in the following format:

$3FF_h$ 000_h 000_h XYZ_h

Because of the existence of both 8- and 10-bit equipment, for detection purposes all values in the ranges 000_h-003_h and $3FC_h$-$3FF_h$ must be considered equivalent to 000_h and $3FF_h$, respectively.

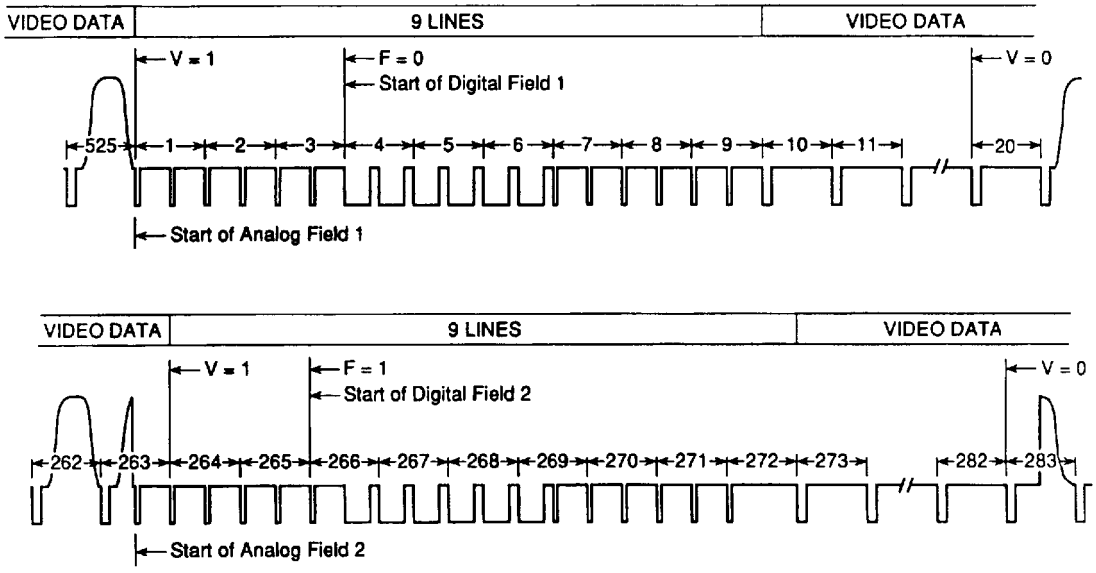


Figure 3 — Relationship of video data/vertical sync

The first three words are a fixed preamble. The fourth word shall contain information defining:

- even field (field 2) identification;
- state of vertical blanking;
- state of horizontal blanking.

Figure 4 is a spatial representation of the timing reference signals during a television frame.

Assignment of bits within the fourth word is shown in table 3. Values for F and V change in the EAV associated with the blanking interval of the line number indicated.

P0, P1, P2, and P3 have states dependent on states of bits F, V, and H according to table 4.

Lines are numbered from 1 through 525 as shown in figure 3.

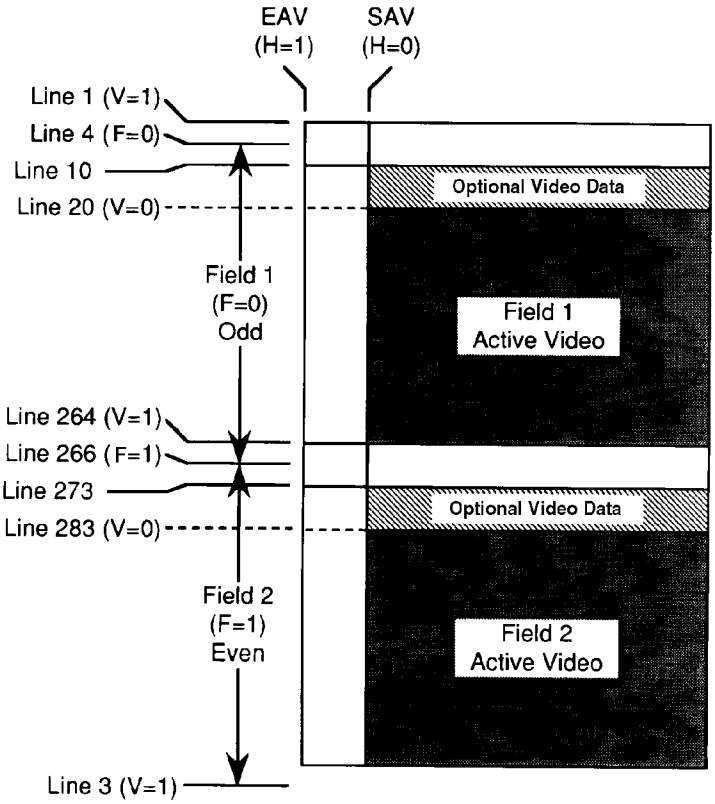
Vertical blanking in the digital interface is in full-line increments.

EAV and SAV are the digital horizontal synchronization signals and occur on every line.

The interval starting at EAV and ending with SAV is the digital horizontal blanking period as shown in figure 2b.

Small blocks of data, less than 268 words in total length, including the HANC sequence (as described in 3.6.1), can be transmitted within the horizontal blanking period on every line.

Large blocks of data, up to 1440 words in total length, including the ANC sequence, can be transmitted within the interval starting with the end of SAV and terminating with the beginning of EAV on lines 1 through 19 and 264 through 282 only.



NOTE -- Previous versions of this standard allowed the V-bit to make its transition from “1" to ”0" on any of the lines 10 (273) through 20 (283). This was to provide for active video fields greater than the nominal corresponding to NTSC operation. Designers should be aware that the “1" to ”0" transition of the V-bit may not necessarily occur on line 20 (283) in some equipment conforming to previous versions of ANSI/SMPTE 125M.

Figure 4 -- Timing reference signal locations

Table 3 — Timing reference signals

Bit	Word 1440 and 1712	Word 1441 and 1713	Word 1442 and 1714	Word 1443 and 1715	
9	1	0	0	1	Fixed
8	1	0	0	F	F = 0 during field 1 F = 1 during field 2
7	1	0	0	V	V = 0 during active video V = 1 during vertical blanking
6	1	0	0	H	H = 1 for EAV H = 0 for SAV
5	1	0	0	P3	See table 4
4	1	0	0	P2	
3	1	0	0	P1	
2	1	0	0	P0	
1	1	0	0	0	
0	1	0	0	0	

NOTES
1 Some equipments can only sense the eight most significant bits.
2 The H, V, and F bits (bits 6-8) provide all the necessary state information. Bits 2-5 provide error detection and correction information.
3 Each 525-line digital video frame is divided into two fields. Field 1 contains 262 complete horizontal lines; field 2 contains 263 complete horizontal lines.
4 The protection bits allow correction of all single-bit errors and detection of two-bit errors.

Table 4 — Protection bit states

Bit	9	8	7	6	5	4	3	2	1	0
		F	V	H	P3	P2	P1	P0		
	1	0	0	0	0	0	0	0	0	0
	1	0	0	1	1	1	0	1	0	0
	1	0	1	0	1	0	1	1	0	0
	1	0	1	1	0	1	1	0	0	0
	1	1	0	0	0	1	1	1	0	0
	1	1	0	1	1	0	1	0	0	0
	1	1	1	0	1	1	0	0	0	0
	1	1	1	1	0	0	0	1	0	0

Video data will not be present on lines 1-9 and 264-272 and may optionally be present on lines 10-19 and 273-282. Ancillary data could be optionally transmitted in the active portion of these lines.

The words during:

- horizontal blanking period on every line;
- the active portion of lines 1-9 and 264-272;
- the active portion of lines 10-19 and 273-282 (when video data is not present);

not used to transmit ancillary data must have the following values:

- the words corresponding to Y samples must have the value 040_h;

- the words corresponding to C_B and C_R samples must have the value 200_h.

3.6 Ancillary data signal format

Ancillary data may be inserted in any portion of the data stream not occupied by timing reference signals or video data (see 3.4.1 and 3.4.2). Two categories of ancillary data, HANC and VANC, are defined for different portions of the data stream. Note that the three-word header used to identify ancillary data is the same for HANC and VANC, although 8-bit representation of the header is permitted for VANC only.

3.6.1 HANC data

HANC data are permitted in all horizontal intervals, but not in the active portion of lines. HANC data are of 10-bit format, and each block of HANC data is preceded by the three-word ancillary data header

000_h $3FF_h$ $3FF_h$

Because of the existence of both 8- and 10-bit equipment, for detection purposes all values in the ranges 000_h-003_h and $3FC_h$-$3FF_h$ must be considered equivalent to 000_h and $3FF_h$, respectively.

The ancillary data header may occur multiple times during each horizontal blanking period if different blocks of data are transmitted.

All permitted data identification words and data formats will protect the values (000_h to 003_h) and ($3FC_h$ to $3FF_h$).

3.6.2 VANC data

VANC data are permitted only in the active portion of lines 1-13, 15-19, 264-276, and 278-282. (Lines 14 and 277 are reserved for digital vertical interval time code (DVITC) and video index. VANC data are of 8-bit format, and each block of VANC data is preceded by the three-word ancillary data header

000_h $3FF_h$ $3FF_h$

Because of the existence of both 8- and 10-bit equipment, for detection purposes all values in the ranges 000_h-003_h and $3FC_h$-$3FF_h$ must be considered equivalent to 000_h and $3FF_h$, respectively.

The ancillary data header may occur multiple times during each line period if different blocks of data are transmitted.

All permitted data identification words and data formats will protect the values (000_h to 003_h) and ($3FC_h$ to $3FF_h$).

3.7 Digital vertical interval time code and video index

Digital vertical interval time code (DVITC) and video index, if present, are carried by the data in the active portion of lines 14 and 277.

3.7.1 DVITC

This signal, if present, is carried by the luminance data in the active portion of lines 14 and 277.

3.7.2 Video index

This signal, if present, is carried by the color-difference data in the active portion of lines 14 and 277. A total of 90 8-bit data words is represented serially by DATA(2) of the 720 color-difference samples of the active portion of the line.

The first color-difference word of the active portion of the line (word 0 of the multiplexed signal, normally a C_B sample) represents the least significant bit (bit 0) of video index word 0. The second color-difference word represents bit 1 of the same word, etc. The last color-difference word of the active portion of the line

(word 1438 of the multiplexed signal, normally a C_R sample) represents the most significant bit (bit 7) of video index word 89.

For all samples, a value of 204_h represents a binary "one" for the appropriate video index bit, and a value of 200_h represents a binary "zero" for the appropriate video index bit.

This transmission method ensures that, after digital to analog conversion, the video signal may be sent to an NTSC encoder without any requirement for special blanking. DVITC will be preserved through the encoder without interference from any video index information which may be present.

3.8 Clock signal

3.8.1 Clock signal description (at transmitter)

The clock signal is a 27-MHz square wave as shown in figure 5. The clock pulse width (tw) is 18.5 ns ± 3 ns.

3.8.2 Clock jitter

The peak-to-peak jitter between rising edges shall be within 3 ns of the average time of the rising edge computed over at least one field.

NOTE – This jitter specification, while appropriate for an effective parallel interface, is not suitable for clocking digital-to-analog conversion or parallel-to-serial conversion.

3.8.3 Clock data timing relationship

The positive transition of the clock signal nominally occurs midway between data transitions (figure 5).

4 Electrical characteristics

4.1 General

The eleven signals shall be transmitted via balanced signal pairs.

Although the use of ECL technology is not specified, the line driver and receiver must be ECL-compatible to permit the use of standard ECL parts for either or both ends in applications where such ECL parts are deemed adequate.

Standard ECL parameters are provided in annex A.

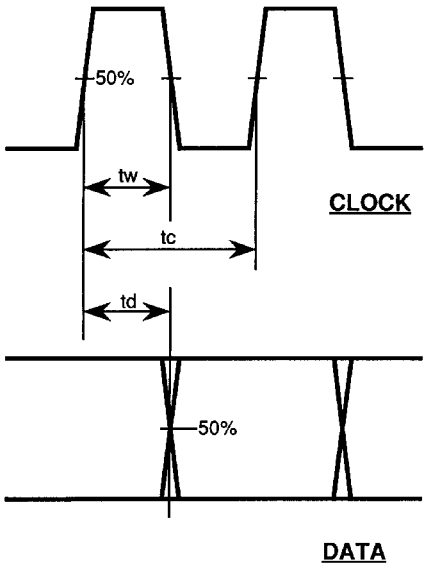
4.2 Transmitter characteristics

4.2.1 Output impedance

The transmitter shall have a balanced output with a maximum output impedance of 110 ohms.

4.2.2 Common mode voltage

The average of the voltages on the two terminals of the line driver shall be –1.3 V ± 15% with reference to the ground terminal.



tw = 18.5 ns ± 3 ns

$tc = \frac{1}{1716\ f_h} = 37$ ns (nominal)

td = 18.5 ns ± 3 ns

f_h = 15.734...KHz (nominal)

Figure 5 — Clock to data timing (at transmitter)

4.2.3 Signal amplitude

The generated signal shall lie between 0.8 V peak-to-peak and 2.0 V peak-to-peak, measured across a 110-ohm resistor connected to the output terminals without any transmission line.

4.2.4 Rise and fall times

Rise and fall times shall be no longer than 5 ns and shall differ by not more than 2 ns, as measured between the 20% and 80% amplitude points across a 110-ohm resistor connected to the output terminals without any transmission line.

4.3 Receiver characteristics

4.3.1 Terminating impedance

The cable shall be terminated by 110 ohms ± 10 ohms.

4.3.2 Maximum input signal

The line receiver must sense properly the binary data when connected directly to a line driver operating at the extreme voltage limits permitted by 4.2.3.

4.3.3 Input sensitivity

The receiver shall require a differential input voltage of no more than 185 mV to correctly attain the intended binary state.

4.3.4 Common mode rejection

The receiver shall operate correctly in the presence of common mode noise having a maximum amplitude of ± 0.5 V.

4.3.5 Differential delay

The receiver shall operate with a differential delay between the received clock and any received data signals up to 11 ns.

5 Mechanical characteristics

5.1 General

This clause defines the mechanical specifications for the interface of digital video systems used in environments where the physical distance between devices is limited and the general physical environment can be termed “interior.”

5.2 Interconnecting cable characteristics

The interface is designed to operate with a nominal signal pair impedance of 110 ohms.

5.2.1 Cable length

The majority of applications of this interface involve lengths less than 50 m. For these lengths, cables with reasonable uniformity will generally give satisfactory results. For cable lengths greater than 50 m, the cable and termination characteristics become more critical, in some cases requiring equalization.

5.2.2 Cable construction

The cable shall contain 12 pairs of conductors of which 11 pairs shall be used as signal lines. The remaining pair shall be used as system ground.

The cable shall be constructed to minimize the effects of crosstalk between signal lines, the susceptibility of the signal lines to external noise, and the transmission of interface signals to the external environment.

The cable shall contain an overall shield to minimize radiation, carried through the cable assembly and connectors via the cable shield pins and the connector body at each end.

The cable shall be constructed to minimize the differential delay between any two conductor pairs.

5.3 Connector characteristics

5.3.1 Mechanical considerations

The connectors shall have the mechanical characteristics conforming to the industry standard 25 contact D subminiature connector described in annex B. Additional information may be found in MIL-C-24308C.

NOTE -- Most applications of this interface require that the connectors be inserted many times. ECL voltage and current levels are relatively low. The materials used in the connector should be appropriate to the application.

5.3.2 Connector contact assignments

The connector contact assignments shall be in accord with table 5.

5.3.3 Cable connector assembly

Cable connectors employ pin contacts and equipment connectors employ socket contacts (see figure 6).

Table 5 — Connector contact assignments

Pin	Signal line	Pin	Signal line
1	Clock	14	Clock return
2	System ground A	15	System ground B
3	Data 9	16	Data 9 return
4	Data 8	17	Data 8 return
5	Data 7	18	Data 7 return
6	Data 6	19	Data 6 return
7	Data 5	20	Data 5 return
8	Data 4	21	Data 4 return
9	Data 3	22	Data 3 return
10	Data 2	23	Data 2 return
11	Data 1	24	Data 1 return
12	Data 0	25	Data 0 return
13	Cable shield		

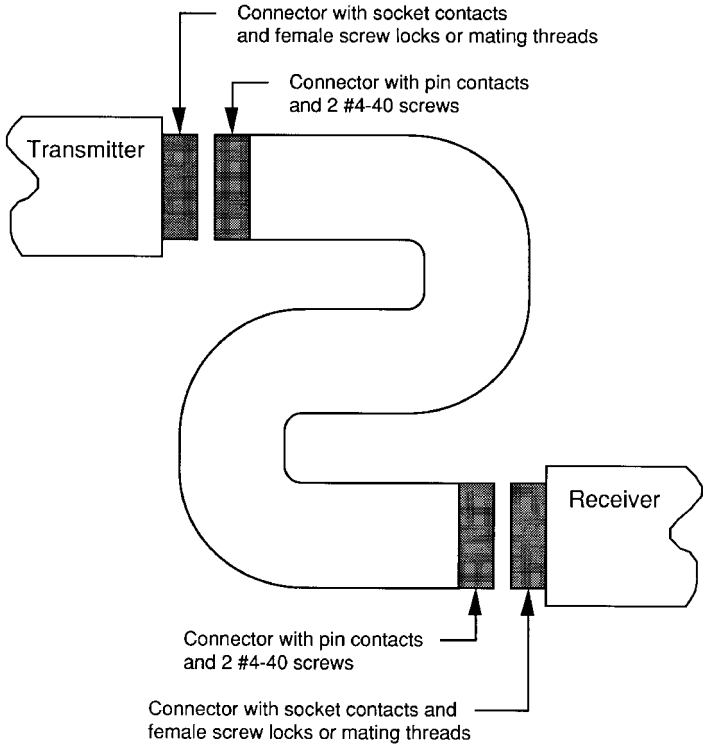


Figure 6 — Cable connector assembly

5.3.4 Connector retaining mechanism

The cable connectors shall be provided with #4-40 mounting screws and the equipment connectors shall be provided with female screw locks or with mating threads as shown in annex B.

Annex A (normative)
ECL 10,000 and 10H000 parameters

A.1 Standard ECL parameters

"Standard ECL" in this application means an integrated circuit device of the ECL 10,000 or 10H000 series or equivalent. Typical key parameters are:

System power supply (V): --4.7 V to --5.7 V; --5.2 V nominal

Logic states with respect to ground (typical): "1" = --0.8 V = High (H); "0" = --1.85 V = Low (L)

Output impedance: Open emitter-follower output (7 ohm typical) to drive terminated lines

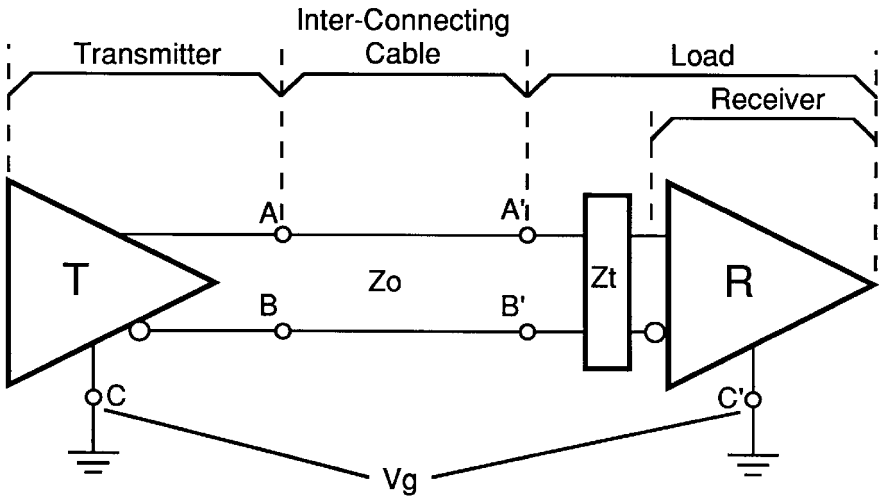
Propagation delay ECL 10,000: 2-3 ns per gate; typical edge speeds are 2-3 ns (20% to 80%)

Propagation delay ECL 10H000: 1-2 ns per gate; typical edge speeds are 1-2 ns (20% -- 80%)

A.2 Balanced interface circuit

Each circuit consists of three parts as shown in figure A.1: the line driver, the balanced interconnecting cable, and the load. The line driver is comprised of a single transmitter (T) with a low-output impedance. The load is comprised of a single receiver (R), and a cable termination impedance (Zt).

Electrical characteristics of the receiver without cable termination shall conform to standard balanced ECL specifications. Use of a cable termination (Zt) is mandatory. Zt shall be nominally 110 ohms.



A, A′ = data line
B, B′ = return line
Zt = cable termination
A, B = transmitter interface points
A′, B′ = load interface points
C = transmitter circuit ground
C′ = load circuit ground
Vg = ground potential difference
Zo = cable characteristic impedance

Figure A.1 — Balanced interface circuit

Annex B (normative)
Connector characteristics

The interface employs the 25 contact D subminiature connector, with the connectors on the transmitter and receivers using socket contacts and the connectors on the cable both using pin contacts. Connectors are locked together by two #4-40 screws on the cable connectors, which go in female screw locks mounted on the equipment connector.

Detailed dimensions for the connector are given in MIL-C-24308C.

The relative position of the connector and the female screw lock is defined in figure B.1. Recommended minimum connector spacing is defined in figure B.2.

It is recommended that the cable connectors employ a conductive backshell to maintain shielding of the signal conductors. Care must be taken to select designs that are appropriate for use with the screw-latching method specified.

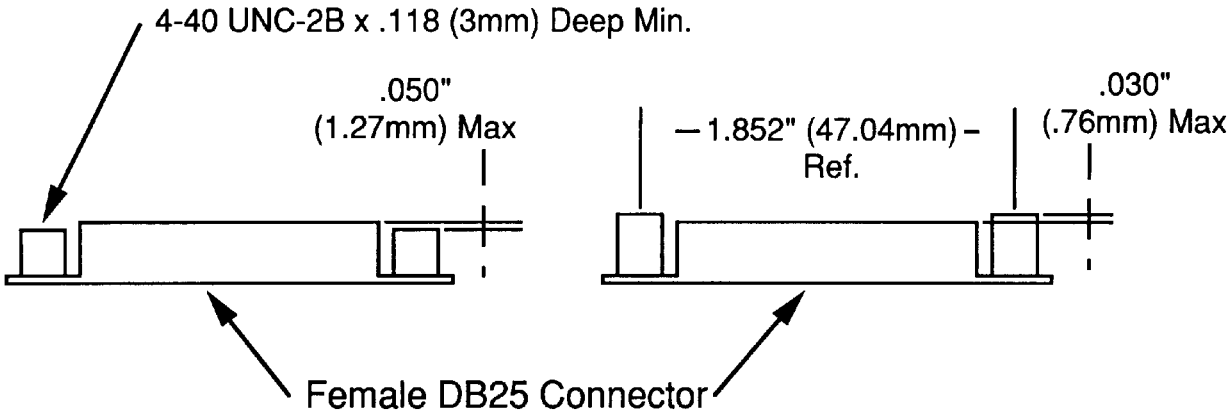


Figure B.1 — Female screw lock mounting

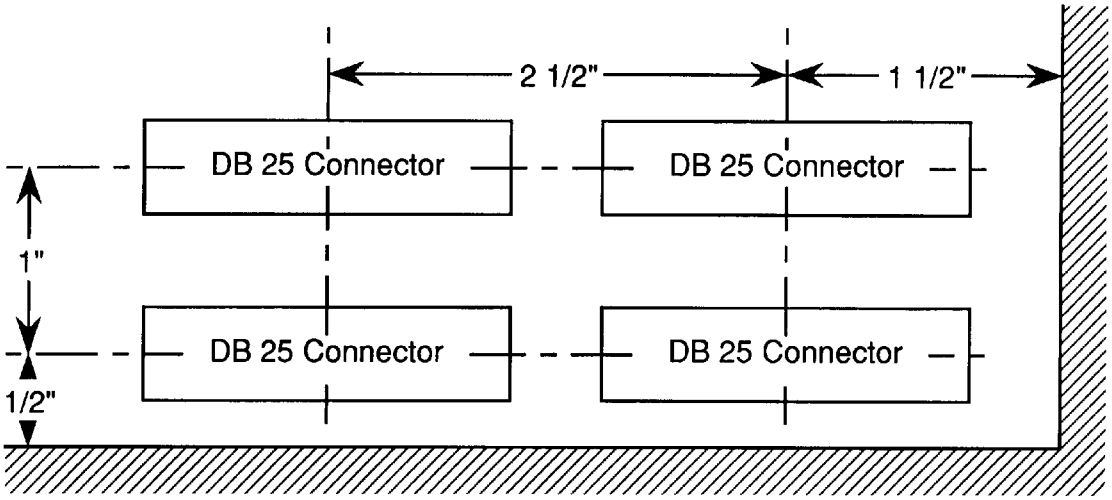


Figure B.2 — Minimum connector spacing

Annex C (informative)
Cable shield pin

The cable shield (pin 13) is for the purpose of controlling electromagnetic radiation from the cable. It is recommended that pin 13 provide high-frequency continuity to the chassis ground at both ends and, in addition, provide dc continuity to the chassis ground at the transmit end.

Annex D (informative)
Connector orientation

Vertical or horizontal mounting: Contact 1 uppermost.

Annex E (informative)
Monochrome operation

Monochrome operation at 29.97 Hz frame rate can be achieved by setting the color-difference signals (C_B, C_R) to zero (200_h).

Annex F (informative)
Error detection and correction in the video timing reference signal

Table F.1 enables single bit errors in the fourth bytes of EAV and SAV to be corrected. Double errors, and some multiple-bit errors, are detected but not corrected. The table gives corrected values for bits 8, 7, and 6 where possible. Multiple errors are denoted by asterisks.

Table F.1 — Error correction table

Received P3 -- P0	Received bits 8, 7, and 6 (F, V, and H)							
	000	001	010	011	100	101	110	111
0000	000	000	000	*	000	*	*	111
0001	000	*	*	111	*	111	111	111
0010	000	*	*	011	*	101	*	*
0011	*	*	010	*	100	*	*	111
0100	000	*	*	011	*	*	110	*
0101	*	001	*	*	100	*	*	111
0110	*	011	011	011	100	*	*	011
0111	100	*	*	011	100	100	100	*
1000	000	*	*	*	*	101	110	*
1001	*	001	010	*	*	*	*	111
1010	*	101	010	*	101	101	*	101
1011	010	*	010	010	*	101	010	*
1100	*	001	110	*	110	*	110	110
1101	001	001	*	001	*	001	010	*
1110	*	*	*	011	*	101	110	*
1111	*	001	010	*	100	*	*	*

Annex G (informative)
Correspondence between this standard and previous (8-bit) specifications of the interface

Table G.1 shows the connector pinout correspondence between the old 8-bit system and the new 10-bit system.

Earlier specifications of this interface did not require that Data A and Data B be driven by the transmitter, or that electrical continuity be maintained on pins 11, 12, 24, and 25. Designers of equipment and systems should be aware that system components built to earlier specifications may result in floating inputs for DATA (0-1).

When a 10-bit signal is received by an 8-bit device, simple truncation or rounding may result in spatial correlation of the noise introduced and visible “striations” in the displayed picture. Designers of equipment and systems should consider the use of techniques such as randomized rounding, if appropriate to their application, when the number of bits must be reduced.

Table G.1 — Connector pinout correspondence

Old 8-bit system	Connector pin number	New 10-bit system
Clock	1	Clock
System ground A	2	System ground A
Data 7 (MSB)	3	Data 9 (MSB)
Data 6	4	Data 8
Data 5	5	Data 7
Data 4	6	Data 6
Data 3	7	Data 5
Data 2	8	Data 4
Data 1	9	Data 3
Data 0	10	Data 2
Data A	11	Data 1
Data B	12	Data 0
Cable shield	13	Cable shield
Clock return	14	Clock return
System ground B	15	System ground B
Data 7 return	16	Data 9 return
Data 6 return	17	Data 8 return
Data 5 return	18	Data 7 return
Data 4 return	19	Data 6 return
Data 3 return	20	Data 5 return
Data 2 return	21	Data 4 return
Data 1 return	22	Data 3 return
Data 0 return	23	Data 2 return
Data A return	24	Data 1 return
Data B return	25	Data 0 return

Annex H (informative)
Bibliography

ITU-R BT.601-4, Encoding Parameters of Digital Television for Studios

ITU-R Report 962-1, The Filtering, Sampling and Multiplexing for Digital Encoding of Colour Television Signals

MIL-C-24308C, Connectors, Electric, Rectangular, Nonenvironmental, Miniature, Polarized Shell, Rack and Panel, General Specification for

Documents are in preparation to cover auxiliary signals (HANC, VANC, DVITC, and video index) but are not yet available.