SMPTE STANDARD

SMPTE 274M-2008
Revision of
SMPTE 274M-2005

for Television — 1920 x 1080 Image Sample Structure, Digital Representation and Digital Timing Reference Sequences for Multiple Picture Rates

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Approved
January 29, 2008

Foreword

SMPTE (the Society of Motion Picture and Television Engineers) is an internationally recognized standard developing organization. Headquartered and incorporated in the United States of America, SMPTE has members in over 80 countries on six continents. SMPTE's Engineering Documents, including Standards, Recommended Practices and Engineering Guidelines, are prepared by SMPTE's Technology Committees. Participation in these Committees is open to all with a bona fide interest in their work. SMPTE cooperates closely with other standards-developing organizations, including ISO, IEC and ITU.

SMPTE Engineering Documents are drafted in accordance with the rules given in Part XIII of its Administrative Practices.

SMPTE Standard 274M was prepared by Technology Committee N26.

1 Scope

1.1 This standard defines a family of image sample structures for the representation of stationary or moving two-dimensional images sampled temporally at a constant frame rate and having an image format (sample structure) of 1920 x 1080 and an aspect ratio of 16:9 as given in Table 1. This standard specifies:

– R'G'B' color encoding;
– R'G'B' analog and digital representation;
– $Y'P'_BP'_R$ color encoding, analog representation and analog interface; and
– $Y'C'_BC'_R$ color encoding and digital representation

An auxiliary component A may optionally accompany R'G'B' and $Y'C'_BC'_R$; these interfaces are denoted R'G'B'A and $Y'C'_BC'_R$ A. The "A" component if present shall have the same characteristics as the Y' or G' channel.

1.2 This standard specifies multiple frame and field rate formats (Table 1) and eight-bit, ten-bit and twelve-bit systems. It is not necessary for an implementation to support all formats to be compliant with this standard. However, an implementation must state which of the formats are supported. Interfaces for twelve-bit systems require more than a single link.

NOTE – For international program interchange, constrained parameters as defined in ITU-R BT 709 shall be used.

1.3 Annex A of this standard defines the segmented frame interface for progressive signals using the 1920x1080 sampling structure.

Table 1 – Image sample structure and frame rates

System No.	System nomenclature	Luminance or R'G'B' samples per active line (S/AL)	Active lines per frame (AL/F)	Frame rate (Hz)	Interface sampling frequency fs (MHz)	Luminance sample periods per total line (S/TL)	Total lines per frame
1	1920 x 1080/60/P	1920	1080	60	148.5	2200	1125
2	1920 x 1080/59.94/P	1920	1080	$\frac{60}{1.001}$	$\frac{148.5}{1.001}$	2200	1125
3	1920 x 1080/50/P	1920	1080	50	148.5	2640	1125
4	1920 x 1080/60/I	1920	1080	30	74.25	2200	1125
5	1920 x 1080/59.94/I	1920	1080	$\frac{30}{1.001}$	$\frac{74.25}{1.001}$	2200	1125
6	1920 x 1080/50/I	1920	1080	25	74.25	2640	1125
7	1920 x 1080/30/P	1920	1080	30	74.25	2200	1125
8	1920 x 1080/29.97/P	1920	1080	$\frac{30}{1.001}$	$\frac{74.25}{1.001}$	2200	1125
9	1920 x 1080/25/P	1920	1080	25	74.25	2640	1125
10	1920 x 1080/24/P	1920	1080	24	74.25	2750	1125
11	1920 x 1080/23.98/P	1920	1080	$\frac{24}{1.001}$	$\frac{74.25}{1.001}$	2750	1125

NOTE – Throughout this standard, references to signals represented by a single letter, e.g., R', G' and B', are equivalent to the nomenclature in earlier documents of the form E'_R, E'_G, and E'_B, which, in turn, refer to signals to which the transfer characteristics given in Section 6 have been applied. Such signals are commonly described as being gamma corrected.

2 Conformance Notation

Normative text is text that describes elements of the design that are indispensable or contains the conformance language keywords: "shall", "should", or "may". Informative text is text that is potentially helpful to the user, but not indispensable, and can be removed, changed, or added editorially without affecting interoperability. Informative text does not contain any conformance keywords.

All text in this document is, by default, normative, except: the Introduction, any section explicitly labeled as "Informative" or individual paragraphs that start with "Note:"

The keywords "shall" and "shall not" indicate requirements strictly to be followed in order to conform to the document and from which no deviation is permitted.

The keywords, "should" and "should not" indicate that, among several possibilities, one is recommended as particularly suitable, without mentioning or excluding others; or that a certain course of action is preferred but not necessarily required; or that (in the negative form) a certain possibility or course of action is deprecated but not prohibited.

The keywords "may" and "need not" indicate courses of action permissible within the limits of the document.

The keyword “reserved” indicates a provision that is not defined at this time, shall not be used, and may be defined in the future. The keyword “forbidden” indicates “reserved” and in addition indicates that the provision will never be defined in the future.

A conformant implementation according to this document is one that includes all mandatory provisions ("shall") and, if implemented, all recommended provisions ("should") as described. A conformant implementation need not implement optional provisions ("may") and need not implement them as described.

3 Normative References

The following standards contain provisions which, through reference in this text, constitute provisions of this standard. At the time of publication, the editions indicated were valid. All standards are subject to revision, and parties to agreements based on this standard are encouraged to investigate the possibility of applying the most recent edition of the standards listed below.

CIE Publication 15:2004, Colorimetry, Third Edition

IEC 61169-8 (2007-02)[1], Radio Frequency Connectors, Part 8: Sectional Specification — R.F. Coaxial Connectors with Inner Diameter of Outer Conductor 6,5 mm (0,256 in) with Bayonet Lock — Characteristics Impedance 50 Ohm (Type BNC), Annex A (Normative) — Information for Interface Dimensions of 75 Ohm Characteristic Impedance Connector with Unspecified Reflection Factor

SMPTE 291M-2006, Television — Ancillary Data Packet and Space Formatting

SMPTE RP 160-1997, Three-Channel Parallel Analog Component High-Definition Video Interface

[1] Please note that the title of this normative reference may be misleading. This standard requires the use of the 75-ohm connector defined in this reference.

4 General

4.1 The specification of a system claiming compliance with this standard shall state:

– which of the systems of Table 1 are implemented;

– which of the signal interfaces are implemented (R'G'B', $Y'P'_BP'_R$, $Y'C'_BC'_R$, R'G'B'A or $Y'C'_BC'_RA$); and

– whether the digital representation employs uniformly quantized (linear), PCM, 8 bits, 10 bits or 12 bits.

4.2 A 10-bit or 12-bit codeword, when converted to a smaller number of sampling bits, should either be rounded or truncated. An eight-bit or ten-bit codeword, when converted to a larger number of sampling bits, should have either two or four padding bits added.

5 Image Structure

5.1 The 1920x1080 image structure defined in this standard shall be mapped onto an interface that contains 1125 total lines as shown in Figures 1 and 2. The Interface sampling frequency shall be maintained to a tolerance of ± 10 ppm.

5.2 A frame shall comprise the indicated total number of lines; each line at the interface shall be of equal duration determined by the interface sampling frequency and the luminance samples per total line (S/TL).

Raster pixel representation at the interface shall be presented from left to right, and in the raster shall be presented from top to bottom. Lines are numbered in time sequence according to the raster structure described in Section 7 and shown in Figures 1 and 2.

5.3 Timing instants in each line shall be defined with respect to a horizontal datum denoted by 0_H which is established by horizontal synchronizing (sync) information in Sections 9 and 10. Each line shall be represented by a number of samples, equally spaced, as indicated by the column S/TL in Table 1. The time between any two adjacent sample instants is called the reference clock interval T.

5.4 A progressive system shall convey 1080 active picture lines per frame in order from top to bottom.

5.5 An interlaced system shall capture the image, as a first field then as a second field, in which the lines of each field have twice the vertical spatial sampling pitch of the frame. Lines in the second field shall be displaced vertically by the vertical sampling pitch and the line timing shall be delayed temporally by half the frame time from the lines in the first field.

The first field shall convey 540 active lines, starting with the top picture line of the frame. The second field shall convey 540 active picture lines, ending with the bottom picture line of the frame.

6 System Colorimetry

6.1 Equipment should be designed in accordance with the colorimetric analysis and opto-electronic transfer function defined in this section. This corresponds to ITU-R BT.709. Designers and users should be aware that some legacy material in this format was originally created using the SMPTE 240M standard, which has different colorimetry. However, the differences between the two are so small that they can be ignored, except for precision test materials.

6.2 Picture information shall be linearly represented by red, green and blue tristimulus values (RGB), lying in the range 0 (reference black) to 1 (reference white), whose colorimetric attributes are based upon reference primaries with the following chromaticity coordinates, in conformance with ITU-R BT.709, and whose reference white conforms to CIE D65 as defined by CIE 15:

	CIE *x*	CIE *y*
Red primary	0.640	0.330
Green primary	0.300	0.600
Blue primary	0.150	0.060
Reference white	0.3127	0.3290

6.3 From the red, green and blue tristimulus values, three nonlinear primary components R', G' and B' shall be computed according to the optoelectronic transfer function of ITU-R BT.709, where L denotes a tristimulus value and V' denotes a nonlinear primary signal:

$$V' = \begin{cases} 4.5L, & 0 \leq L < 0.018 \\ 1.099L^{0.45} - 0.099, & 0.018 \leq L \leq 1 \end{cases}$$

6.4 To ensure the proper interchange of picture information between analog and digital representations, signal levels shall be completely contained in the range specified between reference black and reference white specified in Sections 8.7 and 11.5, except for overshoots and undershoots due to processing.

6.5 The Y' component shall be computed as a weighted sum of nonlinear R'G'B' primary components, using coefficients calculated from the reference primaries according to the method given in SMPTE RP 177:

$$Y' = 0.2126\ R' + 0.7152\ G' + 0.0722\ B'$$

NOTE – Because the Y' component is computed from nonlinear R'G'B' primary components, rather than from the linear tristimulus RGB values, it does not represent the true luminance value of the signal, but only an approximation. For more information, see *Poynton, Charles, A Technical Introduction to Digital Video* (Annex F).

6.6 Color-difference component signals P'_B and P'_R having the same excursion as the Y' component shall be computed as follows:

$$P'_B = \frac{0.5}{1 - 0.0722}(B' - Y')$$

$$P'_R = \frac{0.5}{1 - 0.2126}(R' - Y')$$

P'_B and P'_R are filtered and may be coded as C'_B and C'_R components for digital transmission. Example filter templates are given in Figure D.2.

7 Raster Structure

NOTE ON INTERLACED VERSIONS – All of the image structure systems defined in this document require at the interface a total of 1125 lines per picture. In an analog-only system, this would normally imply that the interlaced versions would divide this total into two equal-length fields of 562½ lines each. However, because a digital interface must also be supported, only whole numbers of lines in each field are allowed, in order to permit unambiguous identification of lines by the digital timing reference sequences (see Section 9). Therefore the interlaced versions define integer, and hence unequal, numbers of lines (563 and 562) in each of the two fields comprising one frame. Analog vertical sync sequences, however, must remain equally spaced in time and are therefore not fully aligned to the fields as defined for the digital interface. This results in the analog vertical sync for the second digital field beginning one half-line before the end of the first digital field.

7.1 For details of vertical timing, see Figures 1 and 2.

7.2 In a progressive system, the assignment of lines within a frame shall be:

– Vertical blanking: lines 1 though 41 inclusive (including vertical sync, lines 1 through 5 inclusive) and lines 1122 through 1125; and

– Picture: 1080 lines, 42 through 1121 inclusive.

7.3 In an interlaced system, the first field shall comprise 563 lines including:

– Vertical blanking: lines 1 though 20 inclusive and lines 561 through 563; and

– Picture: 540 lines, 21 through 560 inclusive.

The second field shall comprise 562 lines, including:

– Vertical blanking: lines 564 through 583 inclusive and lines 1124 and 1125; and

– Picture: 540 lines, 584 through 1123 inclusive.

Interlaced analog vertical sync shall be located on lines 1 through 5 for the first field and from halfway through line 563 to halfway through line 568 for the second field.

7.4 During time intervals not otherwise used, the R’, G’, B’ or Y’, P'_B, C'_B, P'_R and C'_R components shall have a blanking level corresponding to zero.

7.5 The production aperture defines a region 1920 samples by 1080 lines. The horizontal extent of the production aperture shall have the 50% point of its leading transition at reference luminance sample 0 and the 50% point of its trailing transition at luminance sample 1919. The production aperture defines the maximum extent of picture information. For further information, consult informative Annex E.

7.6 The clean aperture of the picture defines a region 1888 samples in width by 1062 lines high, symmetrically located in the production aperture. The clean aperture shall be substantially free from transient effects due to blanking and picture processing.

7.7 The aspect ratio of the image represented by the production aperture and the clean aperture shall be 16:9. The sample aspect ratio is 1:1 (square pixels).

7.8 The center of the picture shall be located at the center of the 1920x1080 sample structure, midway between sample number 959 and 960, and midway between lines 581 and 582 in a progressive system, and midway between lines 291 and 853 in an interlaced and segmented frame system.

7.9 Each edge of the picture width, measured at the 50% amplitude point, shall lie within six reference clock intervals of the production aperture.

NOTE – Ancillary signals, as distinct from ancillary data, may be conveyed in a progressive system during lines 7 through 41 inclusive, and in an interlaced system during lines 7 through 20 inclusive and lines 569 through 583 inclusive. The portion within each of these lines that may be used for ancillary data is defined in Annex B.3. Ancillary signals shall not convey picture information although they may be employed to convey other related or unrelated signals, coded similarly to picture information. Further specifications of ancillary signals is outside the scope of this standard.

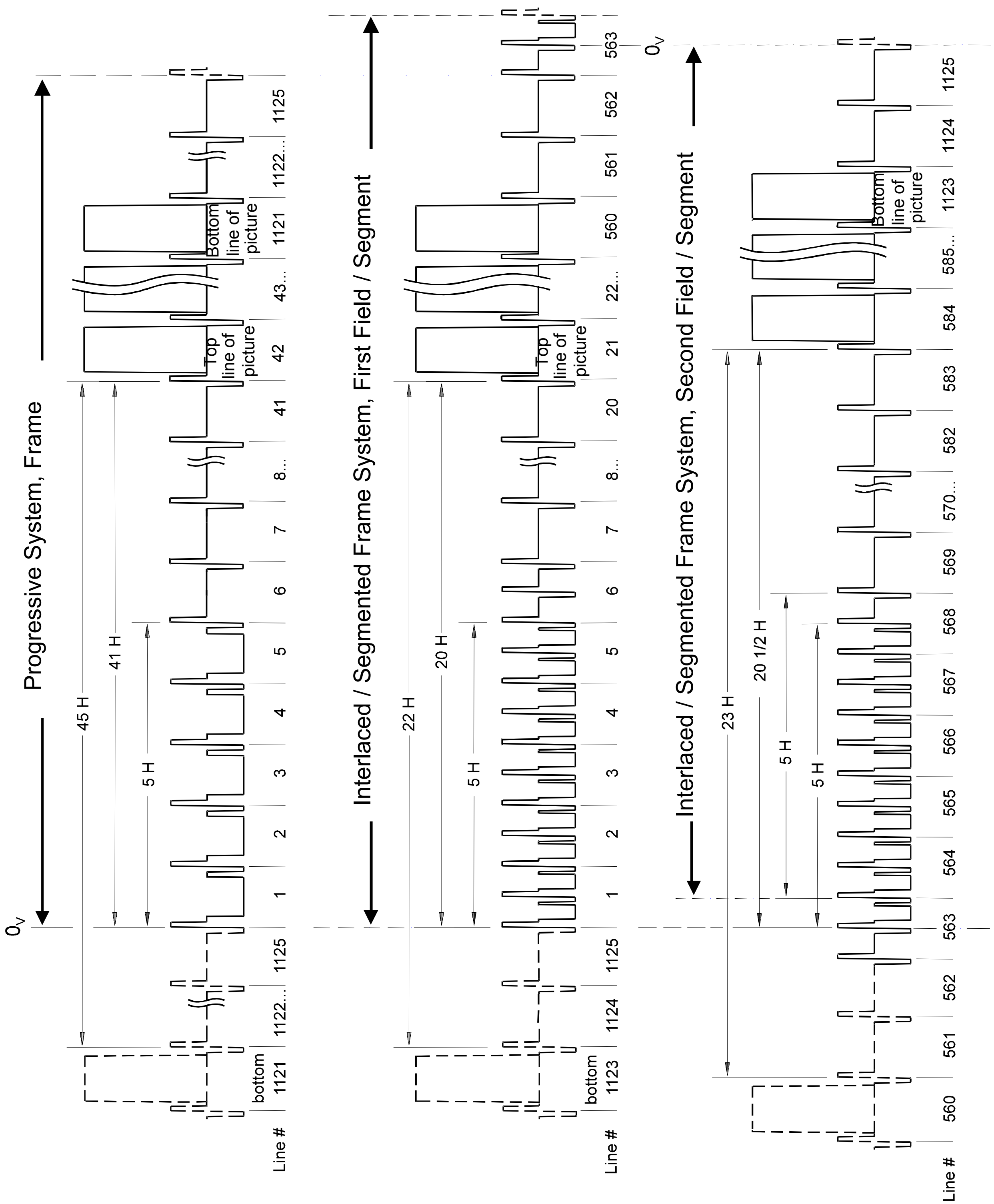


Figure 1 – Analog interface, vertical timing details

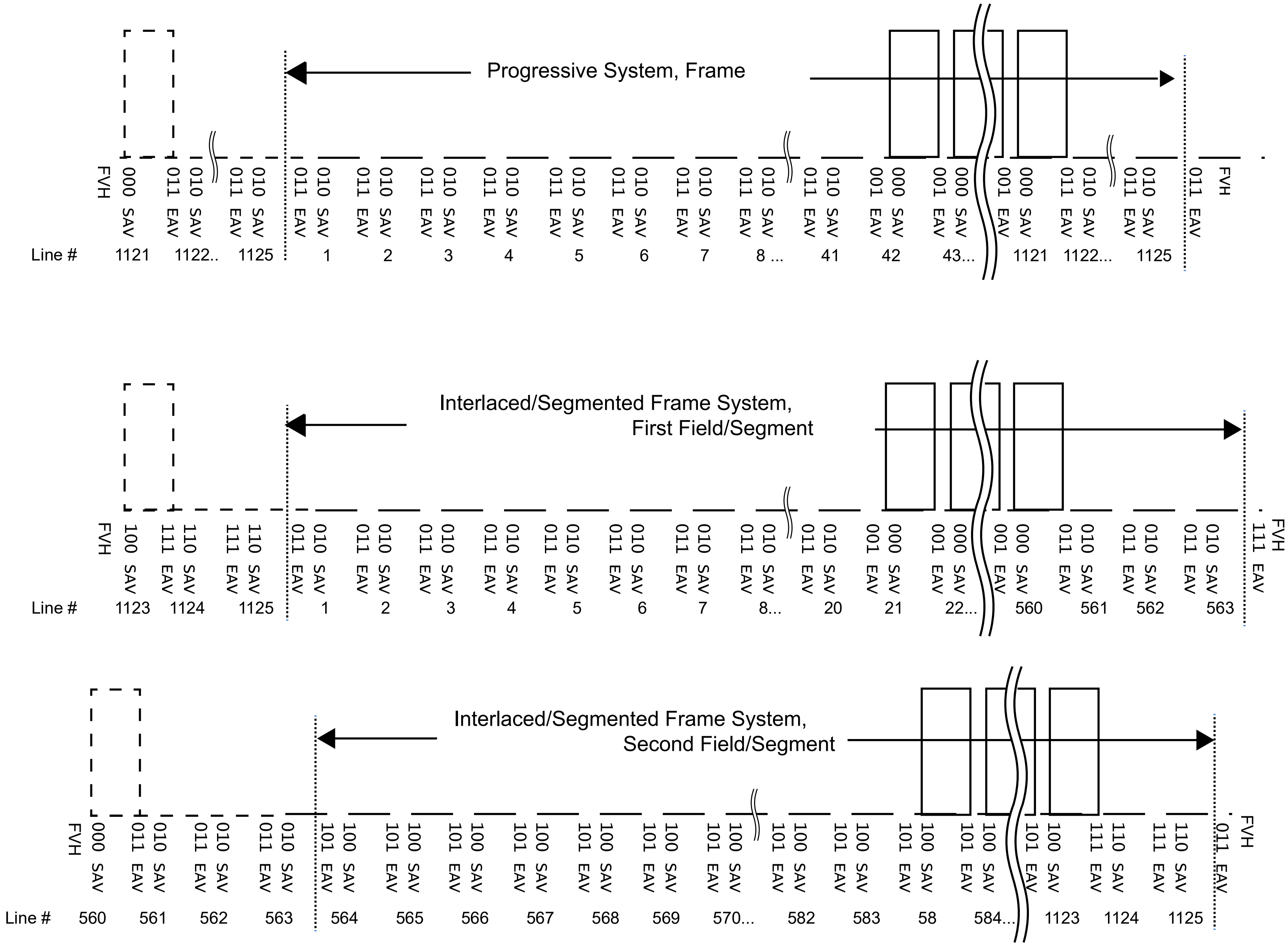


Figure 2 - Digital interface, Vertical timing details

8 Digital Picture Representation

8.1 Digital representation shall employ either R'G'B' or $Y'C'_BC'_R$ components as defined in Section 6, uniformly sampled.

8.2 The digital signals described here are assumed to have been filtered to reduce or prevent aliasing upon sampling (see Annex D).

8.3 R'G'B' signals and Y´ signals shall have a nominal bandwidth of 60 MHz for systems 1, 2 and 3 in Table 1 and 30 MHz for systems 4 through 11. $C'_BC'_R$ shall have bandwidth nominally half that of the associated Y' signal in the case of a 4:2:2 system and the same bandwidth as the associated Y' signal in the case of a 4:4:4 system as shown in Table 2.

8.4 R'G'B' signals and the Y' signal of the $YC'_BC'_R$ interface shall be sampled orthorgonally, line- and picture-repetitive. The interface sampling frequency fs shall be as shown in Table 2. The period of the sampling clock shall be denoted T. R'G'B' samples shall be cosited with each other.

8.5 A sampling instant in a line is denoted in this standard by a number from 0 through one less than the total number of samples in a line. Sample number zero corresponds to the first active video sample. The sample numbering is shown in Figure 3.

8.6 Sampled data at the interface shall be such that appropriate sin(x)/x correction occurs during conversion of the signal to the analog domain.

8.7 Digital R'G'B' and Y' components shall be computed as follows:

$$L'_D = \text{Floor}(219DL' + 16D + 0.5);\ D = 2^{n-8}$$

where L' is the component value in abstract terms from zero to unity, n takes the value 8, 10 or 12 corresponding to the number of bits to be represented, and L'_D is the resulting digital code. The unary function floor yields the largest integer not greater than its argument.

NOTE – This scaling places the extrema of R'G'B' and Y' components at code words 10_h(16) and EB_h(235) in an 8-bit representation, code words 040_h(64) and $3AC_h$(940) in a 10-bit representation or code words 100_h(256) and $EB0_h$(3760) in a 12-bit representation as shown in Table 3.

8.8 Digital C'_B and C'_R components of the $Y'C'_BC'_R$ set shall be computed as follows:

$$C'_D = \text{Floor}(224DC' + 128D + 0.5);\ D=2^{n-8}$$

where C' is the component value in abstract terms from -0.5 to + 0.5 and C'_D is the resulting digital code.

NOTE – This scaling places the extrema of C'_B and C'_R at 10_h(16) and $F0_h$(240) in an 8-bit representation, code words 040_h(64) and $3C0_h$(960) in a 10-bit representation or code words 100_h(256) and $F00_h$(3840) in a 12-bit representation as shown in Table 3.

8.9 C'_B and C'_R signals shall each have the same number of horizontal samples as the Y' component in the case of a 4:4:4 system but shall be horizontally subsampled by a factor of two with respect to the Y' component in the case of a 4:2:2 system as shown in table 2. C'_B and C'_R samples, when subsampled, shall be cosited with even-numbered Y' samples. The subsampled C'_B and C'_R signals shall be time-multiplexed by sample basis in the order of C'_B and C'_R. The multiplexed signal is referred to as C'_B/C'_R.

8.10 Code values having the 8 most-significant bits all zero or all one — that is, 8-bit codes 00_h(0) and FF_h(255) in the case of an 8-bit system, 10-bit codes 000_h(0) through 003_h(3) and $3FC_h$(1020) through $3FF_h$(1023) in the case of a 10-bit system, and 12-bit codes 000_h(0) through $00F_h$(15) and $FF0_h$(4080) through FFF_h(4095) in the case of a 10-bit system as shown in Table 3 — are employed for synchronizing purposes and shall be prohibited from video or ancillary data/signals.

8.11 A system having an 8-bit interface shall address the conversion of 10-bit video data to 8 bits with an appropriate process that minimizes video artifacts such as quantization noise. Ancillary data in 10-bit format shall be converted to 8-bit format by truncating the two least significant bits. In both cases, when converting 8-bit data to 10-bit data the least two significant bits of the 10-bit word shall be set to 0. Every conversion among 8-, 10- and 12-bit systems shall be handled in the same manner.

8.12 For Y', R', G' and B' signals, undershoot and overshoot in video processing may be accommodated by the use of code words 01_h(1) through $0F_h$(15) and code words EC_h(236) through FE_h(254) in an 8-bit system, code words 004_h(4) through $03F_h$(63) and code words $3AD_h$(941) through $3FB_h$(1019) in a 10-bit system, or code words 010_h(16) through $0FF_h$(255) and code words $EB1_h$(3761) through FEF_h(4079) in a 12-bit system as shown in Table 3.

For C'_B and C'_B signals, undershoot and overshoot in video processing may be accommodated by the use of code words 01_h(1) through $0F_h$(15) and code words $E1_h$(241) through FE_h(254) in an 8-bit system, code words 004_h(4) through $03F_h$(63) and code words $3C1_h$(961) through $3FB_h$(1019) in a 10-bit system, or code words 010_h(16) through $0FF_h$(255) and code words $F01_h$(3841) through FEF_h(4079) in a 12-bit system as shown in Table 3.

Table 2 – Bandwidth and interface sampling frequency

Bandwidth and sampling frequency	Signal component	Systems 1, 2 and 3 in Table 1		Systems 4 through 11 in Table 1		Note
		4:2:2	4:4:4	4:2:2	4:4:4	
Maximum bandwidth	R', G', B'	60MHz	60MHz	30MHz	30MHz	Section 8.3
	Y'	60MHz	60MHz	30MHz	30MHz	
	C'_B, C'_R	30MHz	60MHz	15MHz	30MHz	
Interface sampling frequency	R', G', B'	148.5MHz	148.5MHz	74.25MHz	74.25MHz	Section 8.4
	Y'	148.5MHz	148.5MHz	74.25MHz	74.25MHz	
	C'_B, C'_R	74.25MHz	148.5MHz	37.125MHz	74.25MHz	
Horizontal sample number	R', G', B'	1920	1920	1920	1920	Section 8.9
	Y'	1920	1920	1920	1920	
	C'_B, C'_R	960	1920	960	1920	

NOTE – Interface sampling frequency is also scaled by 1/1.001.

Table 3 – Digital representation

Items			8-bit system	10-bit system	12-bit system	Note
R', G', B', Y'		Upper	EB$_h$(235)	3AC$_h$(940)	EB0$_h$(3760)	Section 8.7
		Lower	10$_h$(16)	040$_h$(64)	100$_h$(256)	
C'$_B$, C'$_R$		Upper	F0$_h$(240)	3C0$_h$(960)	F00$_h$(3840)	Section 8.8
		Lower	10$_h$(16)	040$_h$(64)	100$_h$(256)	
Prohibited codes		Upper	FF$_h$(255)	3FC$_h$-3FF$_h$(1020-1023)	FF0$_h$-FFF$_h$(4080-4095)	Section 8.10
		Lower	00$_h$(0)	000$_h$-003$_h$(0-3)	000$_h$-00F$_h$(0-15)	
Overshoot and undershoot	G' B' R'	Upper	EC$_h$-FE$_h$(236-254)	3AD$_h$-3FB$_h$(941-1019)	EB1$_h$-FEF$_h$(3761-4079)	Section 8.12
		Lower	01$_h$–0F$_h$(1-15)	004$_h$-03F$_h$(4-63)	010$_h$-0FF$_h$(16-255)	
	C'$_B$ C'$_R$	Upper	F1$_h$-FE$_h$(241-254)	3C1$_h$-3FB$_h$(961-1019)	F01$_h$-FEF$_h$(3841-4079)	
		Lower	01$_h$-0F$_h$(1-15)	004$_h$-03F$_h$(4-63)	010$_h$-0FF$_h$(16-255)	

9 Digital Timing Reference Sequences (SAV, EAV)

9.1 SAV (start of active video) and EAV (end of active video) digital synchronizing sequences shall define synchronization across the serial digital interface. Figures 2, 3 and 4 show the relationship of the SAV and EAV sequences to analog video and digital video.

9.2 An SAV or EAV sequence shall comprise four consecutive code words: a code word of all ones, a code word of all zeros, another code word of all zeros, and a code word including F (field/frame), V (vertical), H (horizontal), P3, P2, P1, and P0 (parity) bits. An SAV sequence shall be identified by having H = 0; EAV shall have H = 1 (Tables 5 and 6 show details of the coding).

9.3 When digitized, every line shall include a four-sample EAV sequence commencing 88 clocks prior to 0_H (systems 1, 2, 4, 5, 7, and 8 in table 1), 528 clocks prior to 0_H (systems 3, 6 and 9), or 638 clocks prior to 0_H (systems 10 and 11), and a four-sample SAV sequence commencing 188 clocks after 0_H. Digitized lines shall be numbered and the numbering shall change state prior to the horizontal timing point (0_H), as shown in Figure 2. The EAV sequence immediately preceding the 0_H datum of line 1 shall be considered to be the start of the digital frame.

NOTE – At the interface there are variants in the mapping known as "PsF". See Annex A for a description.

9.4 In a progressive system, the EAV and SAV of all lines shall have F = 0;

– The EAV and the SAV of lines 1 through 41 inclusive and lines 1122 through 1125 inclusive shall have V = 1;

– The EAV and SAV of lines 42 through 1121 inclusive shall have V = 0.

9.5 In an interlaced system:

– The EAV sequence of line 1 shall be considered to be the start of the first digital field and the EAV sequence of line 564 shall be considered to be the start of the second digital field;

– The EAV and SAV of lines 1 through 563 inclusive shall have F = 0. The EAV and SAV of lines 564 through 1125 inclusive shall have F = 1;

– The EAV and SAV of lines 1 through 20, lines 561 through 583, and lines 1124 and 1125 shall have V = 1;

– The EAV and the SAV of lines 21 through 560 and lines 584 through 1123 shall have V = 0.

NOTE – A line, which in the analog representation is permitted to convey ancillary signals, may convey digitized ancillary signals.

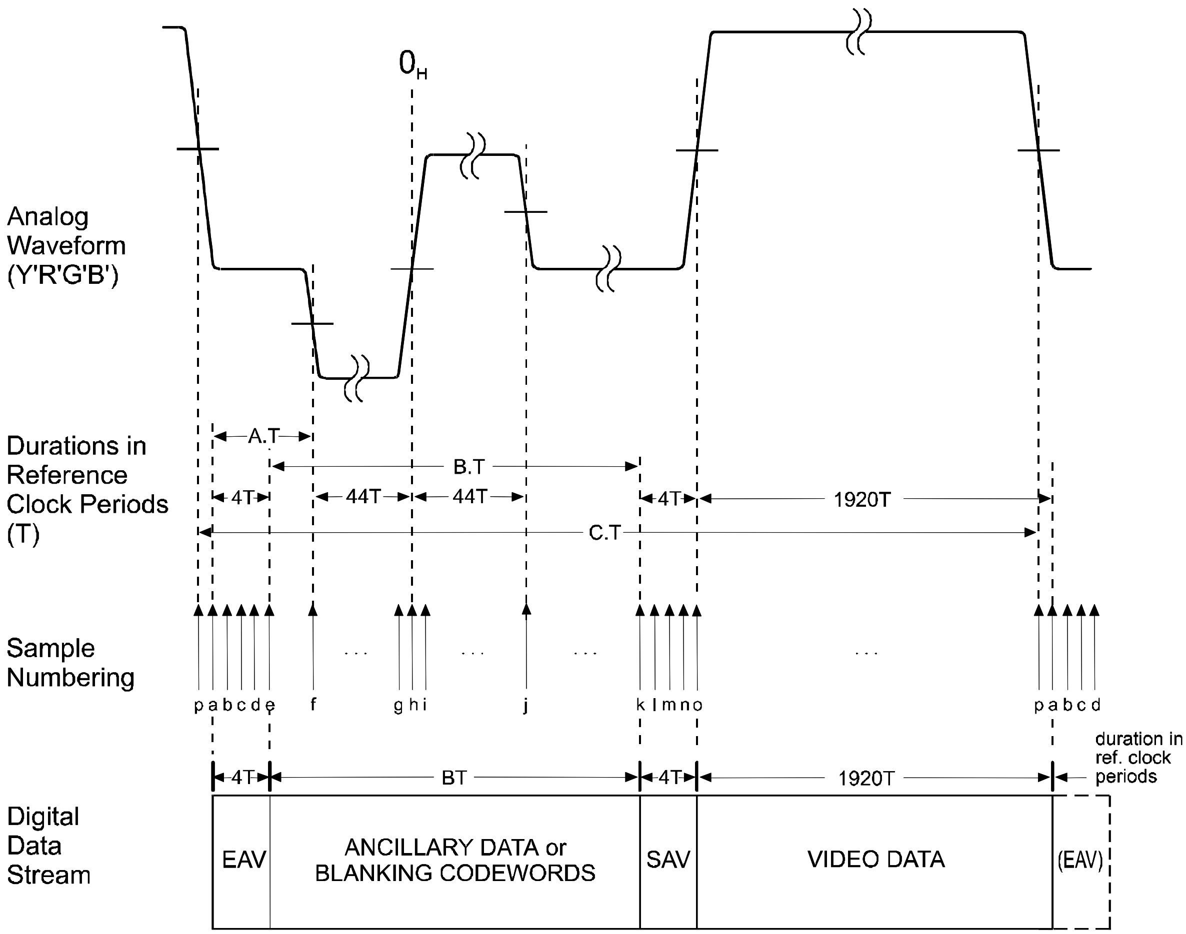


Figure 3 – Analog and digital timing relationship

NOTES

1 Horizontal axis not to scale.

2 0_H is the analog horizontal timing reference point, and in the analog domain is regarded as the start of the line.

3 A line of digital video extends from the first word of EAV through the last word of video data.

4 The number of samples of video data (sample number 'o' through 'p' in Figure 3) is 1920. That is, the letter 'o' denotes sample number 0 and the letter 'p' denotes sample number 1919. Analog 1/2 amplitude duration shall be 1920T –12T/+0T as shown in Table 7.

5 Values a-t, b-t, and c-t are shown in Table 4.

Table 4 – Values for figures 3 and 4 for different Image structure systems

System	Sample numbering															
	a	b	c	d	e	f	g	h	i	j	k	l	m	n	o	p
1,2,4,5,7,8,	1920	1921	1922	1923	1924	1964	2006	2008	2010	2052	2196	2197	2198	2199	0	1919
3, 6, 9	1920	1921	1922	1923	1924	2404	2446	2448	2450	2492	2636	2637	2638	2639	0	1919
10,11	1920	1921	1922	1923	1924	2514	2556	2558	2560	2602	2746	2747	2748	2749	0	1919

System	Durations in reference clock periods (T)		
	A	B	C
1,2,4,5,7,8,	44	272	2200
3,6,9	484	712	2640
10,11	594	822	2750

NOTE – At the interface, there are variants in the mapping known as “PsF”. See Annex A for a description.

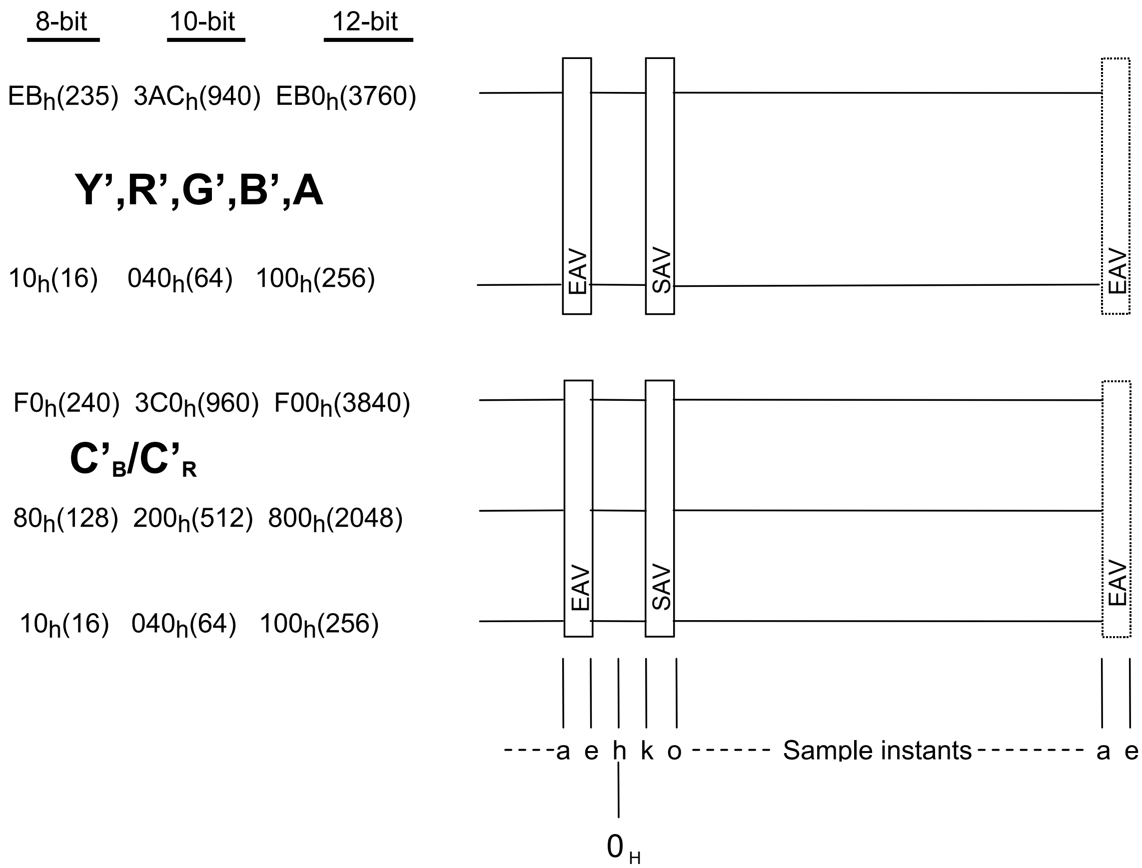


Figure 4 – Digital levels and timing

NOTES

1 Figure 3 and Table 4 show numbering of sample instants for each of the systems covered in this standard.

2 0_H is the analog horizontal timing reference point.

Table 5 – Video timing reference codes

(a) 10-bit system

Bit number		9 (MSB)	8	7	6	5	4	3	2	1	0 (LSB)
Word	Value										
0	$3FF_h$ (1023)	1	1	1	1	1	1	1	1	1	1
1	0	0	0	0	0	0	0	0	0	0	0
2	0	0	0	0	0	0	0	0	0	0	0
3		1	F	V	H	P3	P2	P1	P0	0	0

(b) 12-bit system

Bit number		11 (MSB)	10	9	8	7	6	5	4	3	2	1	0 (LSB)
Word	Value												
0	FFF_h (4095)	1	1	1	1	1	1	1	1	1	1	1	1
1	0	0	0	0	0	0	0	0	0	0	0	0	0
2	0	0	0	0	0	0	0	0	0	0	0	0	0
3		1	F	V	H	P3	P2	P1	P0	0	0	0	0

Table 6 – Protection bits for SAV and EAV

(a) 10-bit system

Bit number	9	8	7	6	5	4	3	2	1	0
Function	1 Fixed	F	V	H	P3	P2	P1	P0	0 Fixed	0 Fixed
0	1	0	0	0	0	0	0	0	0	0
1	1	0	0	1	1	1	0	1	0	0
2	1	0	1	0	1	0	1	1	0	0
3	1	0	1	1	0	1	1	0	0	0
4	1	1	0	0	0	1	1	1	0	0
5	1	1	0	1	1	0	1	0	0	0
6	1	1	1	0	1	1	0	0	0	0
7	1	1	1	1	0	0	0	1	0	0

(b) 12-bit system

Bit number	11	10	9	8	7	6	5	4	3	2	1	0
Function	1 Fixed	F	V	H	P3	P2	P1	P0	0 Fixed	0 Fixed	0 Fixed	0 Fixed
0	1	0	0	0	0	0	0	0	0	0	0	0
1	1	0	0	1	1	1	0	1	0	0	0	0
2	1	0	1	0	1	0	1	1	0	0	0	0
3	1	0	1	1	0	1	1	0	0	0	0	0
4	1	1	0	0	0	1	1	1	0	0	0	0
5	1	1	0	1	1	0	1	0	0	0	0	0
6	1	1	1	0	1	1	0	0	0	0	0	0
7	1	1	1	1	0	0	0	1	0	0	0	0

10 Analog Sync

NOTE – This section, including Table 7, applies to 60-, 59.94- and 50-Hz scanning systems and segmented frame systems (Table 1 systems 1-6, and Table A.1 systems A-E), because direct analog interconnection is not recommended for use with slow-rate systems (30-Hz progressive and below).

10.1 Details of analog sync timing are shown in Figures 1, 3 and 5, and are summarized in Table 7. The parameter ‘h’ not shown in these figures is the duration of the rising edge of horizontal sync pulse.

10.2 A positive zero-crossing of a tri-level sync pulse shall define the 0_H datum for each line. A negative-going transition precedes this instant by 44 reference clock intervals, and another negative-going transition follows this instant by 44 reference clock intervals.

10.3 The positive and negative transition of a tri-level sync pulse shall be skew-symmetric with a rise time from 10% to 90% of 4 ±1.5 reference clock periods. The midpoint of each negative transition shall be coincident with its ideal time within a tolerance of ±3 reference clock periods.

10.4 The tri-level sync pulse shall have structure and timing according to Figures 3 and 5. The positive peak of the tri-level sync pulse shall have a level of +300 mV ± 6 mV; its negative peak shall have a level of -300 mV ± 6 mV. The amplitude difference between positive and negative sync pulses shall be less than 6 mV.

10.5 Each line that includes a vertical sync pulse shall maintain blanking level, here denoted zero, except for the interval(s) occupied by sync pulses. During the horizontal blanking interval, areas not occupied by sync shall be maintained at blanking level, here denoted zero.

10.6 In addition to the tri-level sync pulse that defines 0_H, an interlaced and segmented frame system’s vertical sync line may include a midline tri-level sync pulse whose elements are delayed from 0_H by one-half the line duration. Certain vertical sync lines may therefore contain a broad pulse during the first half line and may contain a broad pulse during the second half line, in the manner described in Sections 10.8 and 10.9, rather than a broad pulse over the whole line as described in Section 10.7. The leading 50% point of a broad pulse shall be 132T after the preceding tri-level zero-crossing; its duration shall be 880T in interlaced or segmented frame systems and 1980T in progressive systems (see Figure 5).

10.7 In a progressive system, a frame shall commence with five vertical sync lines each containing a broad pulse.

10.8 The first field of an interlaced/segmented frame system shall commence with five vertical sync lines (see Figure 1):

– five lines having broad pulses in both the first and second half lines; plus a sixth line having only a midpoint tri-level pulse.

10.9 The second field of an interlaced and segmented frame system shall commence as shown in Figure 1. The vertical sync associated with the second field shall be contained within six lines, comprising:

– the second half of a line having blanking in the first half line, a midline tri-level pulse, and a broad pulse in the second half line;

– four lines having broad pulses in both the first and second half lines and a midline tri-level pulse between them; then

– the first half of one line having a broad pulse in the first half line and a midline tri-level pulse.

11 Analog Interface (Figure 5)

NOTE – This section applies to 60-, 59.94- and 50-Hz scanning systems and segmented frame systems (Table 1 systems 1-6 and Table A.1 systems A-E), because direct analog interconnection is not recommended for use with slow-rate systems (30-Hz progressive and below).

11.1 An analog interface according to this standard may employ either the R'G'B' component set or the Y' $P'_BP'_R$ component set.

11.2 R´G´B´ signals and Y´ signals shall have a nominal bandwidth of 60 MHz for systems 1–3 in Table 1 and 30 MHz for systems 4–11 in Table 1 and systems A-E in Table A.1 as shown in Table 2.

11.3 P'_B and P'_R signals shall have the same bandwidth as that of the associated Y' signal at analog originating equipment. Therefore, the analog interface for P'_B and P'_R signals shall have the same bandwidth as for the Y' signal. P'_B and P'_R signals may have 0.5 the bandwidth of the associated Y' signal for digital equipment.

11.4 Each component signal shall be conveyed electrically as a voltage on an unbalanced coaxial cable into a pure resistive impedance of 75 ohm.

11.5 For the Y' component, reference black (zero) in the expressions of Sections 6 and 7 shall correspond to a level of 0 Vdc, and reference white (unity) shall correspond to 700 mV.

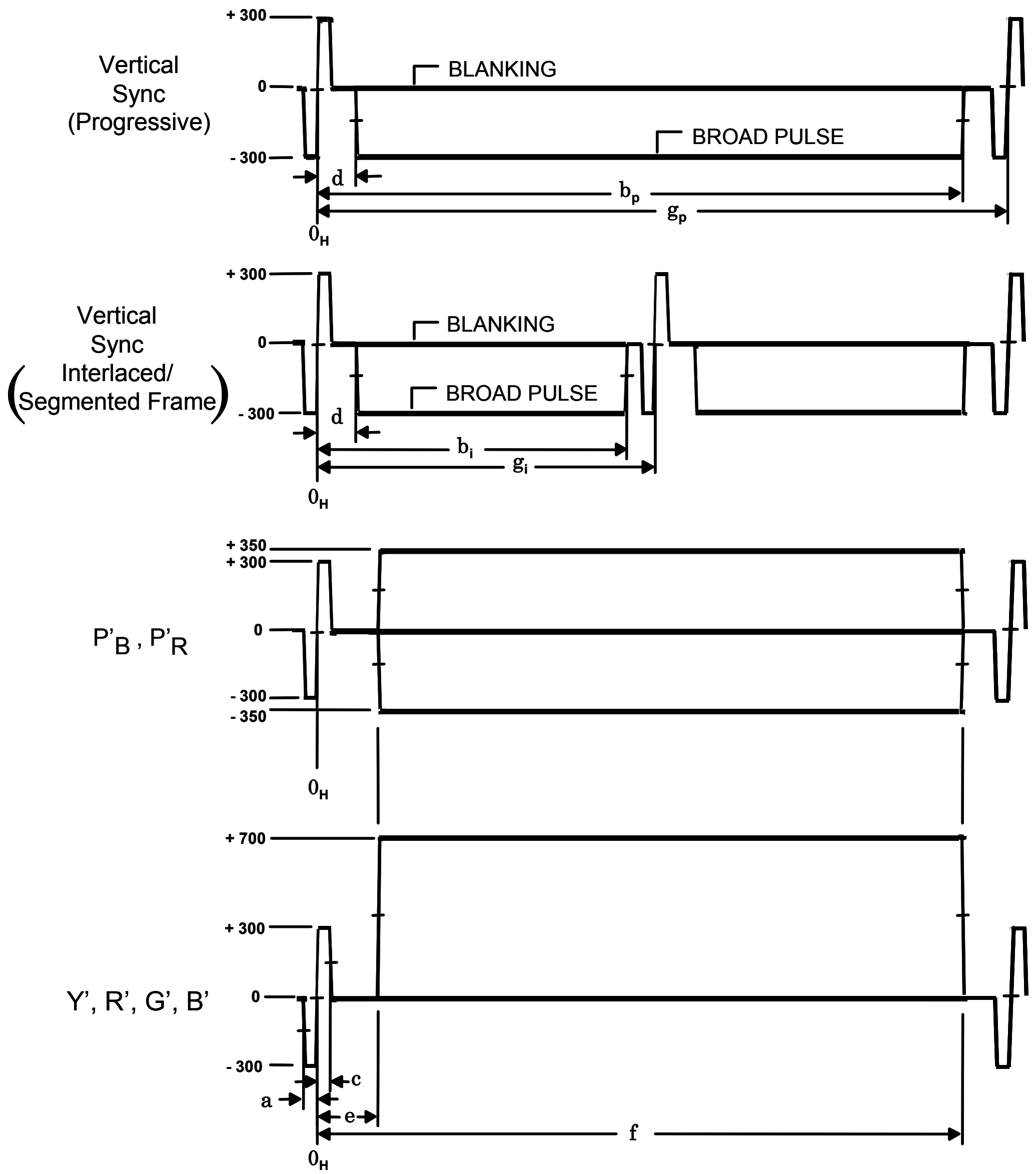
11.6 P'_B and P'_R components are analog versions of the C'_B and C'_R components of Section 6.6, in which zero shall correspond to a level of 0 Vdc and reference peak level (value 0.5 of equations in Section 6.6) shall correspond to a level of +350 mV.

11.7 Tri-level sync according to Section 10 shall be added to each analog component.

11.8 Each of the electrical signals in an analog interface shall employ a connector that conforms either to IEC 61169-8 (2007-2) or to SMPTE RP 160 (three-channel parallel analog interface). In the case of the BNC connector, the impedance of the connector shall be 75 ohm.

Table 7 – Analog sync timing

			Duration (T)			Tolerance (T)
System			1,2,4,5,7, 8, A, B	3,6,9,C	10,11,D, E	
a	See Figure 5		44	44	44	±3
b_i	See Figure 5	(Interlaced/segmented frame)	1012	1012	1012	±3
b_p		(Progressive)	2112	2112	2112	±3
c	See Figure 5		44	44	44	±3
d	See Figure 5		132	132	132	±3
e	See Figure 5		192	192	192	- 0 + 6
f	See Figure 5		2112	2112	2112	- 6 + 0
h	Sync rise time		4	4	4	±1.5
g_i	See Figure 5	(Interlaced/segmented frame)	1100	1320	1375	-
g_p		(Progressive)	2200	2640	2750	-
	Total line		2200	2640	2750	-
	Active line		1920	1920	1920	-12 + 0



NOTES

1 Values for a, b, c, d, e, f and g are given in Table 7.

2 Sync rise time, h, is not shown here.

3 See also Figure 3.

4 Amplitudes are expressed in mV.

Figure 5 – Analog levels and timing

Annex A (Normative) Progressive Segmented Frame System

A.1 A Progressive segmented Frame system (Table A.1) shall scan a frame in the same manner as progressive systems, but shall transmit a frame as if it were interlaced. This provides a means of carrying a progressive picture as two equally divided segments mapped onto an interlaced interface.

A.2 In a Progressive segmented Frame system, the assignment of lines within a frame shall be the same as that of an interlaced system. More specifically, the assignment of each even line of a progressive system shall correspond to lines 1 through 562 of a segmented frame system, and each odd line of a progressive system shall correspond to lines 563 through 1125 of a segmented frame system. The relationship of line N of a progressive system and line M of a segmented frame system shall be in the following equation and as shown in Figure A.1.

$M = N/2$ where $N = 2, 4, 6, \ldots 1124$
$M = (N+1125)/2$ where $N = 1, 3, 5, \ldots 1125$

Table A.1 – Interface ordering

No.	Interface nomenclature	Table 1 system number
A	1920 x 1080/30/PsF	7
B	1920 x 1080/29.97/PsF	8
C	1920 x 1080/25/PsF	9
D	1920 x 1080/24/PsF	10
E	1920 x 1080/23.98/PsF	11

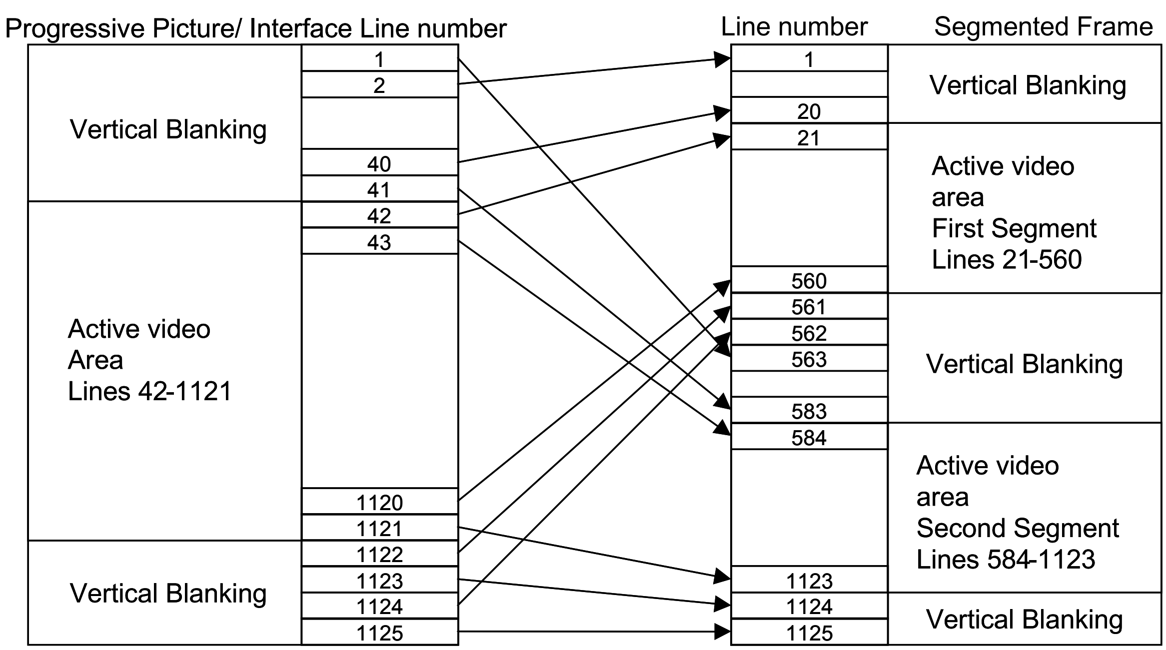


Figure A.1 – Progressive segmented Frame system

Annex B (Normative)
Ancillary Data

B.1 Ancillary data may optionally be included in the blanking intervals of a digital interface according to this standard.

B.2 The interval between the end of EAV and the start of SAV may be employed to convey ancillary data packets. Designers should be aware that when SMPTE 292 serial interface is employed, the first four samples after EAV are reserved for other usage.

B.3 The interval between the end of SAV and the start of EAV of any line that is outside the vertical extent of the picture (as defined in Sections 7.2 and 7.3), and that is not employed to convey digitized ancillary signals, may be employed to convey ancillary data packets.

INFORMATIVE NOTE – The reader is cautioned to be aware that ancillary data should be placed taking into account of the switching point as defined by SMPTE RP 168.

B.4 Ancillary data packets may be conveyed across each of the R', G', B' and A channels, across each of the Y', C'_B, C'_R and A channels or across each of the Y', C'_B/C'_R and A channels.

B.5 In the case of 12-bit representation, the ancillary data is defined by the most significant 10 bits of the 12-bit data and the least significant 2 bits are defined to be zero.

B.6 In the case of 10-bit representation, intervals not used to convey SAV, video data, EAV, ancillary signals or ancillary data shall convey the code word 40_h(64) (black) in the R', G', B', Y' channels, or 200_h(512) in the C'_B/C'_R channels. They shall be 10_h(16) and 80_h(128) respectively in the case of 8-bit representation and 100_h(256) in the R', G', B', Y' channels, or 800_h(2048) in the C'_B, C'_R, C'_B/C'_R channels respectively in the case of 12-bit representation.

B.7 For specifications of the details of ancillary data, see SMPTE 291M.

Annex C (Informative)
Bit-Parallel Interface (for 8-Bit and 10-Bit Systems)

System designers are advised that the inclusion of this interface definition is to cover some legacy equipment. This interface is not in common use and should not be implemented in new designs. Future revisions of SMPTE 274M may not contain information about this interface.

C.1 Electrical interface

C.1.1 This clause describes a bit-parallel electrical interface which is applicable to all the image structure systems specified in this standard. It is a point-to-point interface with one transmitter and one receiver.

C.1.2 Video data shall be transmitted in NRZ form in real time (unbuffered) in blocks, each comprising one active line.

C.1.3 A pair of conductors conveys a clock signal at the sampling rate of Y'(or R', G', B').

C.1.4 Data shall be transmitted in parallel by means of eight or ten shielded conductor pairs for each of the channels.

C.1.5 The signals on the interface shall be transmitted without equalization in systems 4–11 in Table 1 for a distance of up to 20 m (65.6 ft), and in systems 1–3 in Table 1 for a distance of up to 14 m (46.3 ft).

C.1.6 The data bits of each component shall be numbered nine through zero, where zero is the least significant bit.

C.1.7 The R'G'B' interface shall use three sets of the same number of either eight or ten pairs to convey R', G' and B' components on the contacts shown in Table C.1.

C.1.8 The $Y'C'_BC'_R$ interface uses a set of eight or ten pairs to convey the Y' signal (on the pins indicated for the G signals in table C.1), and a second set of the same number of pairs to convey time-multiplexed C'_B and C'_R signals (on the pins indicated for R' in Table C.1).

C.1.9 The $Y'C'_BC'_RA$ interface conveys eight or ten bits of $Y'C'_BC'_R$ as above, and conveys an auxiliary signal A of the same number of bits (on the pins indicated for B' in Table C.1).

Table C.1 – 93-contact connector contact assignment

	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
	1	CK+	17	GND	33	CK-						
MSB	2	G9+	18	GND	34	G9-	49	B4+	64	GND	79	B4-
	3	G8+	19	GND	35	G8-	50	B3+	65	GND	80	B3-
	4	G7+	20	GND	36	G7-	51	B2+	66	GND	81	B2-
	5	G6+	21	GND	37	G6-	52	B1+	67	GND	82	B1-
	6	G5+	22	GND	38	G5-	53	B0+	68	GND	83	B0-
	7	G4+	23	GND	39	G4-	54	R9+	69	GND	84	R9-
	8	G3+	24	GND	40	G3-	55	R8+	70	GND	85	R8-
LSB8	9	G2+	25	GND	41	G2-	56	R7+	71	GND	86	R7-
	10	G1+	26	GND	42	G1-	57	R6+	72	GND	87	R6-
LSB10	11	G0+	27	GND	43	G0-	58	R5+	73	GND	88	R5-
	12	B9+	28	GND	44	B9-	59	R4+	74	GND	89	R4-
	13	B8+	29	GND	45	B8-	60	R3+	75	GND	90	R3-
	14	B7+	30	GND	46	B7-	61	R2+	76	GND	91	R2-
	15	B6+	31	GND	47	B6-	62	R1+	77	GND	92	R1-
	16	B5+	32	GND	48	B5-	63	R0+	78	GND	93	R0-

C.2 Electrical characteristics

C.2.1 The arrangement of the transmitter and receiver devices and conductors for one balanced conductor pair shall be as shown in Figure C.1.

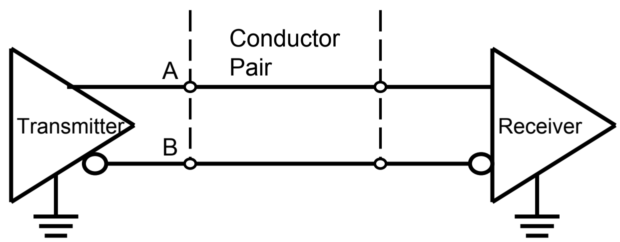


Figure C.1 – Transmitter and receiver connection

NOTE – The transmitter and receiver parameters are ECL-compatible so as to permit, in systems 4-11 in Table 1, the use of standard ECL (10KH series) devices.

C.2.2 The signaling polarity of voltage appearing across the interface shall be positive binary, defined as follows:

– The A terminal of the line driver shall be negative with respect to the B terminal for a binary 0 state;

– The A terminal of the line driver shall be positive with respect to the B terminal for a binary 1 state.

C.2.3 The transmitter in an 8-bit system shall assert bits 1 and 0 to logic zero.

C.2.4 The receiver in an 8-bit system shall terminate bit pairs 1 and 0.

C.2.5 The transmitter shall have a balanced output with a maximum impedance of 110 ohm.

C.2.6 The average of the voltages on the two terminals of the line driver with reference to the ground terminal shall be - 1.29 V ±15%.

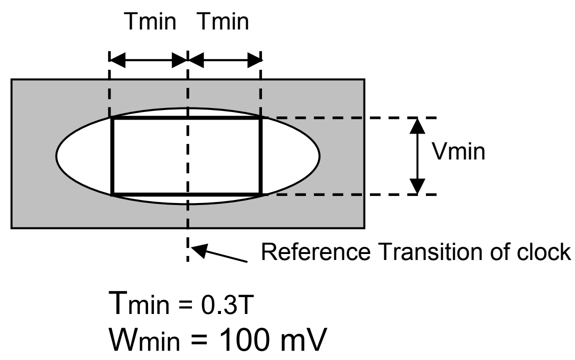
C.2.7 The generated signal shall lie between 0.6 V peak-to-peak and 2.0 V peak-to-peak, measured across a 110 ohm resistor connected to the output terminals without any transmission line.

C.2.8 Rise and fall times shall be no greater than 0.15T when measured between the 20% and the 80% amplitude points across a 110 ohm resistive load. The difference between rise and fall times shall not exceed 0.075T.

C.2.9 The receiver shall present an impedance of 110 ohm ± 10 ohm.

C.2.10 Maximum input signal amplitude shall be 2.0 V peak-to-peak.

C.2.11 The receiver shall require a differential input voltage of no more than 185 mV peak to peak to correctly attain the intended binary state. Additionally, the line receiver must sense correctly the binary data when a random data signal produces, at the data detection point, the conditions represented by the eye diagram shown in Figure C.2.



NOTE – Cable response losses, frequency response characteristics of the interface electronics, propagation delay skew, data source timing skew and clock jitter all affect reliable detection of received data and must be taken into account in system timing margin considerations. This figure assumes propagation skew of 0.18T, data source skew of 0.075T, and clock jitter of 0.04T to show the minimum eye opening of 2 x Tmin, due only to frequency characteristics of the cable and interface electronics. In this case, the total system timing margin goes to zero.

Figure C.2 – Idealized eye diagram corresponding to the minimum input signal level

C.2.12 The receiver shall operate correctly in the presence of common mode noise (comprising interference in the range 0 to line frequency, f_H, with both terminals to ground) having a maximum amplitude of 0.3 V.

C.2.13 Data shall be correctly sensed when the relative differential delay between the received clock and the received data is less than 0.3T.

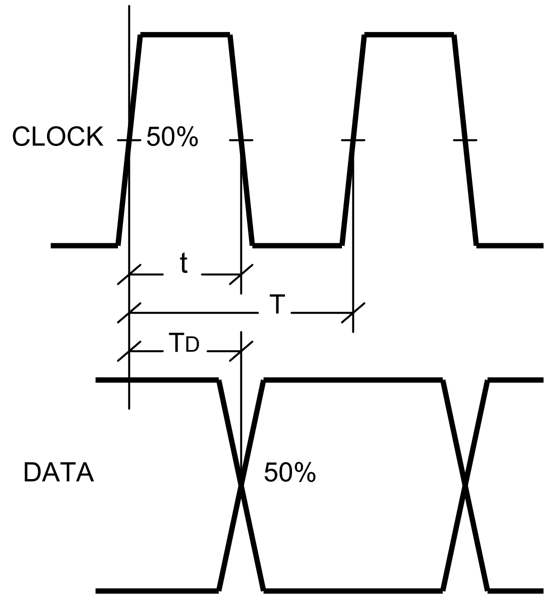
C.3 Clock

C.3.1 One pair on the interface shall convey a clock signal at the sampling frequency, which shall have a positive pulse width of (0.5 ± 0.11) T.

C.3.2 Peak-to-peak jitter between rising edges of the transmitted clock shall be less than 0.08T, measured over a period of one frame.

C.3.3 Data signals shall be asserted by the transmitter at a time interval (0.5 ± 0.075) T, denoted TD, following the 0-to-1 transition of the clock, according to Figure C.3.

C.3.4 Data signals shall be sampled at the receiver by the 0-to-1 transition of the clock.



Clock period, $T = 1/(C \times f_H)$

Clock pulse width, $t = (0.5 \pm 0.11)\ T$

Data timing (sending end), $T_D = (0.5 \pm 0.075)\ T$

(where C equals number of reference clock periods per horizontal scan line; for values of C for the various scanning systems, refer to Table 4)

Figure C.3 – Clock-to data timing (at sending end)

C.4 Mechanical interface

C.4.1 The multichannel cable shall consist of twisted-pair conductors with individual shields. The nominal characteristic impedance of each twisted pair shall be 110 ohm.

C.4.2 This standard applies to applications where the physical length of the cable is at most 20m for systems 4-11 in Table 1, and 14m for systems 1-3 in Table 1. Within this range, equalization of the cable characteristics is not required.

C.4.3 The multichannel cable shall consist of either 21 or 31 twisted pairs of conductors with individual shielding of each pair. The cable should be constructed to minimize the differential delay between any two conductor pairs. Cable with controlled differential delay may be appropriate for transmission distances longer than that specified in Section C.4.2.

C.4.4 The cable shall contain an overall shield to minimize electromagnetic interference (EMI) carried through the cable assembly and connectors via the cable shield and the connector bodies.

C.4.5 An interface according to this standard shall employ a 93-pin connector. Figures C.4, C.5, and C.6 show the mechanical drawings and dimensions of the pin connector (cable plug), the socket connector (equipment receptacle), and the connector metal hood and retaining mechanism, respectively. The cable assembly shall provide pin contacts at both ends. Transmitter and receiver equipment shall have connectors with socket contacts. The connector hood shall be designed to prevent radiation of electromagnetic interference.

C.4.6 Connector contact assignment shall be according to Table C.1. The shield for each conductor pair shall use the ground pin located between pins for the signal pair as shown in Table C.1.

C.4.7 The overall shield of the multichannel cable shall be electrically connected to the connector hood. The connector hood, in turn, shall be grounded to the frame of the equipment. The shield wire of each twisted pair shall be grounded to the system ground of the equipment through a pin contact. There shall be electrical conduction between the overall cable shield and the connector hood and equipment frame.

C.4.8 The cable connectors shall be provided with two M4 mounting screws and the equipment connectors shall be provided with two M4 female threaded bosses.

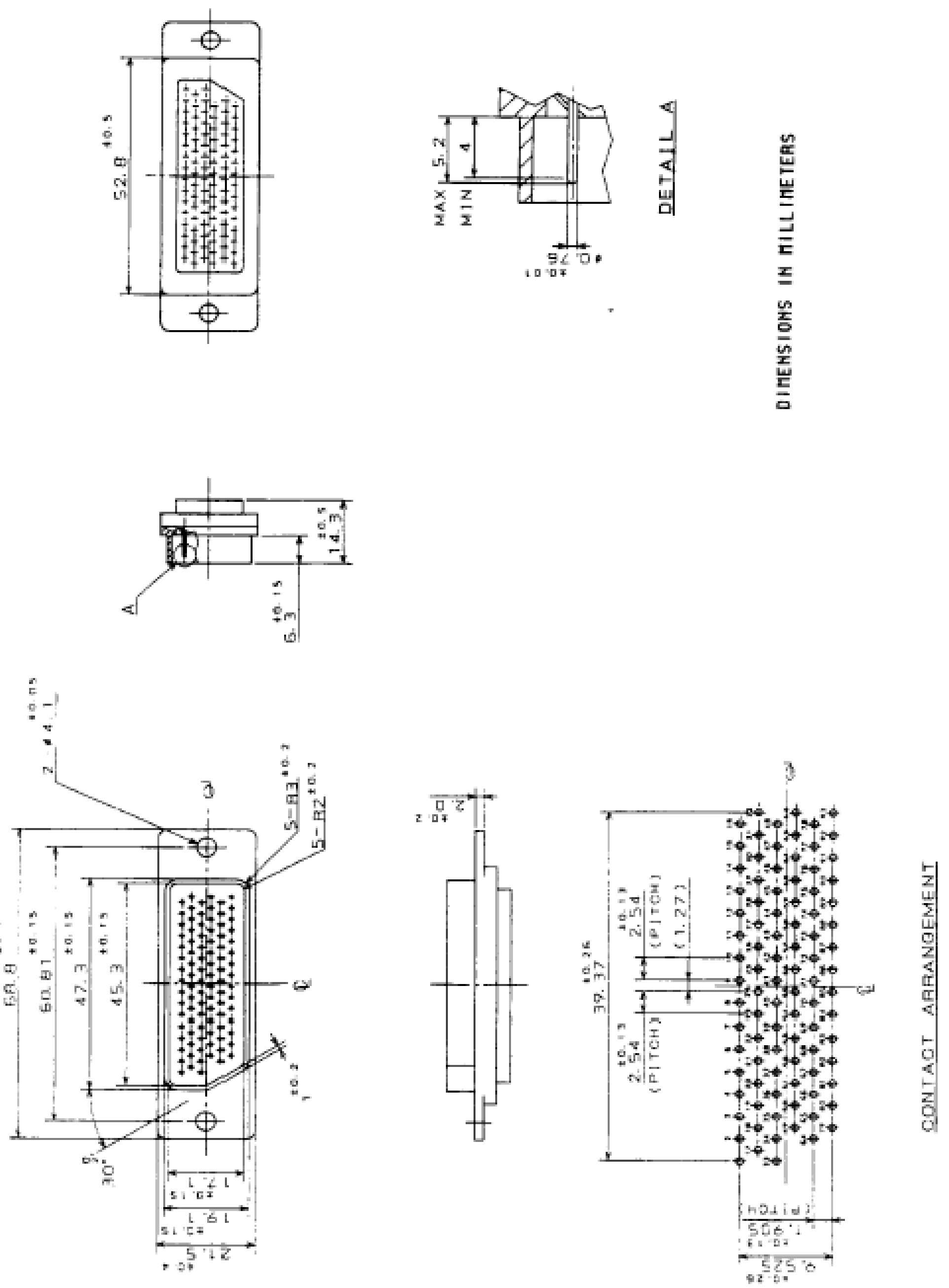


Figure C.4 – 93-contact plug connector (cable)

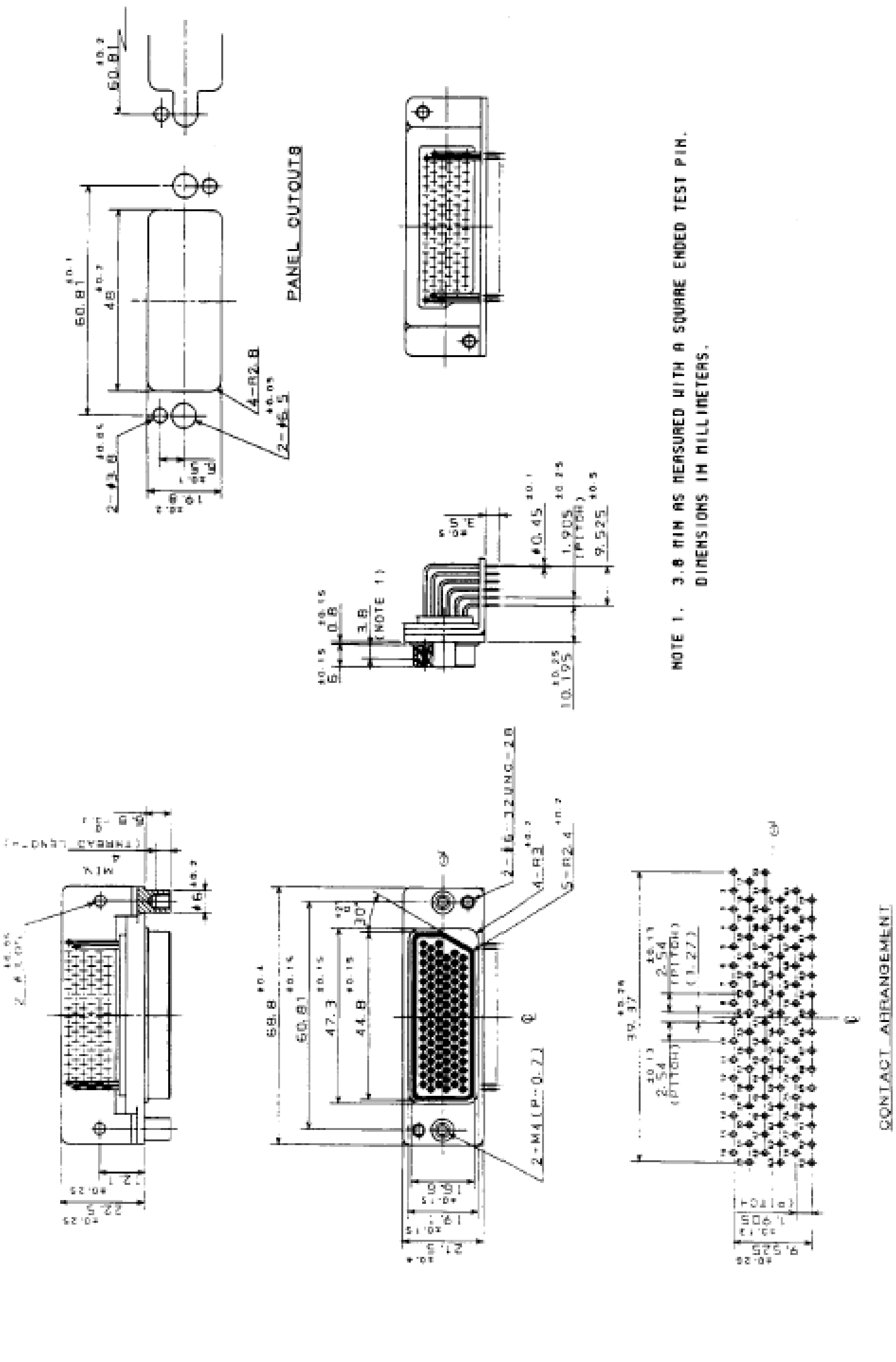


Figure C.5 – 93-contact socket connector (equipment)

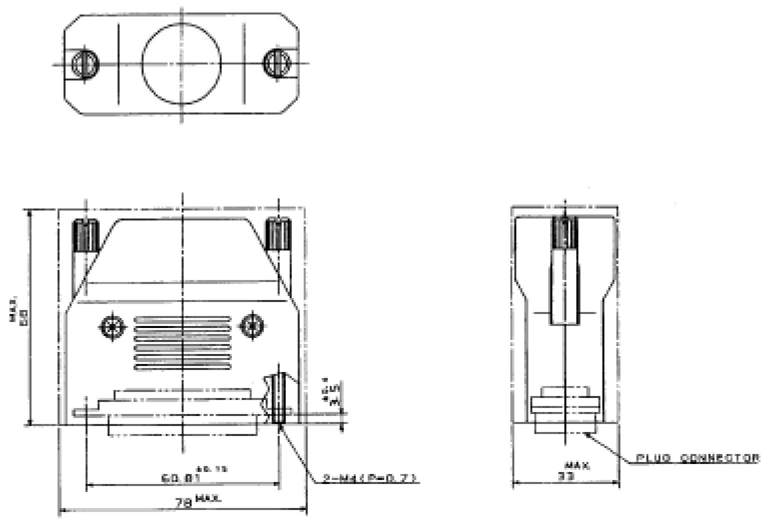


Figure C.6 – 93-contact plug (hood)

Annex D (Informative)
Pre- and Post-Filtering Characteristics

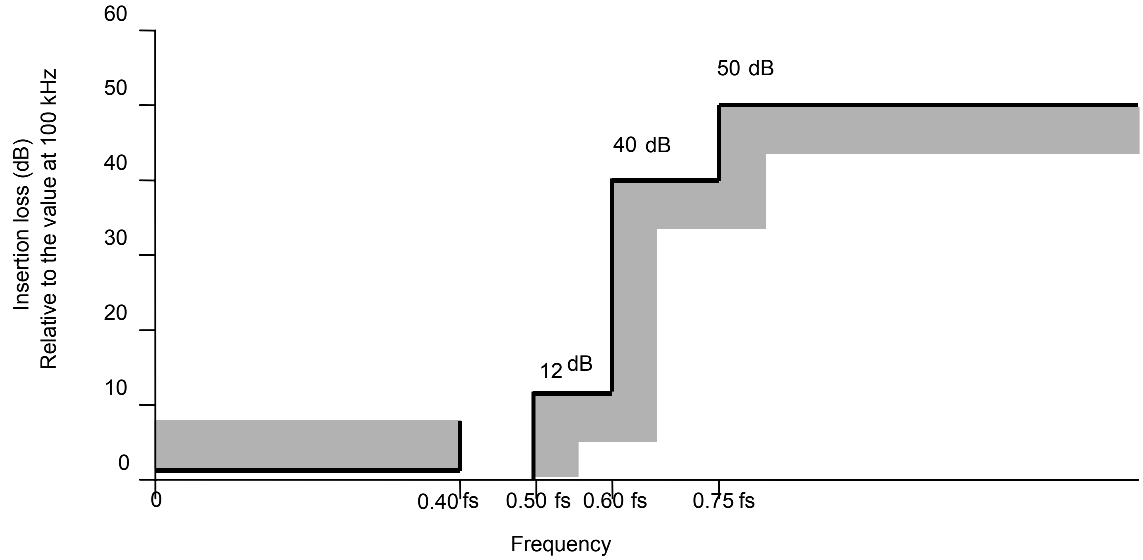
D.1 Figure D.1 depicts example filter characteristics for pre- and post-filtering of Y' R' G' B' P'_B and P'_R component signals in 4:4:4 systems. Figure D.2 depicts example filter characteristics for pre- and post-filtering of $P_{'B}$ and P'_R component signals in 4:2:2 systems.

D.2 The pass band frequency of the component Y´, R´, G´, and B´ signals is nominally 60 MHz for systems 1, 2 and 3, and 30 MHz for systems 4 through 11 in Table 1.

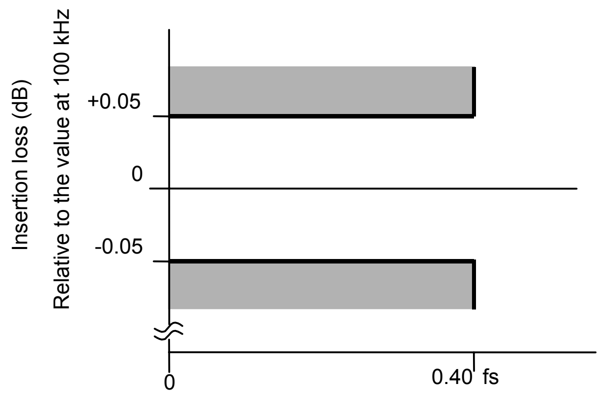
D.3 The value of the amplitude ripple tolerance in the pass band is ± 0.05 dB relative to the insertion loss at 100 kHz.

D.4 The insertion loss characteristics of the filters are frequency-scaled from the characteristics of ITU-R BT.601. Insertion loss is 12 dB or more at half the sampling frequency of the Y' R' G' and B' components, and 6 dB or more at half the sampling frequency of the P'_B and P'_R components, relative to the insertion loss at 100 kHz.

D.5 The specifications for group-delay in the filters are sufficiently tight to produce good performance while allowing the practical implementation of the filters.

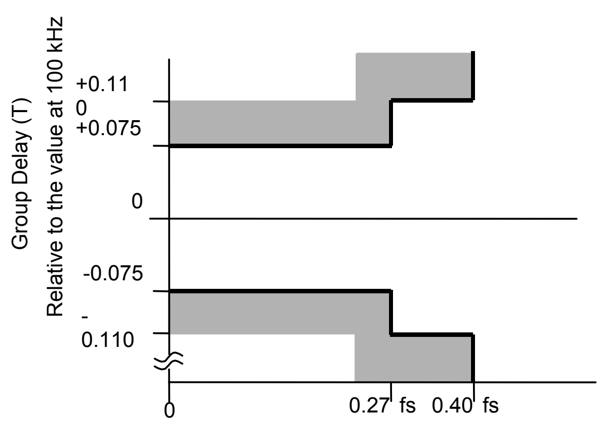


Template for insertion loss



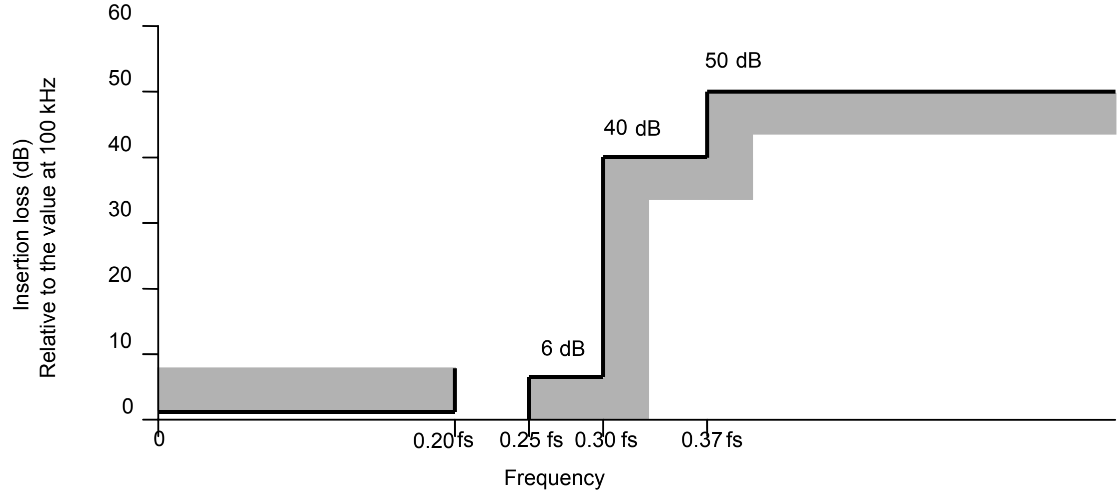
NOTE - The value fs is given in table 1

Template for passband ripple

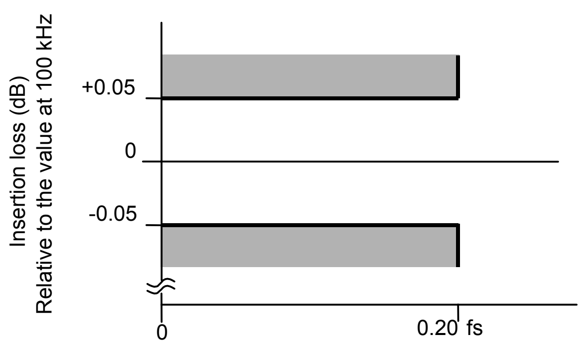


Template for passband group-delay

Figure D.1 – Example filter template for Y’ R’ G’ B’

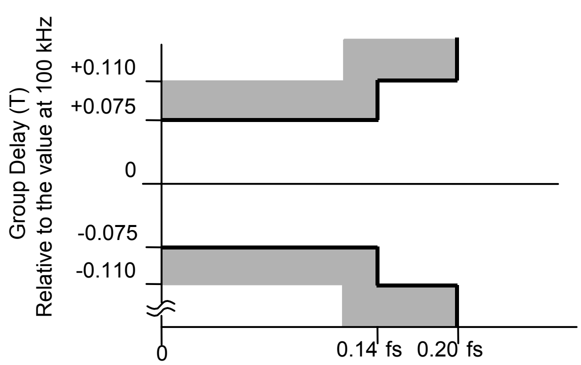


Template for insertion loss



Template for passband ripple

NOTE - The value of fs is given in table 1



Template for passband group-delay

Figure D.2 – Example filter template for P'_B and P'_R components

Annex E (Informative)
Production Aperture

E.1 Production aperture

A production aperture for the studio digital signal defines an active picture area of 1920 pixels by 1080 lines produced by signal sources such as cameras, telecines, digital video tape recorders, and computer-generated pictures conforming to this standard.

E.2 Analog blanking tolerance

E.2.1 The duration of the maximum active analog video signal measured at the 50% points is standardized as 1920 clock periods. However, the analog blanking period may differ from equipment to equipment and the digital blanking may not coincide with the analog blanking in actual implementation.

E.2.2 To maximize the active video duration in picture origination sources, it is desirable to have analog blanking match digital blanking. However, recognizing the need for reasonable tolerance in implementation, analog blanking may be wider than digital blanking (see Figure 3).

E.2.3 To accommodate a practical implementation of analog blanking within various studio equipments, a tolerance of six clock periods is provided at the start and end of active video. Accordingly, the analog tolerances to parameters e and f of Table 7 are as follows:

Parameter	Definition	Nominal value (ref. clocks)	Tolerance (ref. clocks)
e	0_H to start of active video	192	- 0 + 6
f	0_H to end of active video	2112	- 6 + 0

Preferred practice is to provide a full production aperture signal at the output of an analog source prior to first digitization, reserving the tolerance for possible subsequent analog processes.

E.2.4 The relationship of the associated analog representation (inclusive of this tolerance) with the production aperture is shown in Figure 3.

E.3 Transient regions

E.3.1 This standard defines a picture aspect ratio of 16:9 with 1920 pixels per active line and 1080 active lines. However, digital processing and associated spatial filtering can produce various forms of transient effects at picture blanking edges and within adjacent active video that should be taken into account to allow practical implementation of the studio standard.

E.3.2 The following factors contribute to these effects:

– Bandwidth limitation of component analog signals (most noticeably, the ringing on color-difference signals);

– Analog filter implementation;

– Amplitude clipping of analog signals due to the finite dynamic range imposed by the quantization process;

– Use of digital blanking in repeated analog-digital-analog conversions; and

– Tolerance in analog blanking.

E.4 Clean aperture

E.4.1 The bandwidth limitation of an analog signal (pre- and post-filtering) can introduce transient ringing effects which intrude into the active picture area. Also, multiple digital blanking operations in an analog-digital-analog environment can increase transient ringing effects. Furthermore, cascaded spatial filtering and/or techniques for handling the horizontal and vertical edges of the picture (associated with complex digital processing in post-production) can introduce transient disturbances at the picture boundaries, both horizontally and vertically. It is not possible to impose any bounds on the number of cascaded digital processes which might be encountered in the practical post-production system. Hence, recognizing the reality of those picture edge transient effects, the definition of a system design guideline is introduced in the form of a subjectively artifact-free area, called clean aperture.

E.4.2 The clean aperture defines an area within which picture information is subjectively uncontaminated by all edge transient distortions. The clean aperture should be as wide as is needed to accommodate cascaded digital manipulations of the picture. Computer simulations have shown that a transient effect area defined by 16 samples on each side and 9 lines at both top and bottom within the digital production aperture, would represent an acceptable (and practical) worst-case level of protection in allowing two-dimensional transient ringing to settle below a subjectively acceptable level.

E.4.3 This gives rise to a clean aperture of 1888 horizontal active pixels by 1062 active lines whose quality is guaranteed for final release. The clean aperture lies within the production aperture as shown in Figure E.1.

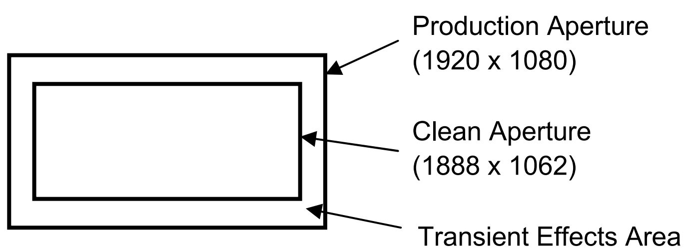


Figure E.1 – Clean aperture

Annex F (Informative)
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Revision Notes

This version incorporates Amendment #1 to SMPTE 274M approved January 29, 2008. The purpose of this revision is to update the normative reference to the physical 75-ohm connector. There are no physical changes to the connector, just the IEC reference number. The changes are summarized below.

1. "Section 2, Conformance Notation" has been added and all sections following have been renumbered (including all references to sections within the document).

2. Under Normative References in Section 3 (previously Section 2), the CIE publication and the IEC document have been updated.

3. Section 11.8 (previously 10.8) has been revised.