



2014-07-14

Withdrawal of SMPTE ST 267M-1995

For Television — Bit-Parallel Digital Interface — Component Video Signal 4:2:2 16×9 Aspect Ratio

This Standard has been withdrawn and its content is no longer endorsed by the Society. This action has been taken because it is judged that there is a significant possibility that use of the document may cause harm.

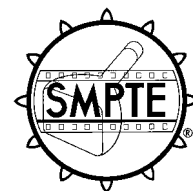
The content of SMPTE ST 267M 'For Television — Bit-Parallel Digital Interface — Component Video Signal 4:2:2 16×9 Aspect Ratio' has been folded into SMPTE ST 125 'SDTV Component Video Signal Coding 4:4:4 and 4:2:2, for 13.5 MHz and 18 MHz Systems' including updated information and some corrections.

To avoid confusion, especially as to the number of active lines, SMPTE ST 267M has been withdrawn.

The following statement has been added at the beginning of the Scope of this withdrawn document:

"This Standard has been withdrawn. The information contained in it, with updates, has been incorporated into SMPTE ST 125:2013."

for Television — Bit-Parallel Digital Interface — Component Video Signal 4:2:2 16×9 Aspect Ratio



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1 Scope

This standard defines an interface for system M (525/59.94) wide screen, 16×9 aspect ratio, digital television equipment based on ITU-R 601-3. Two luminance sampling rates are provided, 13.5-MHz sampling providing full-signal compatibility with equipment operating in compliance with ANSI/SMPTE 125M, and 18-MHz sampling providing equivalent horizontal resolution for the 16×9 aspect ratio of this standard as compared to the 4×3 aspect ratio of ANSI/SMPTE 125M. Use of the 18-MHz sampling method also provides 16×9 to the 4×3 aspect ratio translation by sample selection rather than sample interpolation as would be required with 13.5-MHz sampling. The standard has application in the television studio over distances up to 300 m (1000 ft) for 13.5-MHz sampling and 225 m (750 ft) for 18-MHz sampling.

2 Interface characteristics

2.1 The video signal is transmitted in the form of one luminance (Y) and two color-difference components (scaled version of R-Y and B-Y).

2.2 The video signal is transmitted at the 4:2:2 family level of ITU-R 601-3, with a nominal luminance sampling frequency of 13.5 MHz or 18 MHz. Provision is made to convey signals at 10-bit precision. Because of the potential use of 8-bit data, all synchronizing signals (EAV, SAV, ANC) must be detected by reference to the eight most significant bits only.

2.3 The bits of the digital code words that describe the video signal are transmitted in a parallel arrangement using 10 conductor pairs as described in 6.2.2. Each pair carries a multiplexed stream of bits (of the same significance) of each of the component signals. Accordingly, the bit rate used in each pair is nominally 27 Mbits/s for 13.5-MHz sampling and 36 Mbits/s for 18-MHz sampling. An eleventh conductor pair carries a clock signal at 27 MHz or 36 MHz, respectively.

2.4 The signals on the interface are transmitted using balanced conductor pairs for a distance up to 50 m (160 ft) for 13.5-MHz sampling and 40 m (120 ft) for 18-MHz sampling without equalization, and up to 300 m (1000 ft) for 13.5-MHz sampling and 225 m (750 ft) for 18-MHz sampling with appropriate equalization.

2.5 The interface consists of one transmitter and one receiver in a point-to-point connection.

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2.6 Parameters of the signal format are chosen to facilitate conversion to and from a serial digital interface format. The serial digital interface defined in ANSI/SMPTE 259M is the preferred method for the interconnection of digital equipment when cable lengths exceed 50 m.

2.7 The interface allows the transmission of appropriate ancillary signals that may be multiplexed into the data stream during video blanking intervals.

2.8 Where hexadecimal values are used, they are indicated by a subscript h, such as 3FF_h; other values are decimal.

3 General

3.1 Signal convention

The signaling sense of the voltage appearing across the interconnection cable is positive binary and defined as follows (refer to figure 1):

3.1.1 The A terminal of the transmitter shall be negative with respect to the B terminal for a binary 0 (LOW or L or OFF) state.

3.1.2 The A terminal of the transmitter shall be positive with respect to the B terminal for a binary 1 (HIGH or H or ON) state.

3.2 Signal names

The data lines are designated DATA 0 through DATA 9. The group of 10 signals is identified by placing parentheses around the range of subscripts included, as DATA (0-9). When 8-bit signals are conveyed by the interface, DATA (2-9) shall be used and DATA (0-1) shall be set to zero. DATA 9 is always the most significant bit.

3.3 Component coding considerations

Spectral characteristics of analog signals to be encoded must be restricted to eliminate aliasing. Filters, as described in ITU-R 601-2, annex III, may be considered for use with 13.5-MHz sampling and can be scaled for 18-MHz sampling. Designers are cautioned to use filter characteristics that are best suited for their particular product application.

3.4 Sin x/x considerations

The characteristics of the data word at the interface are based on the assumption that the location of any required sin x/x correction is at the point where the digital signal is converted to an analog format.

3.5 Blanking interval considerations

This standard does not require the device feeding the interface to transmit video data during the entire blanking interval. Therefore, ancillary information may be inserted into the horizontal blanking interval by the user within the constraints specified in 4.4 and 4.5.

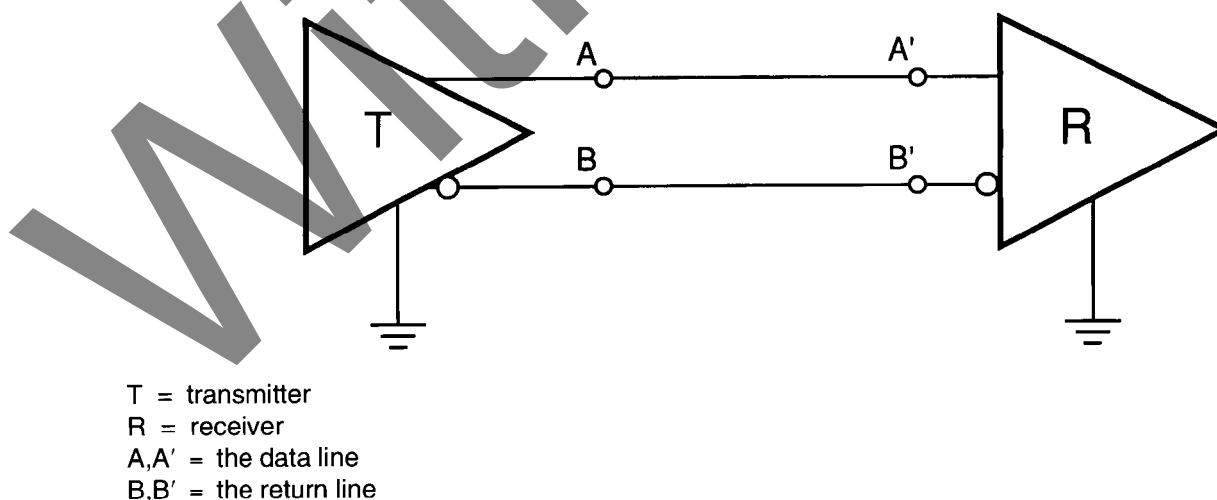


Figure 1 – Positive binary signal convention

The vertical blanking duration is a minimum of nine lines. Ancillary information may be inserted into this nine-line interval by the user within the constraints specified in 4.4 and 4.5.

3.6 Signal specifications

All digital signal time intervals are specified at the half-amplitude points. All transitions are specified between the 20% and 80% amplitude points.

3.7 Electromagnetic interference considerations

Digital apparatus can radiate a significant amount of energy at harmonics of the clock frequency. In the case of 13.5-MHz sampling, clock harmonics lie at 121.5 MHz and 243 MHz, both of which are aeronautical distress frequencies. Equipment and system designers must, therefore, pay particular attention to the provision of adequate shielding.

3.8 Document of compliance

It is suggested that any documentation indicating compliance with this standard be written in such a manner that use of 13.5-MHz and/or 18-MHz sampling is clearly defined. This can be accomplished with a suffix to the numerical designation such as ANSI/SMPTE 267M-13.5 or ANSI/SMPTE 267M-18.

4 Interface format

4.1 General description

The interface consists of a unidirectional, 11-pair interconnection between a transmitting equipment and a receiving equipment. Video data, timing reference information, and ancillary signals are time multiplexed and transferred on 10 data pairs in NRZ form. An eleventh pair provides a synchronous clock.

4.2 Encoding parameters

Table 1 summarizes the encoding parameter values.

4.3 Interface characteristics

Table 2 specifies the interface characteristics.

4.4 Digital blanking relationship

4.4.1 Horizontal sync relationship — 13.5-MHz sampling

Figure 2a shows the relationship between video signals in the digital and analog domains for 525-line systems. Figure 2b shows the multiplex structure.

Transmitted during each active line are 1440 multiplexed luminance and chrominance values (720 luminance, 360 chrominance C_R , and 360 chrominance C_B values).

Eight of the remaining 276 interface clock intervals are used to transmit synchronizing information; the other 268 interface clock intervals may be used to carry ancillary information.

The first of these 1716 interface clock intervals is designated line word 0 for the purpose of reference only. The 1716 sample words per total line are therefore numbered 0 through 1715. Intervals 0 through 1439, inclusive, contain video data. The interface clock intervals occurring during digital blanking are designated 1440 through 1715.

Intervals 1440 through 1443 are reserved for the end-of-active-video (EAV) timing reference described in 4.5.3. Intervals 1712 through 1715 are reserved for the start-of-active-video (SAV) timing reference described in 4.5.3.

The half-amplitude point of the leading (falling) edge of the analog horizontal sync signal shall be coincident with a sample point which would be conveyed by word 1473 if carried across the interface.

4.4.2 Horizontal sync relationship — 18-MHz sampling

Figure 2c shows the relationship between video signals in the digital and analog domains for 525-line systems. Figure 2d shows the multiplex structure.

Transmitted during each active line are 1920 multiplexed luminance and chrominance values (960 luminance, 480 chrominance C_R , and 480 chrominance C_B values).

Eight of the remaining 368 interface clock intervals are used to transmit synchronizing information; the other 360 interface clock intervals may be used to carry ancillary information.

Table 1 – Encoding parameters

Coded signals: These values are obtained from the gamma precorrected signals	$Y = 0.299R + 0.587G + 0.114B$ $C_R = 0.713 (R-Y) = 0.500R - 0.419G - 0.081B$ $C_B = 0.564 (B-Y) = 0.500B - 0.169R - 0.331G$			
Number of samples per line: -- luminance (Y) -- each color-difference signal (C_R , C_B) -- total number of samples	13.5-MHz sampling Total Active		18-MHz sampling Total Active	
	858	720	1144	960
	429	360	572	480
	1716	1440	2288	1920
Sampling structure:	Orthogonal: line, field, and frame repetitive; C_R and C_B samples are cosited with odd (1st, 3rd, 5th) samples in each line			
Sampling frequency: -- luminance (Y) -- each color-difference signal (C_R , C_B)	<u>13.5-MHz sampling</u> 13.5-MHz nominal 6.75-MHz nominal		<u>18-MHz sampling</u> 18-MHz nominal 9-MHz nominal	
Form of encoding:	Uniformly quantized, PCM, 10 bits per sample, for the luminance and each color-difference signal.			
Correspondence between video signal levels and quantization levels: -- luminance (Y) -- each color-difference signal (C_B , C_R)	877 quantization levels with the black level corresponding to level 64 and the peak white level corresponding to level 940. 897 quantization levels symmetrically distributed about level 512, corresponding to the zero signal.			

Table 2 – Interface characteristics

Digital format	Parallel: 11 balanced signal pairs carrying clock and 10 data bits
Interface clock, 13.5-MHz sampling	27.0 MHz nominal
Interface clock, 18-MHz sampling	36.0 MHz nominal
Voltage levels	Standard ECL (10K or 10KH series)
Driver impedance	Standard ECL (10K or 10KH series)
Receiver impedance	110 ohms nominal, balanced

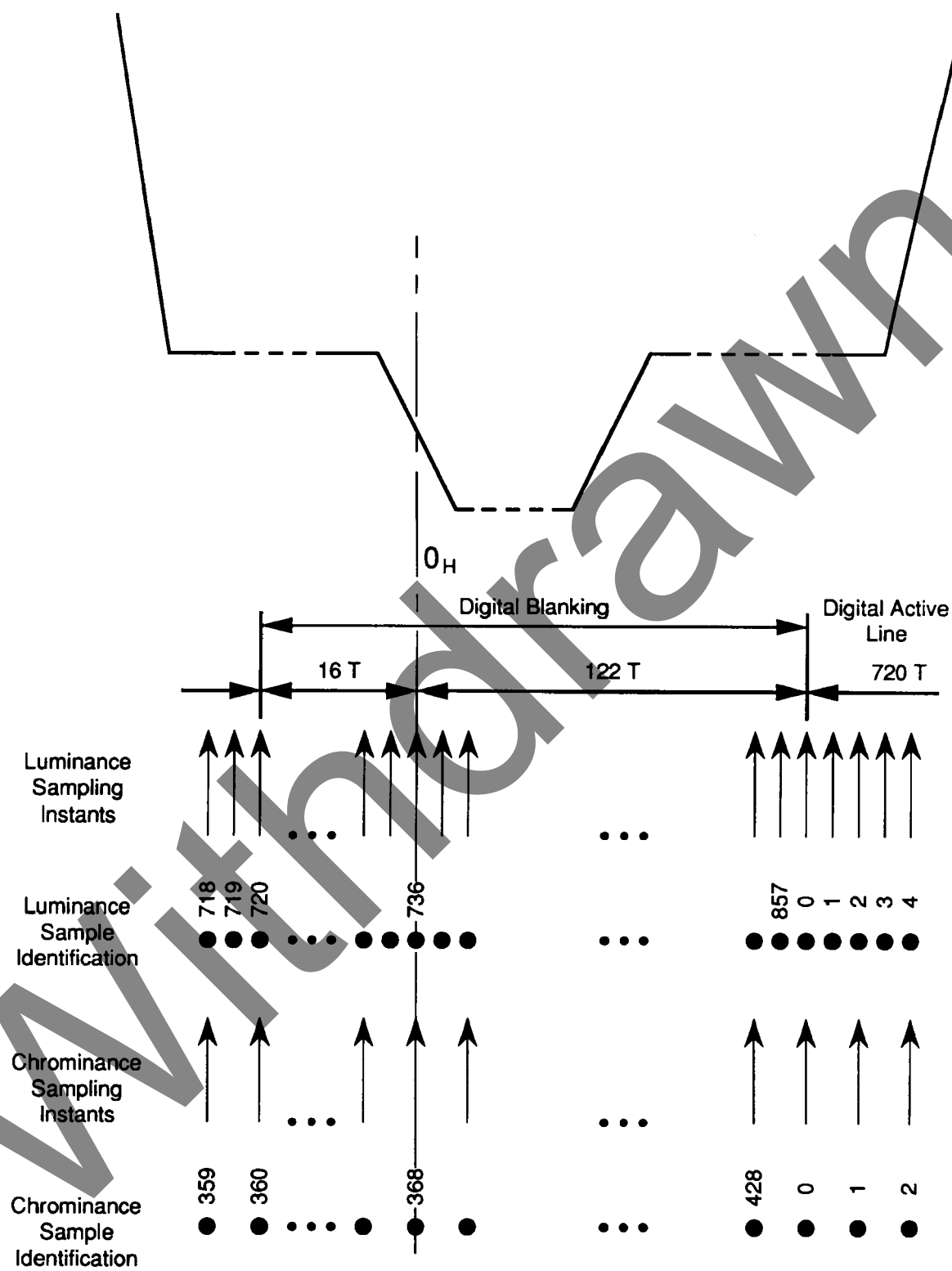


Figure 2a – Horizontal sync relationship — 13.5-MHz sampling

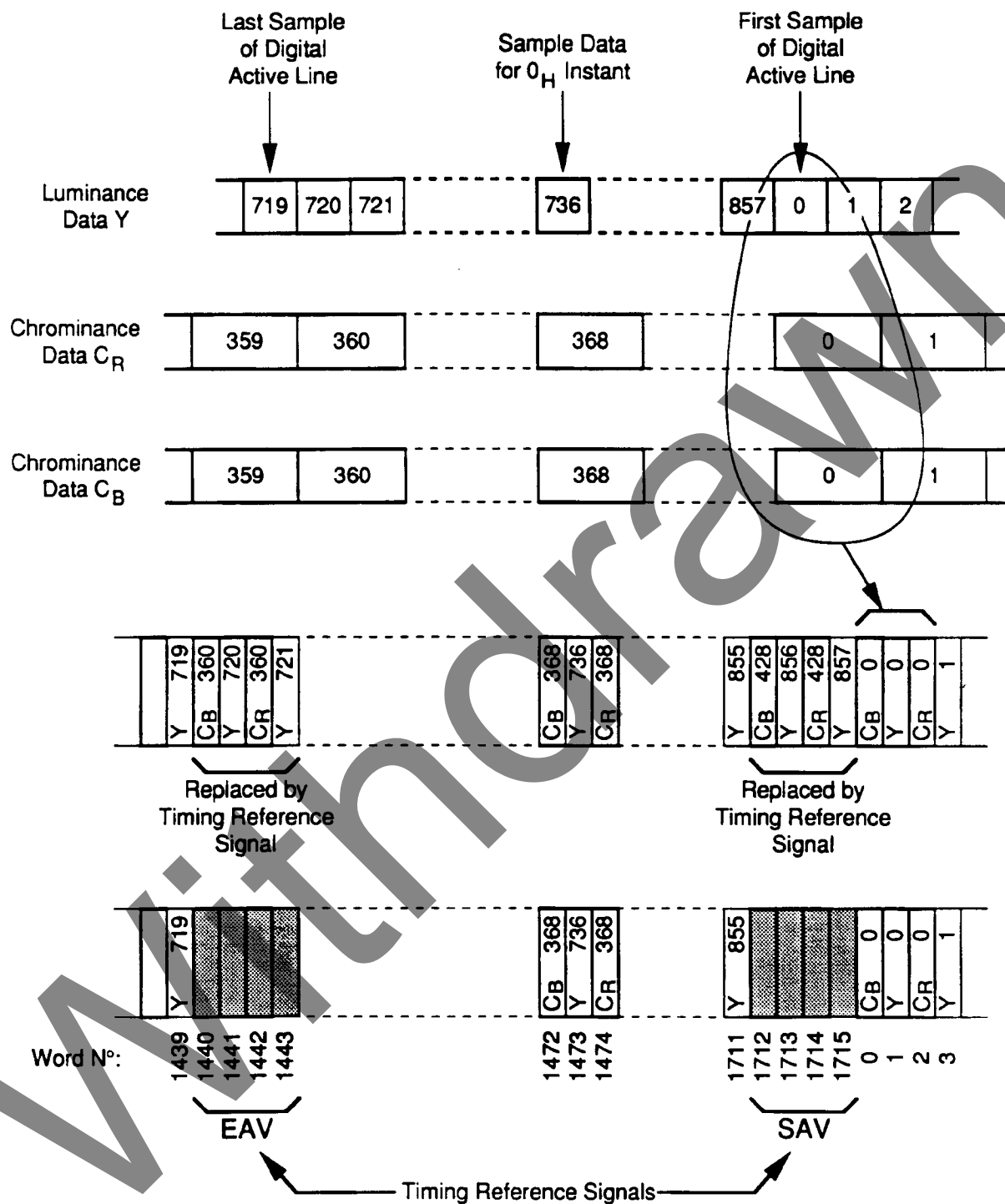


Figure 2b – Multiplex structure — 13.5-MHz sampling

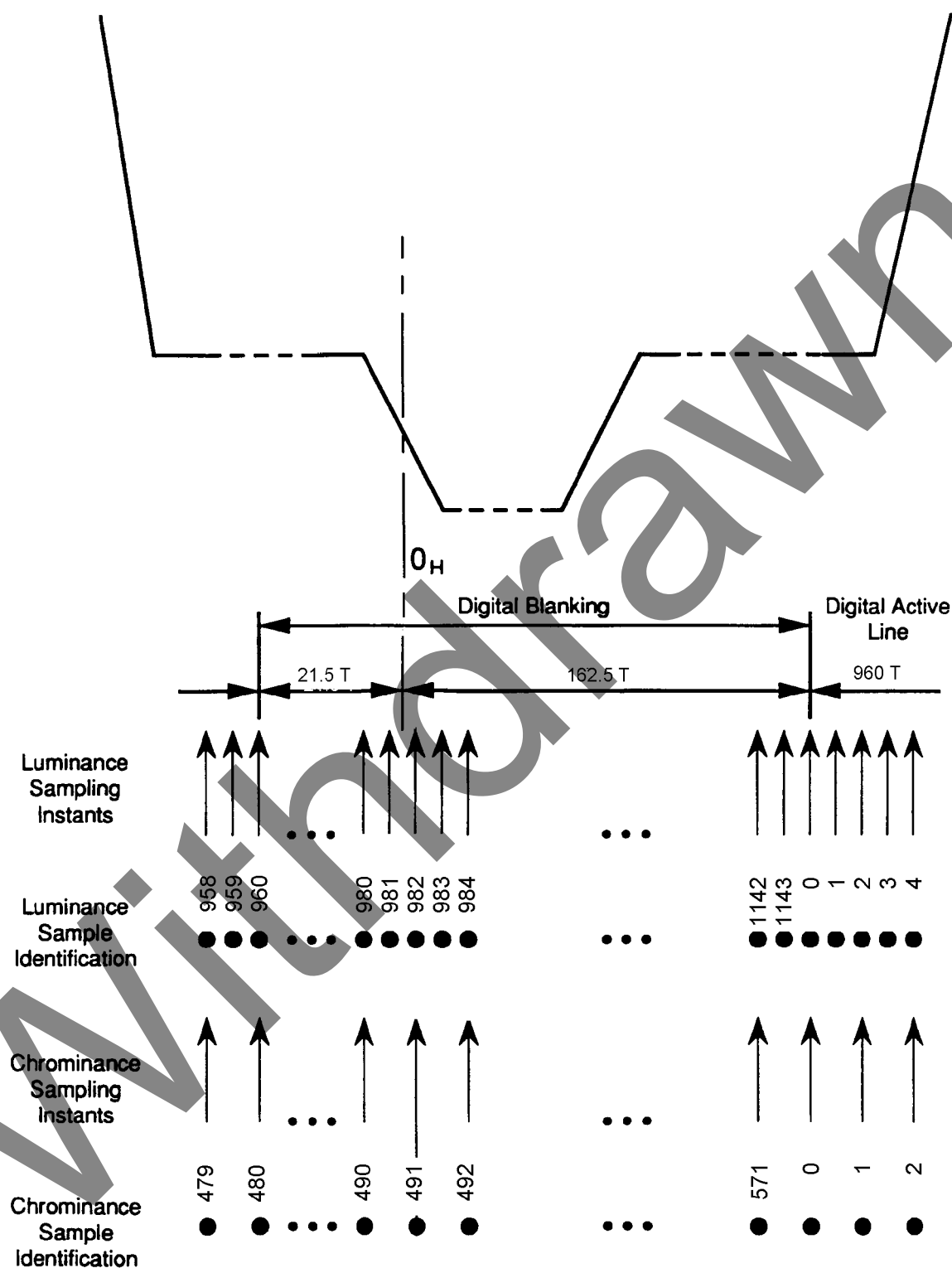


Figure 2c – Horizontal sync relationship — 18-MHz sampling

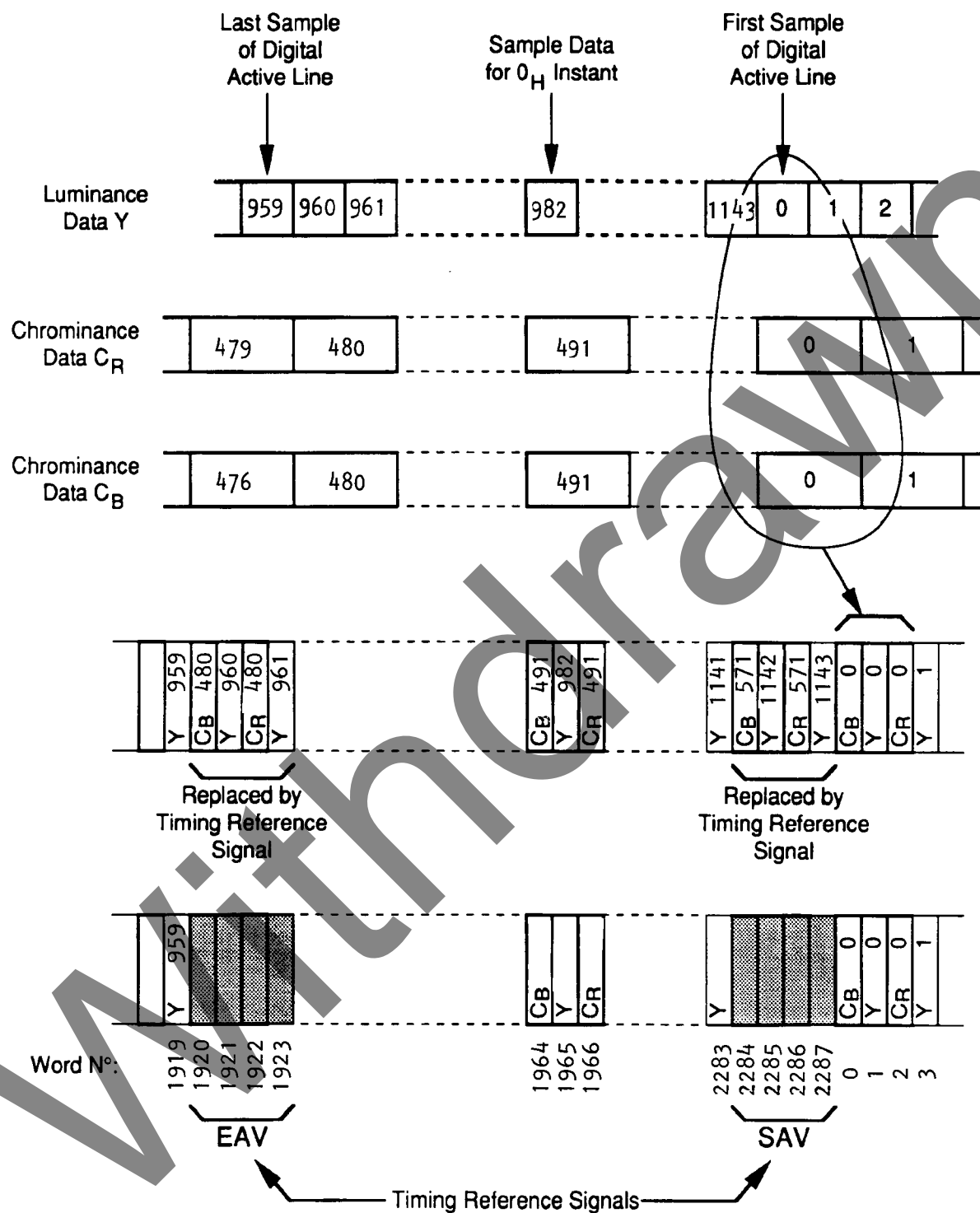


Figure 2d – Multiplex structure — 18-MHz sampling

The first of these 2288 interface clock intervals is designated line word 0 for the purpose of reference only. The 2288 sample words per total line are therefore numbered 0 through 2287. Intervals 0 through 1919, inclusive, contain video data. The interface clock intervals occurring during digital blanking are designated 1920 through 2287.

Intervals 1920 through 1923 are reserved for the end-of-active-video (EAV) timing reference described in 4.5.3. Intervals 2284 through 2287 are reserved for the start-of-active-video (SAV) timing reference described in 4.5.3.

The half-amplitude point of the leading (falling) edge of the analog horizontal sync signal shall be halfway between the sample points which would be conveyed by luminance samples 981 and 982 if carried across the interface. Placement of horizontal sync between the two samples is explained by figure G.1.

4.4.3 Vertical sync relationship

Figure 3 shows the relationship between video signals in the digital and analog domains for 525-line systems.

4.5 Video data signal format

4.5.1 Data signal format

Data is transmitted across the interface on 10 data pairs: DATA 0 through DATA 9. DATA 9 is the most significant bit (MSB). Of the 1024 levels, 1016 are used to express quantized values (digital levels 4 through 1019 or 004_h through 3FB_h in the hexadecimal representation) of the 10-bit word.

Data levels 0 to 3 and 1020 to 1023 (000_h to 003_h and 3FC_h to 3FF_h in the hexadecimal representation) are reserved to indicate timing references.

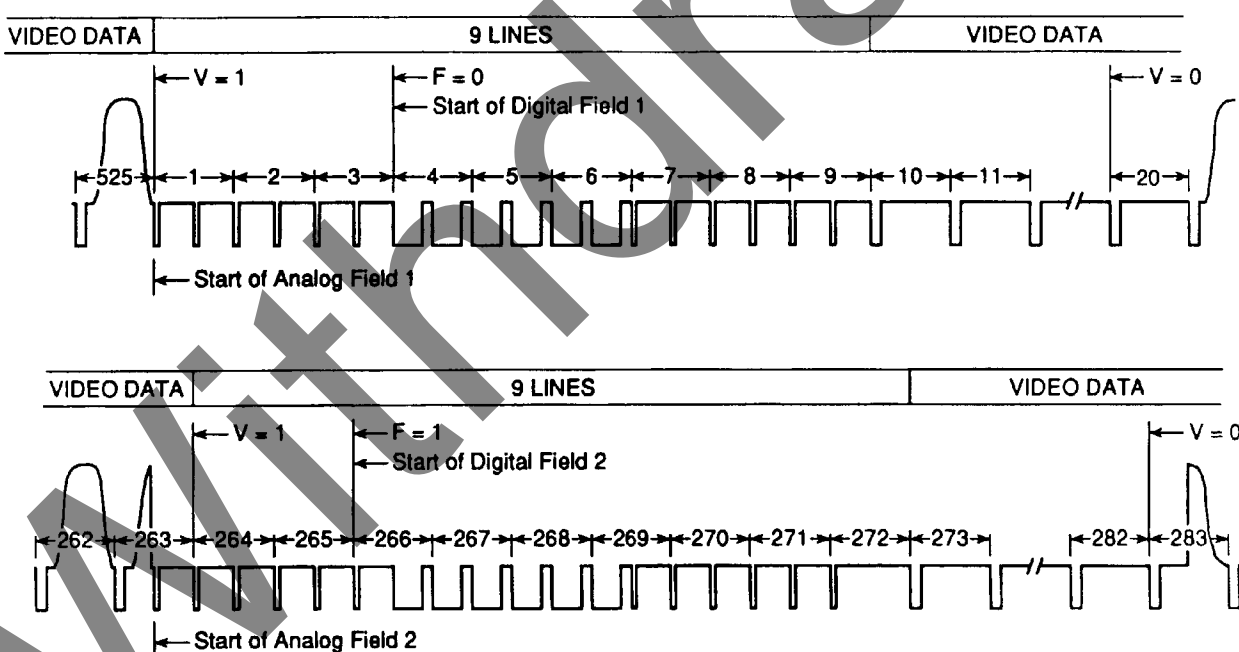


Figure 3 – Relationship of video data/vertical sync

4.5.2 Multiplex structure

The video data words shall be conveyed as a 27 Mword/s multiplex for 13.5-MHz sampling and 36 Mword/s multiplex for 18-MHz in the following order:

$C_B \ Y \ C_R \ [Y] \ C_B \dots$

where the three words $C_B \ Y \ C_R$ refer to cosited samples, the following word $[Y]$ being an isolated luminance-only sample. The C_B and C_R samples are cosited with the first and subsequent alternate Y samples (0, 2, 4...) on each line. (See figures 2b and 2d.) The first video data word in each active line period shall be C_B .

4.5.3 Timing reference signals — Video

Figures 2a and 2c show the position of the timing reference signals with respect to horizontal blanking in the multiplexed data stream. It is implicit that the timing reference signals are contiguous with the video data, when present, and continue through the vertical blanking interval.

Each timing reference signal consists of a four-word sequence in the following format:

3FF 000 000 XYZ

Because of the existence of both 8-bit and 10-bit data, for detection purposes all values in the ranges 000_h-003_h and 3FC_h-3FF_h must be considered equivalent to 000_h and 3FF_h, respectively.

The first three words are a fixed preamble. The fourth word shall contain information defining:

- even field (field 2) identification;
- state of vertical blanking;
- state of horizontal blanking.

Figure 4 is a spatial representation of the timing reference signals during a television frame. Assignment of bits within the fourth word is shown in table 3. Values for F and V change in the EAV associated with the blanking interval of the line number indicated. $P0$, $P1$, $P2$, and $P3$ have states dependent on states of bits F , V , and H according to table 4. Lines are numbered from 1 through 525 as shown in figure 3. Vertical blanking in the digital interface is in full-line increments. EAV and SAV are the digital horizontal synchronization signals and occur on every line.

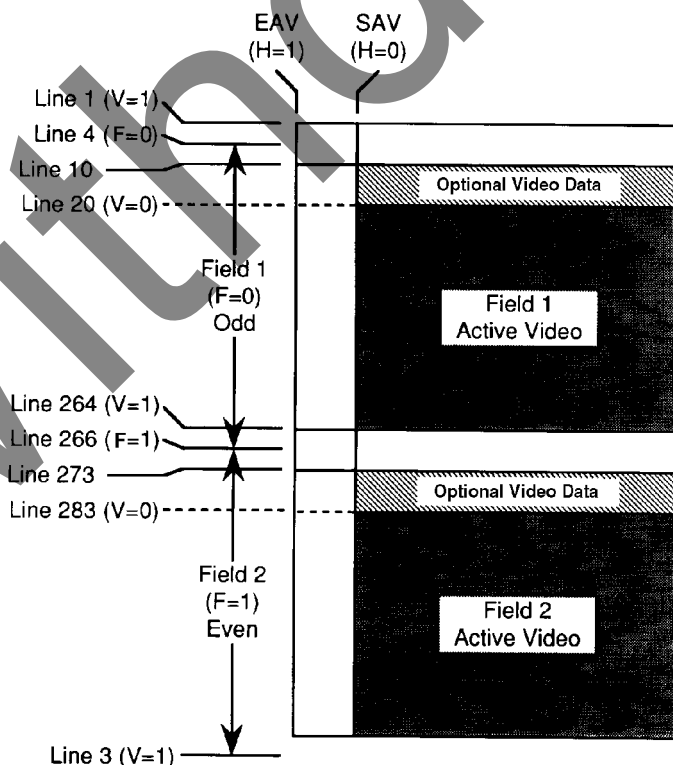


Figure 4 – Timing reference signal locations

Table 3 – Timing reference signals

13.5/18-MHz sampling Bit	Words 1440/1920 and 1712/2284	Words 1441/1921 and 1713/2285	Words 1442/1922 and 1714/2286	Words 1443/1923 and 1715/2287	
9	1	0	0	1	Fixed
8	1	0	0	F	F = 0 during field 1 F = 1 during field 2
7	1	0	0	V	V = 0 during active video V = 1 during vertical blanking
6	1	0	0	H	H = 1 for EAV H = 0 for SAV
5	1	0	0	P3	} See table 4
4	1	0	0	P2	
3	1	0	0	P1	
2	1	0	0	P0	
1	1	0	0	0	
0	1	0	0	0	

NOTES

- 1 Some equipment can only sense the eight most significant bits.
- 2 The H, V, and F bits (bits 6-8) provide all the necessary information. Bits 2-5 provide error detection and correction information.
- 3 Each 525-line digital video frame is divided into two fields. Field 1 contains 262 complete horizontal lines. Field 2 contains 263 complete horizontal lines.
- 4 The protection bits allow correction of all single-bit errors and detection of two-bit errors.

Table 4 – Protection bit states

Bit	9	8	7	6	5	4	3	2	1	0
		F	V	H	P3	P2	P1	P0		
1	0	0	0	0	0	0	0	0	0	0
1	0	0	1	1	1	0	1	0	0	0
1	0	1	0	1	0	1	1	0	0	0
1	0	1	1	0	1	1	0	0	0	0
1	1	0	0	0	1	1	1	0	0	0
1	1	0	1	1	0	1	0	0	0	0
1	1	1	0	1	1	0	0	0	0	0
1	1	1	1	0	1	1	0	0	0	0
1	1	1	1	1	0	0	0	1	0	0

The interval starting at EAV and ending with SAV is the digital horizontal blanking period as shown in figures 2b and 2d.

Small blocks of data, less than 268 words in total length for 13.5-MHz sampling and 360 words in total length for 18-MHz sampling, including the HANC sequence (as described in 4.6.1), can be transmitted within the horizontal blanking period on every line.

Large blocks of data, up to 1440 words in total length for 13.5-MHz sampling and up to 1920 words in total length for 18-MHz sampling, including the VANC sequence, can be transmitted within the interval starting with the end of SAV and terminating with the beginning of EAV on lines 1 through 19 and 264 through 282 only.

Video data will not be present on lines 1-9 and 264-272 and may optionally be present on lines 10-19 and 273-282. Ancillary data could be optionally transmitted in the active portion of these lines.

The words during:

- horizontal blanking period on every line;
- the active portion of lines 1-9 and 264-272;
- the active portion of lines 10-19 and 273-282 (when video data is present)

not used to transmit ancillary data must have the following values:

- the words corresponding to Y samples must have the value 040_h;
- the words corresponding to C_B and C_R samples must have the value 200_h.

4.6 Ancillary data signal format

Ancillary data may be inserted in any portion of the data stream not occupied by timing reference signals or video data (see 4.4.1, 4.4.2, and 4.4.3). Two categories of ancillary data, HANC and VANC, are defined for different portions of the data stream. Note that the three-word header used to identify ancillary data is the same for HANC and VANC.

4.6.1 HANC data

HANC data are permitted in all horizontal intervals, but not in the active portion of lines. HANC data are

of 10-bit format, and each block of HANC data is preceded by the three-word ancillary data header 000_h 3FF_h 3FF_h.

Because of the existence of 8-bit data, for detection purposes all values in the ranges 000_h-003_h and 3FC_h-3FF_h must be considered equivalent to 000_h and 3FF_h, respectively.

The ancillary data header may occur multiple times during each horizontal blanking period if different blocks of data are transmitted.

All permitted data identification words and data formats will protect the values (000_h to 003_h) and (3FC_h to 3FF_h).

4.6.2 VANC data

VANC data are permitted only in the active portion of lines 1-13, 15-19, 264-276, and 278-282. (Lines 14 and 277 are reserved for digital vertical interval time code [DVITC] and video index.) VANC data are of 8-bit format, and each block of VANC data is preceded by the three-word ancillary data header 000_h 3FF_h 3FF_h.

Because of the existence of 8-bit data, for detection purposes all values in the ranges 000_h-003_h and 3FC_h-3FF_h must be considered equivalent to 000_h and 3FF_h, respectively.

The ancillary data header may occur multiple times during each line period if different blocks of data are transmitted.

All permitted data identification words and data formats will protect the values (000_h to 003_h) and (3FC_h to 3FF_h).

4.7 Digital vertical interval time code and video index

Digital vertical interval time code (DVITC) and video index, if present, are carried by the data in the active portion of lines 14 and 277.

4.7.1 DVITC

This signal, if present, is carried by the luminance data in the active portion of lines 14 and 277.

4.7.2 Video index

This signal, if present, is carried by the color-difference data in the active portion of lines 14 and 277. A total of 90 8-bit data words is represented serially by DATA(2) of the 720 color-difference samples of the active portion of the line for 13.5-MHz sampling. A total of 90 8-bit data words is represented serially by DATA(2) of the 960 color-difference samples of the active portion of the line for 18-MHz sampling.

The first color-difference word of the active portion of the line (word 0 of the multiplexed signal, normally a C_B sample) represents the least significant bit (bit 0) of video index word 0. The second color-difference word represents bit 1 of the same word, etc. The last color-difference word of the active portion of the line (word 1438 of the multiplexed signal, normally a C_R sample) represents the most significant bit (bit 7) of video index word 89 for 13.5-MHz sampling. The color-difference word 1438 of the active portion of the multiplexed signal (normally a C_R sample) represents the most significant bit (bit 7) of video index word 89 for 18-MHz sampling.

For all samples, a value of 204_h represents a binary one for the appropriate video index bit, and a value of 200_h represents a binary zero for the appropriate video index bit.

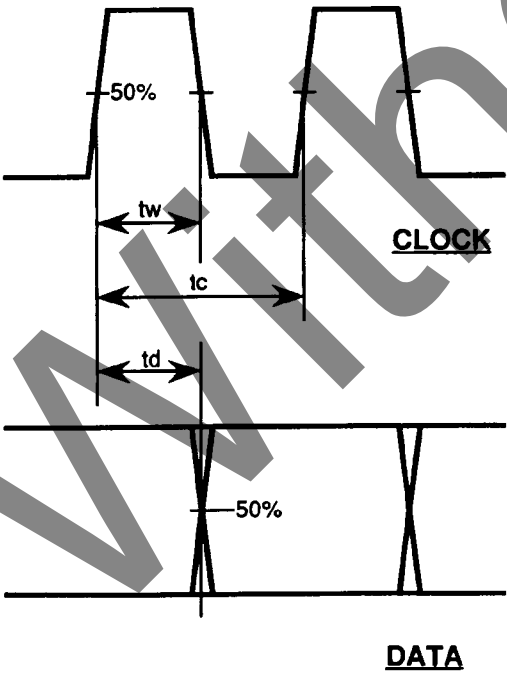
This transmission method ensures that, after digital to analog conversion, the video signal may be sent to an NTSC encoder without any requirement for special blanking. DVITC will be preserved through the encoder without interference from any video index information which may be present.

4.8 Clock signal

4.8.1 Clock signal description (at transmitter)

For 13.5-MHz sampling, the clock signal is a 27-MHz square wave as shown in figure 5. The clock pulse width (tw) is 18.5 ns ± 3 ns.

For 18-MHz sampling, the clock signal is a 36-MHz square wave as shown in figure 5. The clock pulse width (tw) is 13.9 ns ± 2 ns.



Parameter	13.5-MHz sampling	18-MHz sampling
tw	18.5 ns ± 3 ns	13.9 ns ± 2 ns
tc	37.0 ns (nominal)	27.8 ns (nominal)
td	18.5 ns ± 3 ns	13.9 ns ± 2 ns
fh	15.734 ... kHz (nominal)	

Figure 5 – Clock to data timing (at transmitter)

4.8.2 Clock jitter

For 13.5-MHz sampling, the peak-to-peak jitter between rising edges shall be within 3 ns of the average time of the rising edge computed over at least one field.

For 18-MHz sampling, the peak-to-peak jitter between rising edges shall be within 2 ns of the average time of the rising edge computed over at least one field.

NOTE – Designers of equipment receiving signals from this interface should consider that the jitter requirements for a digital to analog converter may be more restrictive than those of the interface.

4.8.3 Clock data timing relationship

The positive transition of the clock signal nominally occurs midway between data transitions (figure 5).

5 Electrical characteristics

5.1 General

The 11 signals shall be transmitted via balanced signal pairs. Although the use of ECL technology is not specified, the line driver and receiver must be ECL-compatible to permit the use of standard ECL parts for either or both ends in applications where such ECL parts are deemed adequate. (Standard ECL parameters are provided in annex A.)

5.2 Transmitter characteristics

5.2.1 Output impedance

The transmitter shall have a balanced output with a maximum output impedance of 110 ohms.

5.2.2 Common mode voltage

The average of the voltages on the two terminals of the line driver shall be $-1.3 \text{ V} \pm 15\%$ with reference to the ground terminal.

5.2.3 Signal amplitude

The generated signal shall lie between 0.8 V peak-to-peak and 2.0 V peak-to-peak, measured across a 110-ohm resistor connected to the output terminals without any transmission line.

5.2.4 Rise and fall times

Rise and fall times shall be no longer than 5 ns and differ by not more than 2 ns, as measured between the 20% and 80% amplitude points across a 110-ohm resistor connected to the output terminals without any transmission line.

5.3 Receiver characteristics

5.3.1 Terminating impedance

The cable shall be terminated by $110 \text{ ohms} \pm 10 \text{ ohms}$.

5.3.2 Maximum input signal

The line receiver must sense properly the binary data when connected directly to a line driver operating at the extreme voltage limits permitted by 5.2.3.

5.3.3 Input sensitivity

The receiver shall require a differential input voltage of no more than 185 mV to correctly attain the intended binary state.

5.3.4 Common mode rejection

The receiver shall operate correctly in the presence of common mode noise having a maximum amplitude of 0.5 V.

5.3.5 Differential delay

The receiver shall operate with a differential delay between the received clock and any received data signals up to 11 ns for 13.5-MHz sampling and 7 ns for 18-MHz sampling.

6 Mechanical characteristics

6.1 General

This clause defines the mechanical specifications for the interface of digital video systems used in environments where the physical distance between devices is limited and the general physical environment can be termed interior.

6.2 Interconnecting cable characteristics

The interface is designed to operate with a nominal signal pair impedance of 110 ohms.

6.2.1 Cable length

The majority of applications of this interface involve lengths less than 50 m for 13.5-MHz sampling and 40 m for 18-MHz sampling. For these lengths, cables with reasonable uniformity will generally give satisfactory results. For cable lengths greater than 50 m for 13.5-MHz sampling and 40 m for 18-MHz sampling, the cable and termination characteristics become more critical, in some cases requiring equalization.

6.2.2 Cable construction

The cable shall contain 12 pairs of conductors of which 11 pairs shall be used as signal lines. The remaining pair shall be used as system ground.

The cable shall be constructed to minimize the effects of crosstalk between signal lines, the susceptibility of the signal lines to external noise, and the transmission of interface signals to the external environment.

The cable shall contain an overall shield to minimize radiation, carried through the cable assembly and connectors via the cable shield pins and the connector body at each end.

The cable shall be constructed to minimize the differential delay between any two conductor pairs.

6.3 Connector characteristics

6.3.1 Mechanical considerations

The connectors shall have the mechanical characteristics conforming to the industry standard 25-contact D subminiature connector described below. Additional information may be found in MIL-C-24308C.

(Most applications of this interface require that the connectors be inserted many times. ECL voltage and current levels are relatively low. The materials used in the connector should be appropriate to the application.)

6.3.2 Connector contact assignments

The connector contact assignments shall be in accord with table 5.

6.3.3 Cable connector assembly

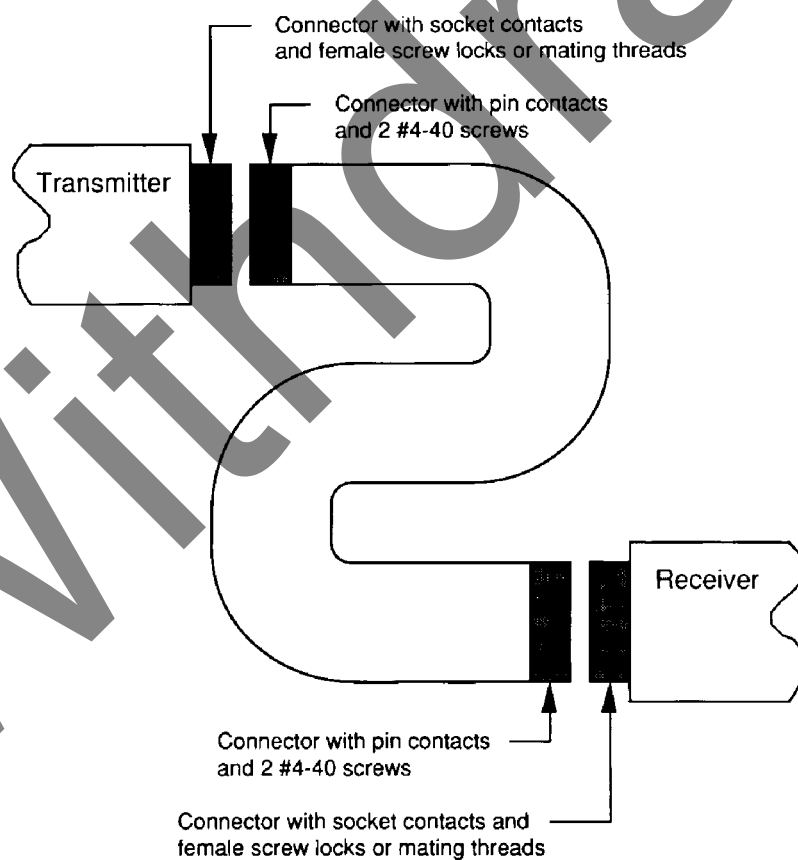
Cable connectors employ pin contacts and equipment connectors employ socket contacts (see figure 6).

6.3.4 Connector retaining mechanism

The cable connectors shall be provided with #4-40 mounting screws and the equipment connectors shall be provided with female screw locks or mating threads as shown in annex B.

Table 5 – Connector contact assignments

Pin	Signal line	Pin	Signal line
1	Clock	14	Clock return
2	System ground A	15	System ground B
3	DATA 9	16	DATA 9 return
4	DATA 8	17	DATA 8 return
5	DATA 7	18	DATA 7 return
6	DATA 6	19	DATA 6 return
7	DATA 5	20	DATA 5 return
8	DATA 4	21	DATA 4 return
9	DATA 3	22	DATA 3 return
10	DATA 2	23	DATA 2 return
11	DATA 1	24	DATA 1 return
12	DATA 0	25	DATA 0 return
13	Cable shield		

**Figure 6 – Cable connector assembly**

Annex A (normative)

ECL 10,000 and 10H000 parameters

A.1 Standard ECL parameters

"Standard ECL" in this application means an integrated circuit device of the ECL 10,000 or 10H000 series or equivalent. Typical key parameters are:

System power supply (V): -4.7 V to -5.7 V ; -5.2 V nominal;

Logic states with respect to ground (typical): "1" = -0.8 V = High (H); "0" = -1.85 V = Low (L);

Output impedance: Open emitter-follower output (7 ohm typical) to drive terminated lines;

Propagation delay ECL 10,000: 2-3 ns per gate; typical edge speeds are 2-3 ns (20% to 80%);

Propagation delay ECL 10H000: 1-2 ns per gate; typical edge speeds are 1-2 ns (20% to 80%).

A.2 Balanced interface circuit

Each circuit consists of three parts as shown in figure A.1: the line driver, the balanced interconnecting cable, and the load. The line driver is comprised of a single transmitter (T) with a low-output impedance. The load is comprised of a single receiver (R), and a cable termination impedance (Z_t).

Electrical characteristics of the receiver without cable termination shall conform to standard balanced ECL specifications. Use of a cable termination (Z_t) is mandatory. Z_t shall be nominally 110 ohms.

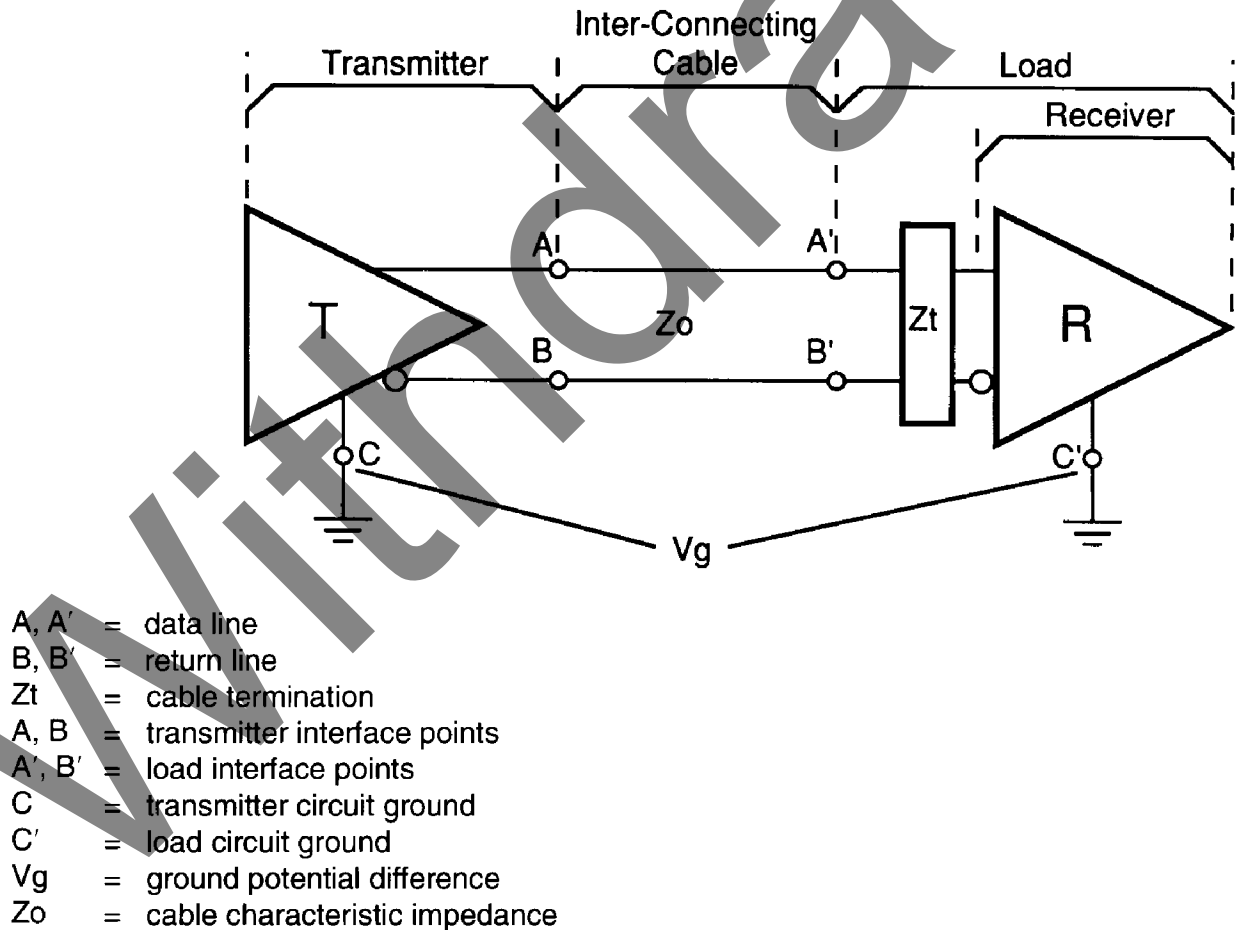


Figure A.1 – Balanced interface circuit

Annex B (normative)

Connector characteristics

The interface employs the 25 contact D subminiature connector, with the connectors on the transmitter and receivers using socket contacts and the connectors on the cable both using pin contacts. Connectors are locked together by two #4-40 screws on the cable connectors, which go in female screw locks mounted on the equipment connector.

Detailed dimensions for the connector are given in MIL-C-24308C.

The relative position of the connector and the female screw lock is defined in figure B.1. Recommended minimum connector spacing is defined in figure B.2.

It is recommended that the cable connectors employ a conductive backshell to maintain shielding of the signal conductors. Care must be taken to select designs that are appropriate for use with the screw-latching method specified.

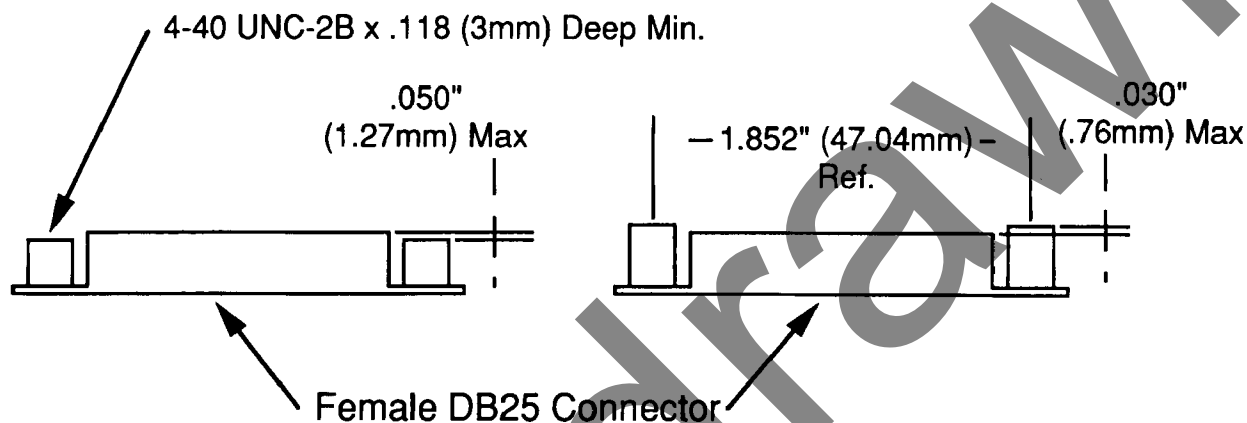


Figure B.1 – Female screw lock mounting

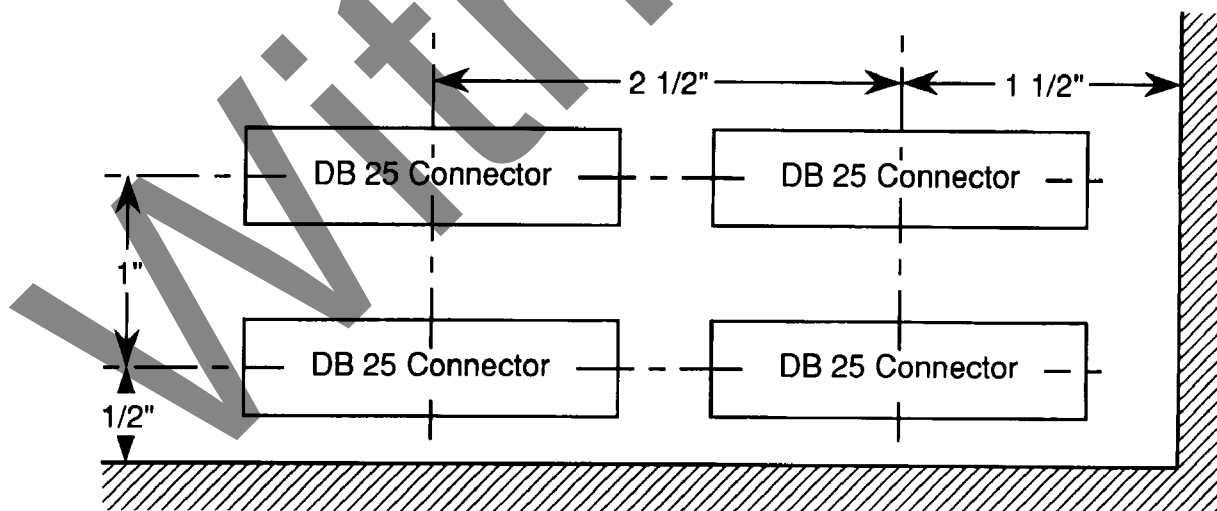


Figure B.2 – Minimum connector spacing

Annex C (informative)

Cable shield pin

The cable shield (pin 13) is for the purpose of controlling electromagnetic radiation from the cable. It is recommended that pin 13 provide high-frequency continuity to the chassis

ground at both ends and, in addition, provide dc continuity to the chassis ground at the transmit end.

Annex D (informative)

Connector orientation

Vertical or horizontal mounting: Contact 1 uppermost.

Annex E (informative)

Monochrome operation

Monochrome operation at 29.97 Hz frame rate can be achieved by setting the color-difference signals (C_B , C_R) to zero (200_h).

Annex F (informative)

Error detection and correction in the video timing reference signal

Table F.1 enables single-bit errors in the fourth bytes of EAV and SAV to be corrected. Double errors, and some multiple-bit errors, are detected but not corrected. The table gives

corrected values for bits 8, 7, and 6 where possible. Multiple errors are denoted by asterisks.

Table F.1 – Error correction table

Received P3 – P0	Received bits 8, 7, and 6 (F, V, and H)							
	000	001	010	011	100	101	110	111
0000	000	000	000	*	000	*	*	111
0001	000	*	*	111	*	111	111	111
0010	000	*	*	011	*	101	*	*
0011	*	*	010	*	100	*	*	111
0100	000	*	*	011	*	*	110	*
0101	*	001	*	*	100	*	*	111
0110	*	011	011	011	100	*	*	011
0111	100	*	*	011	100	100	100	*
1000	000	*	*	*	*	101	110	*
1001	*	001	010	*	*	*	*	111
1010	*	101	010	*	101	101	*	101
1011	010	*	010	010	*	101	010	*
1100	*	001	110	*	110	*	110	110
1101	001	001	*	001	*	001	010	*
1110	*	*	*	011	*	101	110	*
1111	*	001	010	*	100	*	*	*

Annex G (informative)

Picture centering

Relative horizontal picture centering for 13.5-MHz and 18-MHz sampling structures is shown in figure G.1.

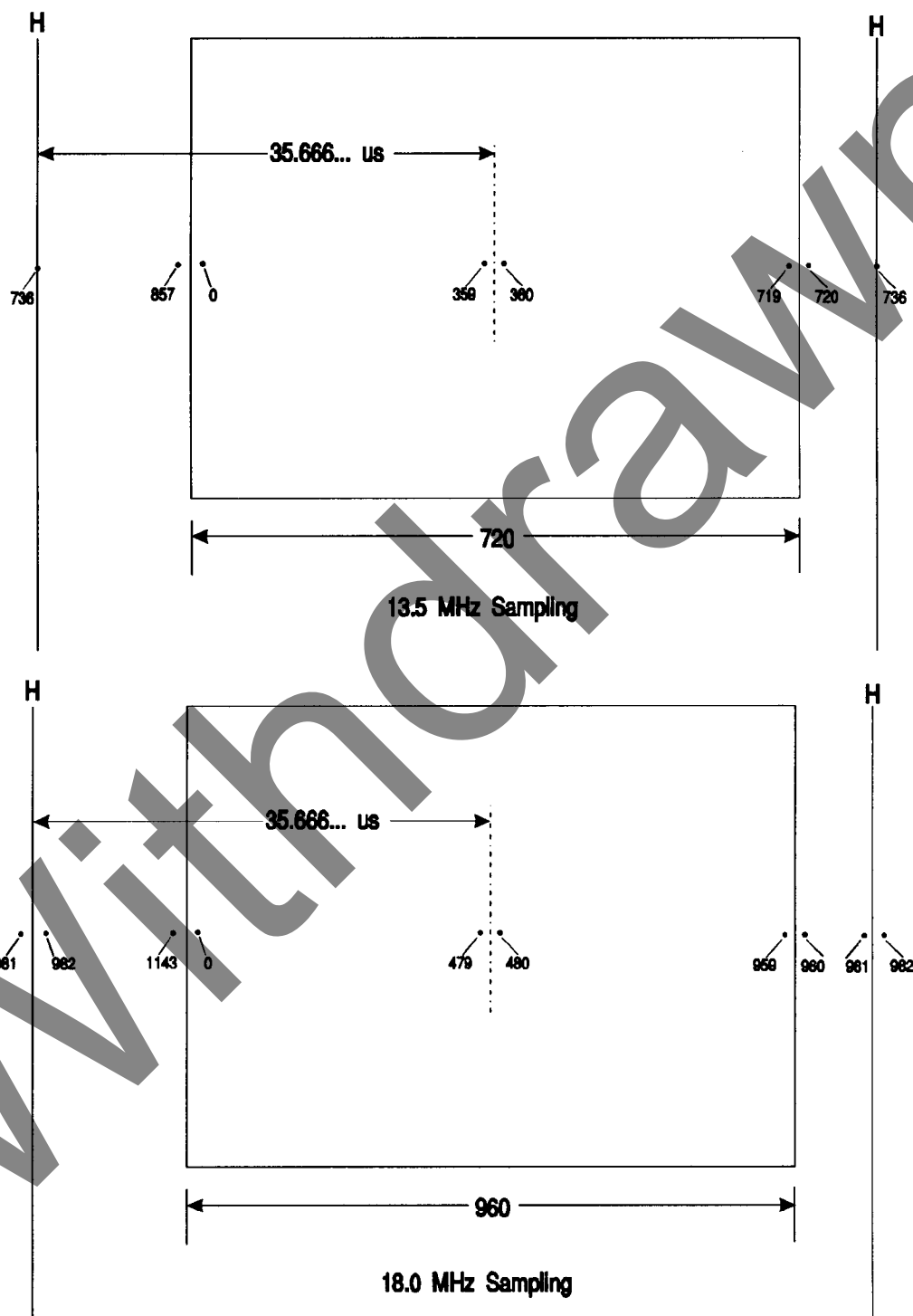


Figure G.1 – Horizontal picture centering for 525/59.94 component systems

Annex H (informative)**Bibliography**

ANSI/SMPTE 125M-1992, Television — Component Video Signal 4:2:2 — Bit-Parallel Digital Interface

ANSI/SMPTE 259M-1993, Television — 10-Bit 4:2:2 Component and $4f_{sc}$ NTSC Composite Digital Signals — Serial Digital Interface

MIL-C-24308C, General Specification for Connectors, Electric, Rectangular, Nonenvironmental, Miniature, Polarized Shell, Rack and Panel

ITU-R 601-3, Encoding Parameters of Digital Television for Studios

ITU-R Report 962-1, The Filtering, Sampling and Multiplexing for Digital Encoding of Colour Television Signals

Documents are in preparation to cover auxiliary signals (HANC, VANC, DVITC, and video index), but are not yet available.