SMPTE 306M-2002
Revision of
SMPTE 306M-1998

SMPTE STANDARD

for Television — 6.35-mm Type D-7 Component Format — Video Compression at 25 Mb/s and 50 Mb/s — 525/60 and 625/50

Table of contents

Abbreviations and Acronyms

AAUX	Audio auxiliary data
AP1	Audio application ID
AP2	Video application ID
AP3	Subcode application ID
APT	Track application ID
Arb	Arbitrary
AS	AAUX source pack
ASC	AAUX source control pack
B/W	Black and white flag
CGMS	Copy generation management system
DBN	DIF block number
DCT	Discrete cosine transform
DIF	Digital interface
DSF	DIF sequence flag
ECC	Error correction code

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NOTE: Figures 63 and 64 Corrected September 30, 2002
Approved March 15, 2002

EFC	Emphasis channel flag
EOB	End of block
ID	Identification
IDP	ID parity
ITI	Insert and track information
LF	Locked mode flag
PF	Pilot frame
QNO	Quantization number
QU	Quantization
Res	Reserved for future use
SMP	Sampling frequency
SSA	Start sync area
SSYB	Subcode sync block number
STA	Status of the compressed macro block
Syb	Sync block number
TF	Transmitting flag
TIA	Track information area
Trp	Track pair number
VAUX	Video auxiliary data
VLC	Variable length coding
VS	VAUX source pack
VSC	VAUX source control pack
VSM	Vibrating sample magnetometer

1 Scope

This standard specifies the content, format and recording method of the data blocks containing video, audio, and associated data which form the helical records on 6.35-mm tape contained in cassettes as specified in SMPTE 307M.

In addition, this standard specifies the content, format, and recording method for longitudinal cue and control tracks.

One video channel and two independent audio channels are recorded in the digital format for 25 Mb/s VTRs and one video channel and four independent audio channels for 50 Mb/s VTRs. Each of these channels is designed to be capable of independent editing.

The video channel records and reproduces a component television signal in the 525-line system with a frame frequency of 29.97 Hz (hereinafter referred to as the 525/60 system) and the 625-line system with a frame frequency of 25.00 Hz (hereinafter referred to as the 625/50 system).

Prior to recording, the digital signal shall be compressed to a DV-based 25 Mb/s bit stream with 4:1:1 sampling or a DV-based 50 Mb/s bit stream with 4:2:2 sampling.

The standard includes the process required to decode the DV-based 25 Mb/s bit stream and 50 Mb/s bit stream into output video, audio, and data.

2 Normative reference

The following standard contains provisions which, through reference in this text, constitute provisions of this standard. At the time of publication, the edition indicated was valid. All standards are subject to revision, and parties to agreements based on this standard are encouraged to investigate the possibility of applying the most recent edition of the standard indicated below.

AES3-1992, Serial Transmission Format for Two-Channel Linearly Represented Digital Audio Data

ANSI/SMPTE 12M-1999, Television, Audio and Film — Time and Control Code

SMPTE 307M-2002, Television Digital Recording — 6.35-mm Type D-7 and Type D-12 Component Format — Tape Cassette

SMPTE 314M-1999, Television — Data Structure for DV-Based Audio, Data and Compressed Video — 25 and 50 Mb/s [see note 1]

SMPTE 321M-2002, Television — Data Stream Format for the Exchange of DV-Based Audio, Data and Compressed Video over a Serial Data Transport Interface [see note 2]

ITU BT.601-5, Studio Encoding Parameters of Digital Television for Standard 4:3 and Wide-Screen 16:9 Aspect Ratios

NOTES

1 Contents of this document related to compression are the same as in the referred document.

2 If equipment conforming to this standard includes a serial digital interface based on SMPTE 305.2M (SDTI), such an interface shall conform to SMPTE 321M. The presence of such an interface is optional.

– Barometric pressure: From 86 kPa to 106 kPa
– Tape conditioning: Not less than 24 h
– Center tape tension: 0.09 N ± 0.02 N (see annex A)

3 Environment and test conditions

3.1 Environment

Tests and measurements made on the system to check the requirements of this standard shall be carried out under the following conditions:

– Temperature: 20°C ± 1°C
– Relative humidity: (50 ± 2)%

3.2 Reference tape

A blank tape for reference recordings shall be available from the format holder or approved source.

3.3 Calibration tapes

The calibration tapes meeting the requirements of clauses 3.3.1, 3.3.2, and 4 shall be made available from manufacturers who produce digital television tape recorders and players in accordance with this standard.

3.3.1 Record locations and dimensions

Calibration tape shall be manufactured to tolerances shown in table 1 or table 2 for 25 Mb/s format or table 3 or table 4 for 50 Mb/s format but with these tolerance reduced by 50%.

3.3.2 Calibration signals

Two sets of signals shall be recorded on the calibration tape:

a) – Video: 100 / 0 / 100 / 0 color bars
– Audio: 1 kHz tone at 20 dB below full scale on each audio channel
– Cue: 1 kHz and 6-kHz tone at the analog recording reference level

b) A signal of constant recorded frequency (i.e., the Nyquist frequency) for the purpose of mechanical alignment. Recording level shall conform to 6.1.4.3

4 Tape

4.1 Base

The base material shall be polyester or equivalent.

4.2 Width

The tape width shall be 6.350 mm ± 0.005 mm.

The tape, covered with glass, is measured without tension at a minimum of five different positions along the tape using a calibrated comparator having an accuracy of 0.001 mm (1 μm). The tape width shall be within the aforementioned specification at any measuring position.

4.3 Width fluctuation

Tape width fluctuation shall not exceed 5 μm peak-to-peak. Measurement of tape width fluctuation shall be taken over a tape length of 900 mm. The tape width fluctuation shall be within the aforementioned specification at each of ten equally spaced points in the 900-mm span.

4.4 Reference edge straightness

The reference edge straightness maximum deviation is 6 μm peak-to-peak. Edge straightness fluctuation is measured at the edge of a moving tape guided by three guides having contact on the same edge and having a distance of 85 mm from the first to second guide and 85 mm from the second to third guide. Edge measurements are averaged over a 10 m length and are made 5 mm from the midpoint between the first and second guide towards the first guide.

4.5 Tape thickness

The total tape thickness shall be 8.8 μm + 0.0 μm - 0.8 μm and 6.7 μm + 0.0 μm - 0.4 μm.

NOTE – Tape of either thickness may be used for 25 Mb/s or 50 Mb/s formats.

4.6 Transmissivity

Transmissivity shall be less than 5 %, measured over the range of wavelengths 800 nm to 1000 nm.

4.7 Offset yield strength

The offset yield strength shall be greater than 3 N. The force to produce 0.2 % elongation of a 1000-mm test sample with a pull rate of 10 mm per minute shall be used to confirm the offset yield strength. The line beginning at 0.2 % elongation parallel to the initial tangential slope is drawn and then read at the point of intersection of the line and the stress-strain curve.

4.8 Magnetic coating

The magnetic layer of the tape shall consist of a coating of metal particles or equivalent.

4.9 Coating coercivity

The magnetic coating coercivity shall be a class 2300 (approximately 2300 Oe / 184000 A/m), with an applied field of 10000 Oe / 800000 A/m measured by a VSM.

5 Helical recordings

5.1 Tape speed

The tape speed for the 25 Mb/s format shall be 33.8201 mm/s for the 525/60 system and 33.8539 mm/s for the 625/50 system. The tape speed for the 50 Mb/s format shall be 67.6401 mm/s for the 525/60 system and 67.7077 mm/s for the 625/50 system. The tolerance shall be ± 0.2 % respectively.

5.2 Sectors

Each recorded track contains an ITI sector, an audio sector, a video sector and a subcode sector.

5.3 Record locations and dimensions

5.3.1 Record locations and dimensions for continuous recording of 25 Mb/s format shall be as specified in figures 1 and 3, and table 1 (525/60 system) or in figures 1 and 3, and table 2 (625/50 system). In recording, sector locations on each helical track shall be contained within the tolerance specified in figure 1 and table 1 (525/60 system) or in figure 1 and table 2(625/50 system).

Record location and dimensions for continuous recording of 50 Mb/s format shall be as specified in figures 2 and 3, and table 3 (525/60 system) or in figures 2 and 3, and table 4 (625/50 system). In recording, sector locations on each helical track shall be contained within the tolerance specified in figure 2 and table 3 (525/60 system) or in figure 2 and table 4 (625/50 system).

5.3.2 The reference edge of the tape for dimensions specified in this standard shall be the lower edge as shown in figures 1 and 2. The magnetic coating, with the direction of tape travel as shown in figures 1 and 2, are on the side facing the observer.

5.3.3 As indicated in figures 1 and 2, this standard anticipates a zero guard band between recorded tracks, and the nominal record head width shall be equal to the track pitch of 18 μm. The scanner head configuration should be chosen such that the recorded track widths are contained within the limits of 16 μm to 20 μm.

5.3.4 The format requires flying erasure for recording. In insert editing, this standard provides a guard band of 3 μm ± 1.5 μm between the previously recorded track and the inserted track at editing points only. A typical track pattern for insert editing is shown in figures B.1 and B.2 of annex B.

5.4 Helical track record tolerance zones

In the case of 25 Mb/s format, the center of two consecutive tracks starting at the first track in each video frame shall be contained within the pattern of the two tolerance zones established in figure 4. Each zone is defined by two parallel lines which are inclined at an angle of 9.1784° basic with respect to the tape reference edge. The centerlines of each zone shall be spaced apart 18.0 μm basic. The width of zone 1 shall be 3 μm and the width of zone 2 shall be 5 μm. These zones are established to contain track angle errors, track straightness errors, and vertical head offset tolerance (the measuring technique is shown in annex C).

In the case of 50 Mb/s format, the lower edge of four consecutive tracks starting at the first track in each video frame shall be contained within the pattern of the four tolerance zones established in figure 5. Each zone is defined by two parallel lines which are inclined at an angle of 9.1784° basic with respect to the tape reference edge. The centerlines of each zone shall be spaced apart 18.0 μm basic. The width of zone 2 shall be 3 μm and the width of zone 1, 3 and 4 shall be 5 μm. These zones are established to contain track angle errors, track straightness errors, and vertical head offset tolerance.

5.5 Relative positions of recorded information

5.5.1 Relative positions of longitudinal tracks

Audio, video, control track and cue track with information intended to be time coincident shall be positioned as shown in figures 1 to 3.

5.5.2 Program area reference point

The program area reference point is determined by the intersection of a line parallel to the reference edge of the tape at a distance Y_0 from the reference edge and the centerline of track 0 in each ITI sector (see figures 1 to 3).

The end of the preamble and beginning of SSA in the ITI sector shall be recorded at the program area reference point, and the tolerance of dimension X_0. The locations are shown in figures 1 to 3; dimensions X_0 and Y_0 are specified in tables 1 to 4. The relationship between sectors and contents of each sector is specified in clause 6.

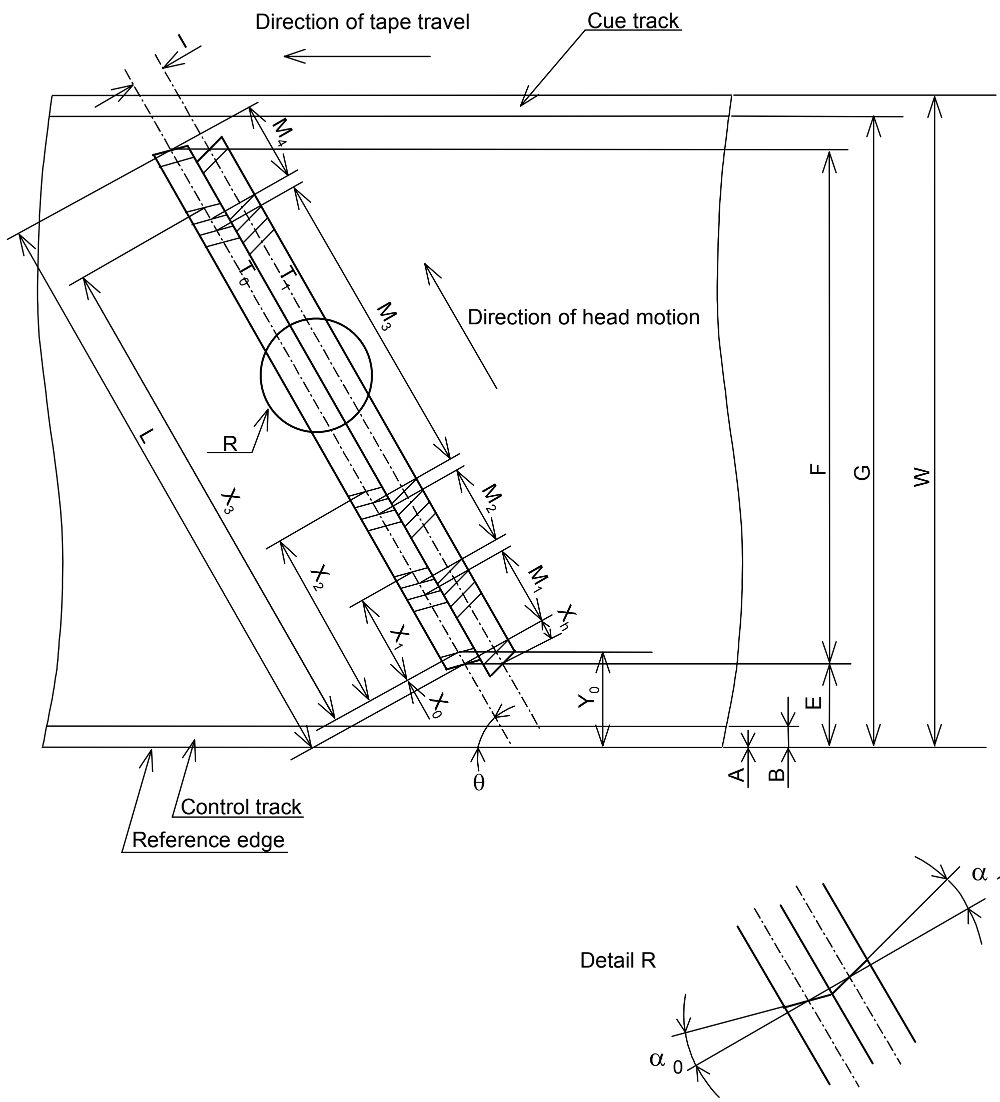


Figure 1 – Locations and dimensions of recorded tracks of 25 Mb/s format

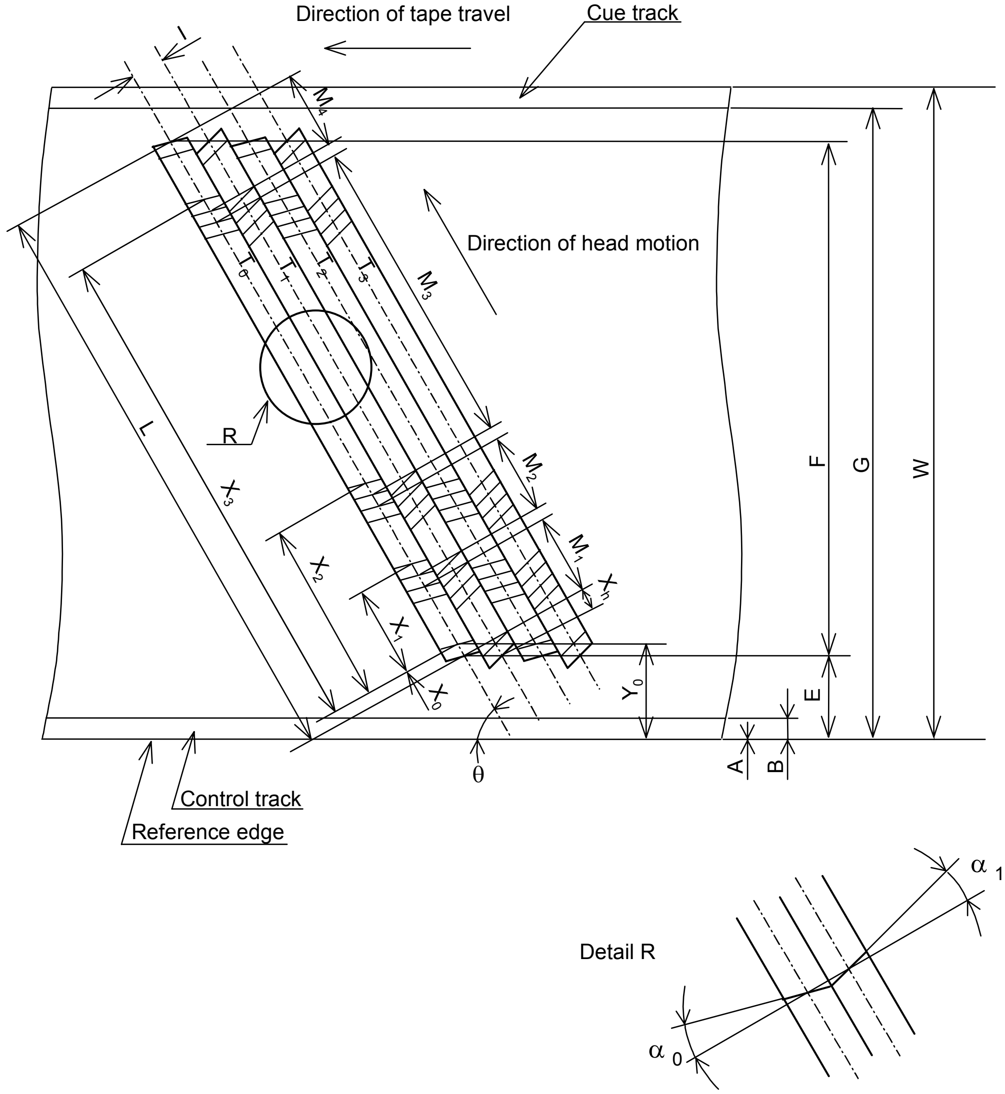


Figure 2 – Locations and dimensions of recorded tracks of 50 Mb/s format

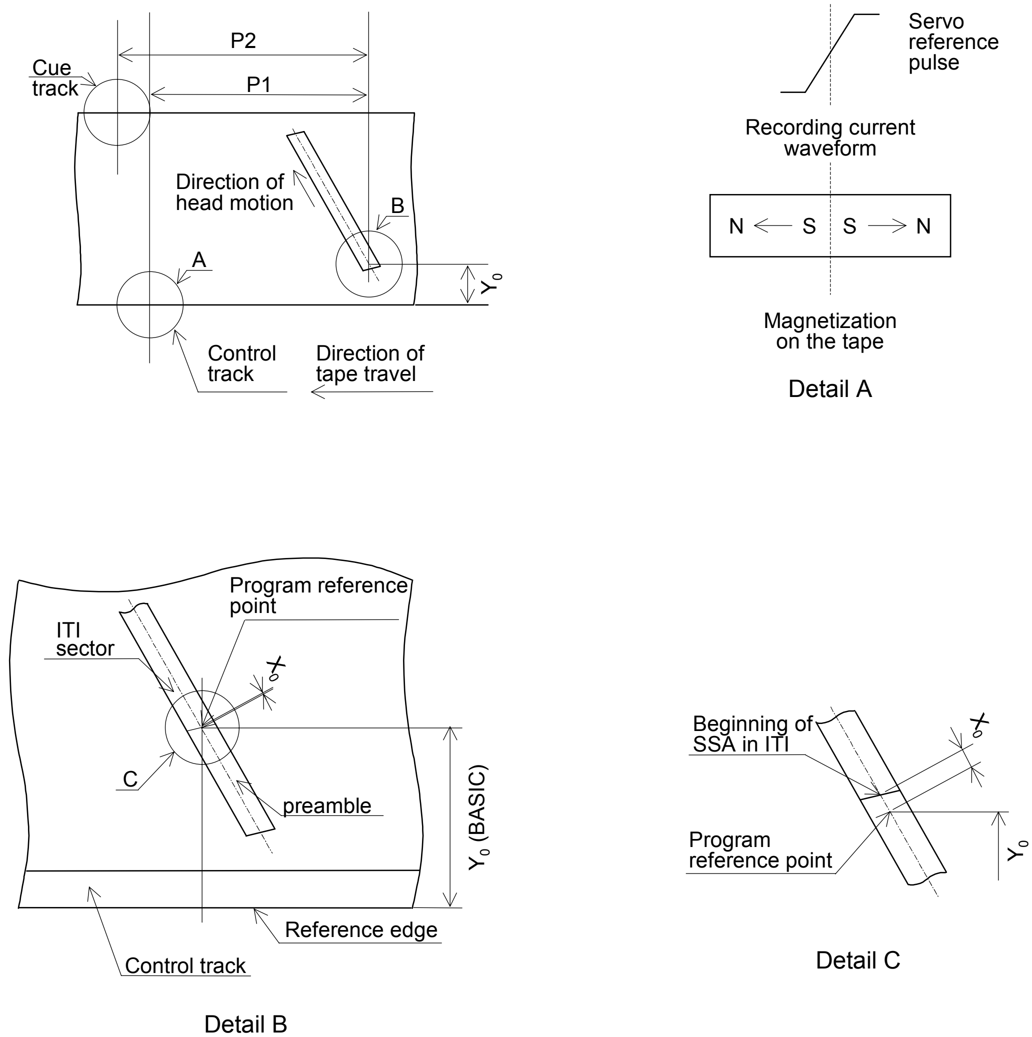


Figure 3 – Location of cue and control track record

Table 1 - Record locations and dimensions (525/60 system of 25 Mb/s format)

Dimensions in millimeters

Dimensions		Nominal	Tolerance
A	Control track lower edge	0	Basic
B	Control track upper edge	0.400	± 0.050
E	Program area lower edge	0.56	Derived
F	Program area width	5.24	Derived
G	Cue track lower edge	6.000	± 0.050
I	Helical track pitch	0.018	Ref.
L	Total length of helical track	32.842	Derived
M_1	Length of ITI sector with preamble and post-amble	0.876	Derived
M_2	Length of audio sector with preamble and post-amble	2.810	Derived
M_3	Length of video sector with preamble and post-amble	27.548	Derived
M_4	Length of subcode sector with preamble and post-amble	0.906	Derived
P_1	Control track reference pulse to program reference point (see figure 3)	67.500	± 0.030
P_2	Cue signal, start of code word of cue to program reference point (see figure 3)	69.900	± 0.300
W	Tape width	6.350	± 0.005
X_0	Location of beginning of SSA in ITI sector	0	± 0.050
X_1	Location of start of audio data sync blocks	0.809	± 0.050
X_2	Location of start of video data sync blocks	3.790	± 0.050
X_3	Location of start of subcode data sync blocks	31.885	± 0.050
Xh	Head stagger and inline tolerance	0.111	± 0.021
Y_0	Program track reference point	0.615	Basic
θ	Track angle	9.1784 °	Basic
α_0	Azimuth angle (track 0)	19.97 °	± 0.150 °
α_1	Azimuth angle (track 1)	20.03 °	± 0.150 °

NOTE – Measurements shall be made under the conditions specified in 3.1. The measurements shall be corrected to account for actual tape speed (see figures C.1 and C.2)

Table 2 - Record locations and dimensions (625/50 system of 25 Mb/s format)

Dimensions in millimeters

Dimensions		Nominal	Tolerance
A	Control track lower edge	0	Basic
B	Control track upper edge	0.400	± 0.050
E	Program area lower edge	0.56	Derived
F	Program area width	5.24	Derived
G	Cue track lower edge	6.000	± 0.050
I	Helical track pitch	0.018	Ref.
L	Total length of helical track	32.842	Derived
M_1	Length of ITI sector with preamble and post-amble	0.877	Derived
M_2	Length of audio sector with preamble and post-amble	2.813	Derived
M_3	Length of video sector with preamble and post-amble	27.576	Derived
M_4	Length of subcode sector with preamble and post-amble	0.877	Derived
P_1	Control track reference pulse to program reference point (see figure 3)	67.500	± 0.030
P_2	Cue signal, start of code word of cue to program reference point (see figure 3)	70.380	± 0.300
W	Tape width	6.350	± 0.005
X_0	Location of beginning of SSA in ITI sector	0	± 0.050
X_1	Location of start of audio data sync blocks	0.810	± 0.050
X_2	Location of start of video data sync blocks	3.793	± 0.050
X_3	Location of start of subcode data sync blocks	31.917	± 0.050
Xh	Head stagger and inline tolerance	0.111	± 0.021
Y_0	Program track reference point	0.615	Basic
θ	Track angle	9.1784 °	Basic
α_0	Azimuth angle (track 0)	19.97 °	± 0.150 °
α_1	Azimuth angle (track 1)	20.03 °	± 0.150 °

NOTE – Measurements shall be made under the conditions specified in 3.1. The measurements shall be corrected to account for actual tape speed (see figure C.1 and C.2).

Table 3 – Record locations and dimensions (525/60 system of 50 Mb/s format)

Dimensions in millimeters

Dimensions		Nominal	Tolerance
A	Control track lower edge	0	Basic
B	Control track upper edge	0.400	± 0.050
E	Program area lower edge	0.56	Derived
F	Program area width	5.24	Derived
G	Cue track lower edge	6.000	± 0.050
I	Helical track pitch	0.018	Ref.
L	Total length of helical track	32.842	Derived
M_1	Length of ITI sector with preamble and post-amble	0.876	Derived
M_2	Length of audio sector with preamble and post-amble	2.810	Derived
M_3	Length of video sector with preamble and post-amble	27.548	Derived
M_4	Length of subcode sector with preamble and post-amble	0.906	Derived
P_1	Control track reference pulse to program reference point (see figure 3)	67.500	± 0.030
P_2	Cue signal, start of code word of cue to program reference point (see figure 3)	67.500	± 0.300
W	Tape width	6.350	± 0.005
X_0	Location of beginning of SSA in ITI sector	0	± 0.050
X_1	Location of start of audio data sync blocks	0.809	± 0.050
X_2	Location of start of video data sync blocks	3.790	± 0.050
X_3	Location of start of subcode data sync blocks	31.885	± 0.050
Xh	Head stagger and inline tolerance	0.111	± 0.021
Y_0	Program track reference point	0.615	Basic
θ	Track angle	9.1784 °	Basic
α_0	Azimuth angle (track 0, 2)	19.97 °	± 0.150 °
α_1	Azimuth angle (track 1, 3)	20.03 °	± 0.150 °

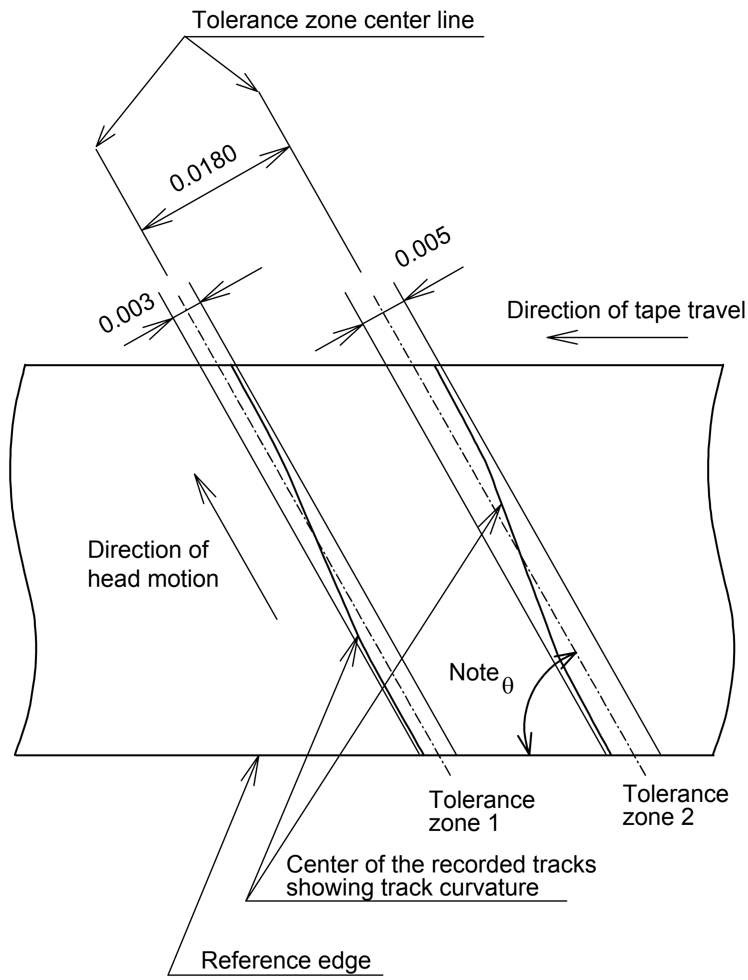
NOTE – Measurements shall be made under the conditions specified in 3.1. The measurements shall be corrected to account for actual tape speed (see figures C.1 and C.3).

Table 4 – Record locations and dimensions (625/50 system of 50 Mb/s format)

Dimensions in millimeters

Dimensions		Nominal	Tolerance
A	Control track lower edge	0	Basic
B	Control track upper edge	0.400	± 0.050
E	Program area lower edge	0.56	Derived
F	Program area width	5.24	Derived
G	Cue track lower edge	6.000	± 0.050
I	Helical track pitch	0.018	Ref.
L	Total length of helical track	32.842	Derived
M_1	Length of ITI sector with preamble and post-amble	0.877	Derived
M_2	Length of audio sector with preamble and post-amble	2.813	Derived
M_3	Length of video sector with preamble and post-amble	27.576	Derived
M_4	Length of subcode sector with preamble and post-amble	0.877	Derived
P_1	Control track reference pulse to program reference point (see figure 3)	67.500	± 0.030
P_2	Cue signal, start of code word of cue to program reference point (see figure 3)	67.500	± 0.300
W	Tape width	6.350	± 0.005
X_0	Location of beginning of SSA in ITI sector	0	± 0.050
X_1	Location of start of audio data sync blocks	0.810	± 0.050
X_2	Location of start of video data sync blocks	3.793	± 0.050
X_3	Location of start of subcode data sync blocks	31.917	± 0.050
Xh	Head stagger and inline tolerance	0.111	± 0.021
Y_0	Program track reference point	0.615	Basic
θ	Track angle	9.1784°	Basic
α_0	Azimuth angle (track 0, 2)	19.97 °	± 0.150 °
α_1	Azimuth angle (track 1, 3)	20.03 °	± 0.150 °

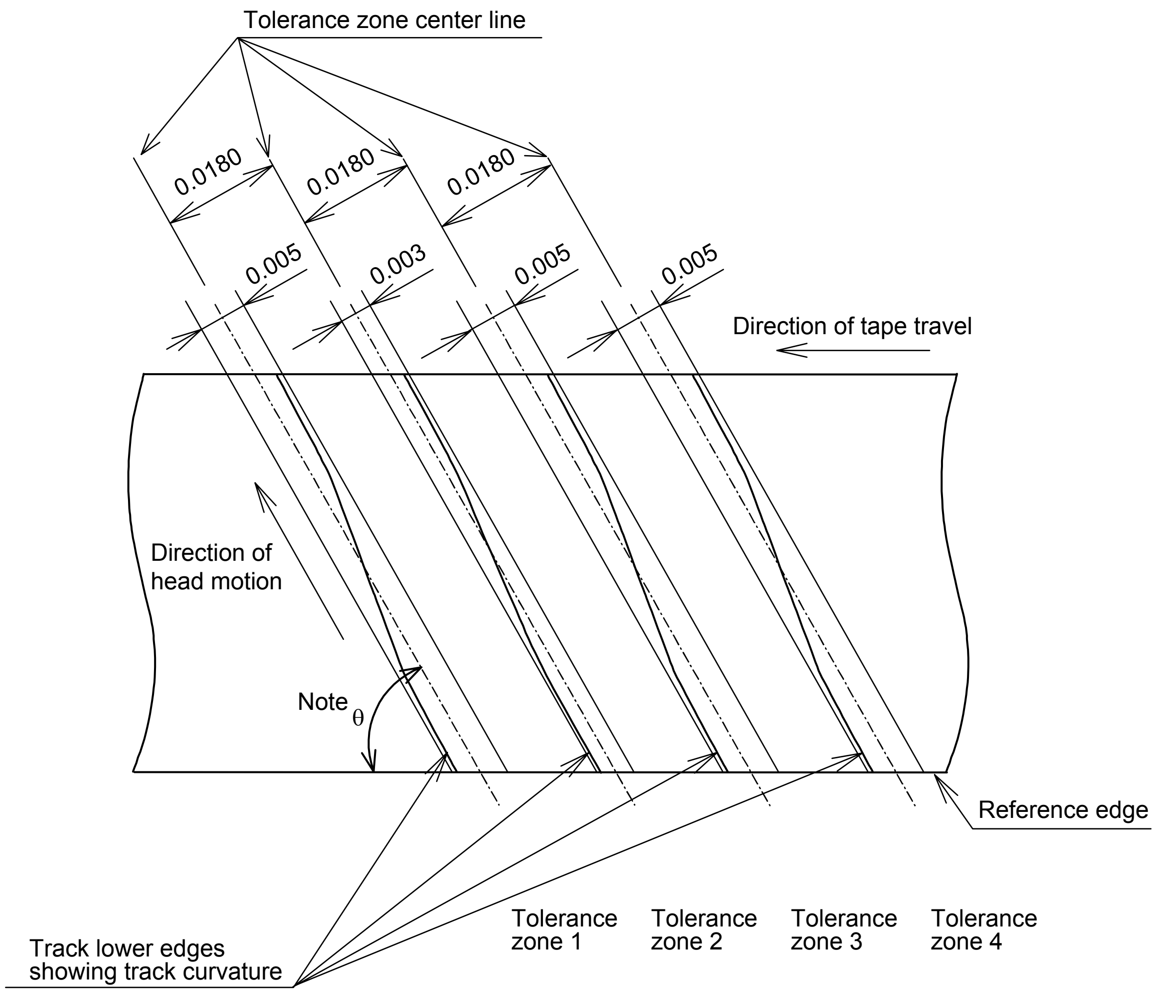
NOTE – Measurements shall be made under the conditions specified in 3.1. The measurements shall be corrected to account for actual tape speed (see figures C.1 and C.3).



Dimensions in millimeters

NOTE - θ = 9.1784 °.

Figure 4 - Locations and dimensions of tolerance zones of helical track record of 25 Mb/s format



Dimensions in millimeters

NOTE - θ = 9.1784 °.

Figure 5 - Locations and dimensions of tolerance zones of helical track record of 50 Mb/s format

5.6 Gap azimuth

5.6.1 Cue and control track

The azimuth angle of the cue and control track head gaps used to produce longitudinal track records shall be perpendicular to these recorded tracks.

5.6.2 Helical track

The azimuth of the head gaps used for the helical track shall be inclined at angles α_0 and α_1 as specified in tables 1 to 4 with respect to a line perpendicular to the helical track. For 25 Mb/s format, the azimuth of track No.0 for every field shall be oriented in a clockwise direction with respect to a line perpendicular to the helical track direction when viewed from the side of the tape containing the magnetic record. For 50 Mb/s format, the azimuth of tracks No.0 and 2 for every field shall be oriented in a clockwise direction in the same manner.

5.7 Transport and scanner

The effective drum diameter, tape tension, helix angle, and tape speed taken together determine the track angle. Different methods of design and/or variations in drum diameter and tape tension can produce equivalent recordings for interchange purposes.

A possible configuration of the transport uses a scanner with an effective diameter of 21.700 mm. Scanner rotation is in the same direction as tape motion during record mode. In 25 Mb/s format, data are recorded by two heads each mounted 180° apart. Figure 6 shows a possible mechanical configuration of the scanner and the relationship between the longitudinal heads and the scanner. Table 5 shows the corresponding mechanical parameters.

In 50 Mb/s format, data are recorded by two pairs of heads each mounted 180° apart. Figure 7 shows a possible mechanical configuration of the scanner and the relationship between the longitudinal heads and the scanner. Table 6 shows the corresponding mechanical parameters.

Other mechanical configurations are allowable provided the same footprint of recorded information is produced on tape.

Table 5 – Parameters for a possible scanner design of 25 Mb/s format

Parameters	525/60 system	625/50 system
Scanner rotation speed (rpm)	9000/1.001	9000
Number of tracks per rotation	2	
Drum diameter (mm)	21.700	
Center span tension (N)	0.09	
Helix angle (degrees)	9.1500	
Effective wrap angle (degrees)	174	
Scanner circumferential speed (m/s)	10.182	10.192
Bit frequency fb (Hz)	41850000	
H1, H2 overwrap head entrance (degrees)	5	
H1, H2 overwrap head exit (degrees)	6	
Maximum tip projection (μm)	20	
Record head track width (μm)	18	

Table 6 – Parameters for a possible scanner design of 50 Mb/s format

Parameters	525/60 system	625/50 system
Scanner rotation speed (rpm)	9000/1.001	9000
Number of tracks per rotation	4	
Drum diameter (mm)	21.700	
Center span tension (N)	0.09	
Helix angle (degrees)	9.1197	
Effective wrap angle (degrees)	174.6	
Scanner circumferential speed (m/s)	10.149	10.159
Bit frequency fb (Hz)	41715000	
H1, H3 overwrap head entrance (degrees)	4.7	
H1, H3 overwrap head exit (degrees)	5.7	
Maximum tip projection (μm)	20	
Record head track width (μm)	18	

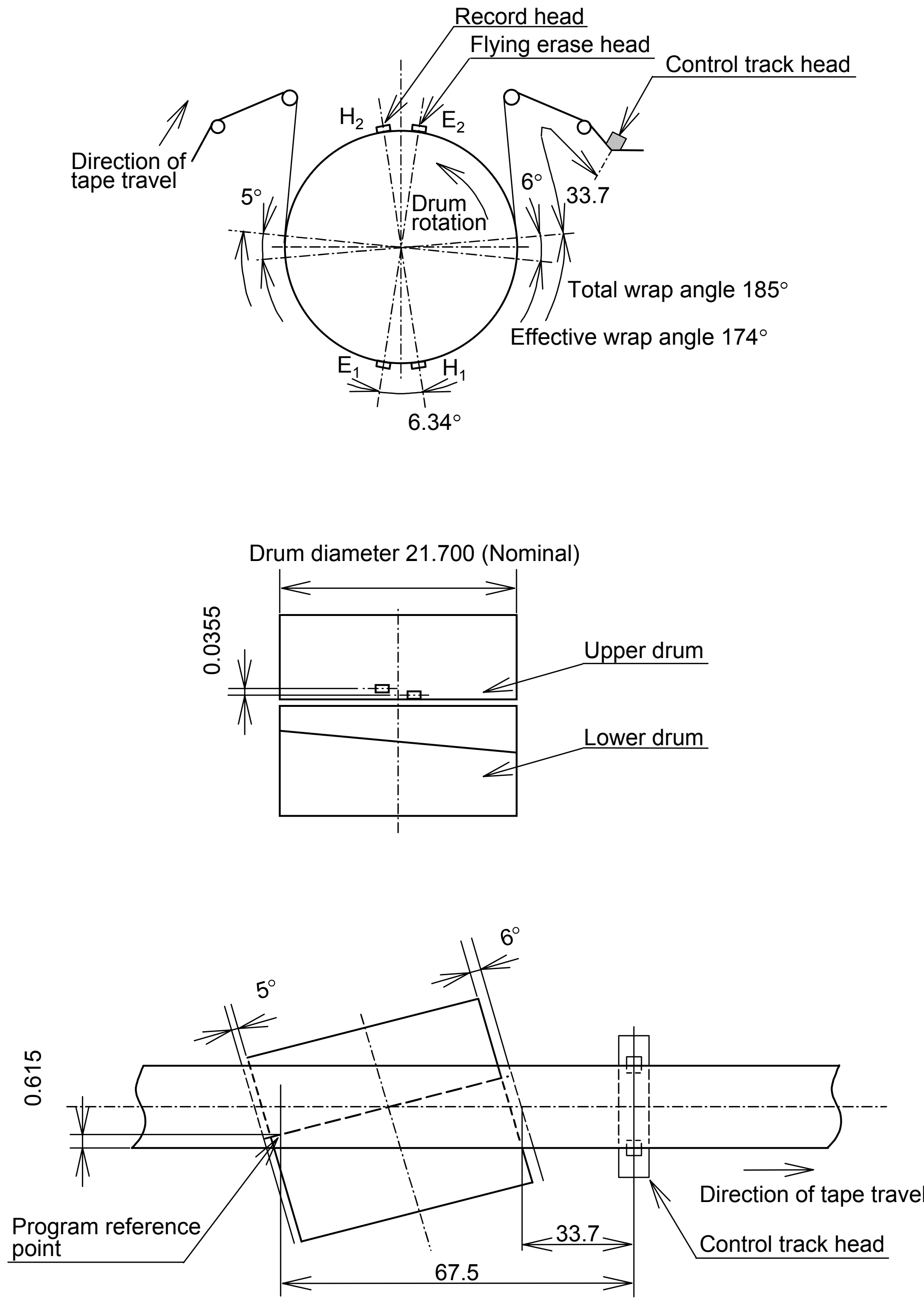
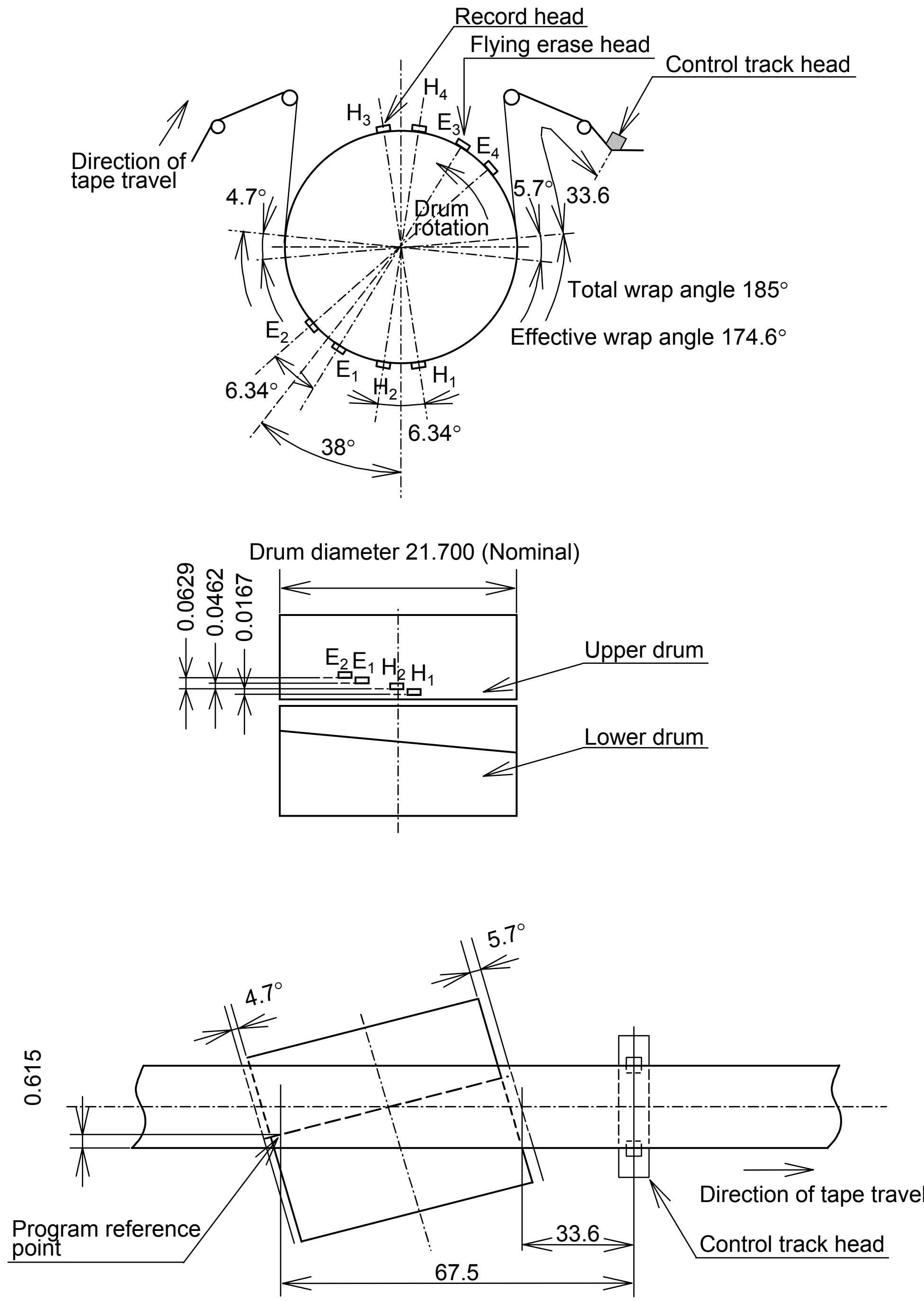


Figure 6 – A possible scanner configuration and tape wrap of 25 Mb/s format



Dimensions in millimeters

Figure 7 – A possible scanner configuration and tape wrap of 50 Mb/s format

6 Program track data

6.1 General

6.1.1 Introduction

For the 25 Mb/s format, each television frame is recorded on 10 tracks for the 525/60 system or 12 tracks for the 625/50 system. For the 50 Mb/s format, each television frame is recorded on 20 tracks for the 525/60 system or 24 tracks for the 625/50 system. The helical tracks contain digital data from the ITI sector, video sector, audio sector, and subcode sector.

The ITI sector contains the start sync and track information. The subcode sector contains the time and control code data and it may also include other optional data.

Figure 8 shows a typical block diagram of the recording circuit. All edit gaps between sectors accommodate timing errors during editing. Figure 9 shows the arrangement of the ITI sector, video and audio sectors, and the subcode sector on the tape.

For the generation of low frequency tracking information, the helical data stream is converted by 24/25 modulation to obtain the following conditions:

- Track F_0: Attenuation of f_1 and f_2 frequency components by at least 9 dB;
- Track F_1: Generation of f_1 component of at least 16 dB, but not more than 19 dB;
- Track F_2: Generation of f_2 component of at least 16 dB, but not more than 19 dB.

where f_1 = fb / 90 (Hz)
f_2 = fb / 60 (Hz)
f_b = Bit frequency : The frequency whose period is a time interval of one channel bit(Hz).

Tracks are recorded in the repeated cycle of F_0 - F_1 - F_0 - F_2 sequence.

In the 525/60 system for the 25 Mb/s format, PF shows the frame information for the second track of each frame. Figures 10 and 11 and tables 7 and 8 show the arrangement of the pilot signals of the 25 Mb/s format. Figures 12 and 13 and tables 9 and 10 show the arrangement of the pilot signals of the 50 Mb/s format. The frequency characteristics and the recorded level of the low frequency pilot signals shall be chosen in accordance with figure 14.

The recommended frequency characteristic of the F_0 track is specified in annex D.

6.1.2 Labeling convention

The most significant bit is written on the left and first recorded to tape. The lowest numbered byte is shown at the left/top and is the first encountered in the input data stream. Byte values are expressed in hexadecimal notation unless otherwise noted. An h subscript indicates a hexadecimal value.

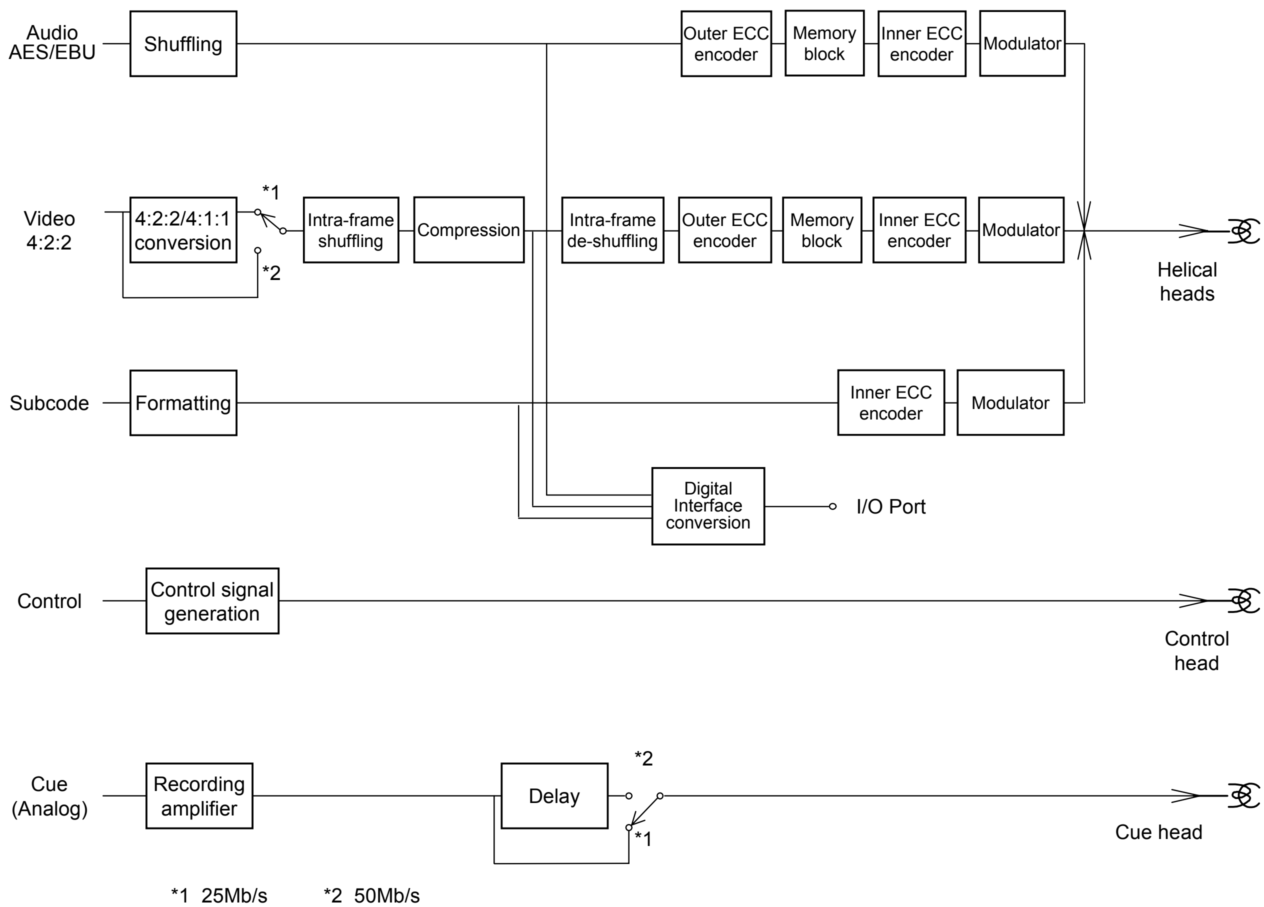


Figure 8 – Possible recording system configuration with digital interface port (informative)

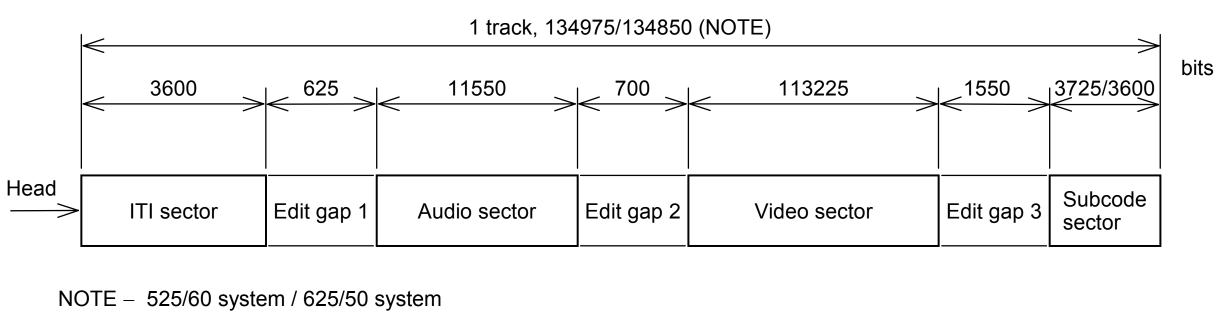


Figure 9 – Sector arrangement on helical track

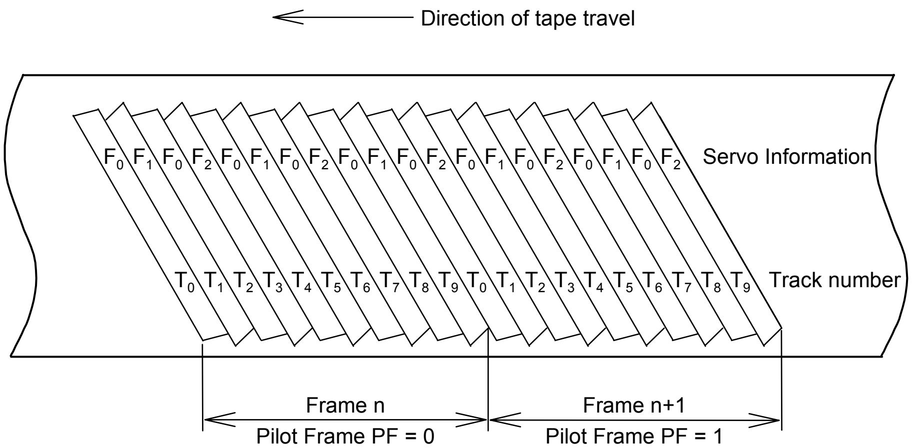


Figure 10 – Frames and tracks (525/60 system of 25 Mb/s format)

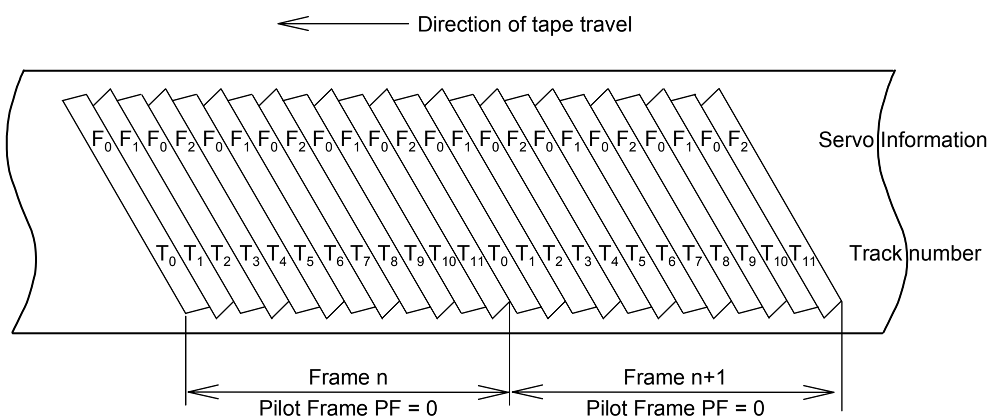


Figure 11 – Frames and tracks (625/50 system of 25 Mb/s format)

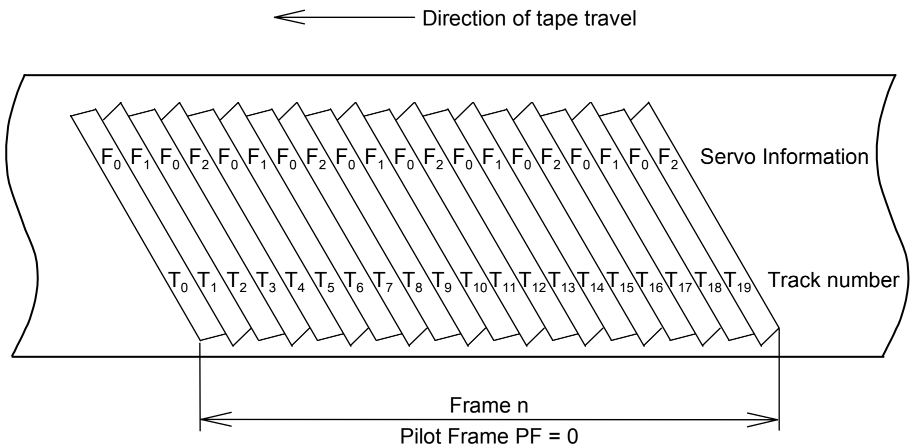


Figure 12 – A frame and tracks (525/60 system of 50 Mb/s format)

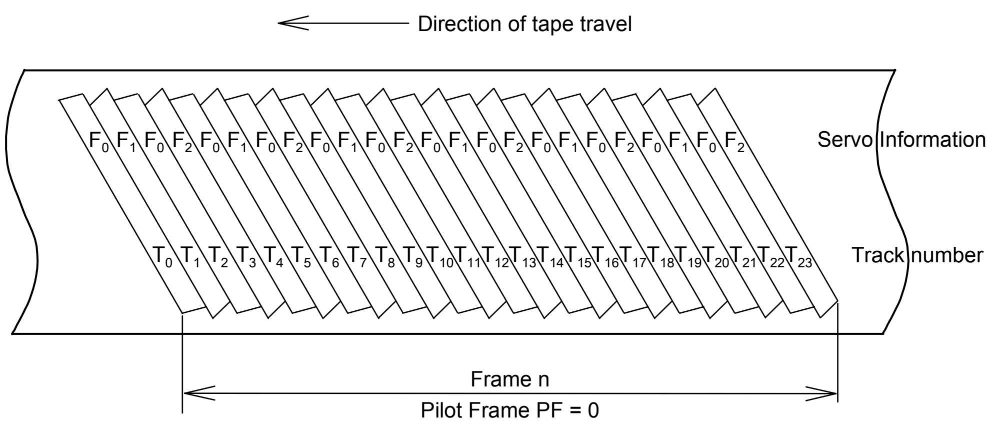


Figure 13 – A frame and tracks (625/50 system of 50 Mb/s format)

Table 7 – Frames and servo information (525/60 system of 25 Mb/s format)

Frame	Track number	Servo information	Pilot frame PF
Frame n	T_0	F_0	0
	T_1	F_1	0
	T_2	F_0	0
	T_3	F_2	0
	T_4	F_0	0
	T_5	F_1	0
	T_6	F_0	0
	T_7	F_2	0
	T_8	F_0	0
	T_9	F_1	0
Frame n+1	T_0	F_0	1
	T_1	F_2	1
	T_2	F_0	1
	T_3	F_1	1
	T_4	F_0	1
	T_5	F_2	1
	T_6	F_0	1
	T_7	F_1	1
	T_8	F_0	1
	T_9	F_2	1

Table 8 – Frames and servo information (625/50 system of 25 Mb/s format)

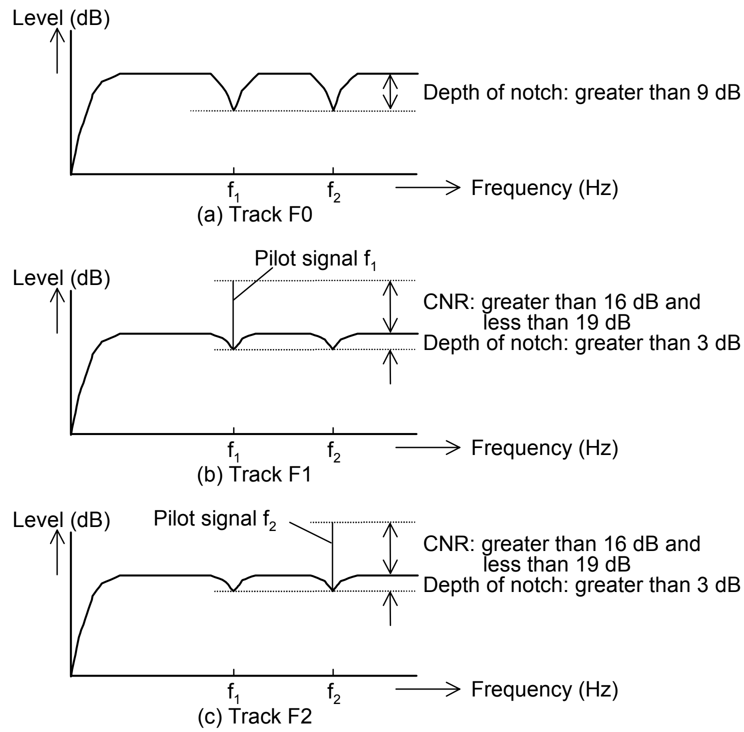
Frame	Track number	Servo information	Pilot frame PF
Frame n	T_0	F_0	0
	T_1	F_1	0
	T_2	F_0	0
	T_3	F_2	0
	T_4	F_0	0
	T_5	F_1	0
	T_6	F_0	0
	T_7	F_2	0
	T_8	F_0	0
	T_9	F_1	0
	T_{10}	F_0	0
	T_{11}	F_2	0
Frame n+1	T_0	F_0	0
	T_1	F_1	0
	T_2	F_0	0
	T_3	F_2	0
	T_4	F_0	0
	T_5	F_1	0
	T_6	F_0	0
	T_7	F_2	0
	T_8	F_0	0
	T_9	F_1	0
	T_{10}	F_0	0
	T_{11}	F_2	0

Table 9 – A frame and servo information (525/60 system of 50 Mb/s format)

Frame	Track number	Servo information	Pilot frame PF
Frame n	T_0	F_0	0
	T_1	F_1	0
	T_2	F_0	0
	T_3	F_2	0
	T_4	F_0	0
	T_5	F_1	0
	T_6	F_0	0
	T_7	F_2	0
	T_8	F_0	0
	T_9	F_1	0
	T_{10}	F_0	0
	T_{11}	F_2	0
	T_{12}	F_0	0
	T_{13}	F_1	0
	T_{14}	F_0	0
	T_{15}	F_2	0
	T_{16}	F_0	0
	T_{17}	F_1	0
	T_{18}	F_0	0
	T_{19}	F_2	0

Table 10 – A frame and servo information (625/50 system of 50 Mb/s format)

Frame	Track number	Servo information	Pilot frame PF
Frame n	T_0	F_0	0
	T_1	F_1	0
	T_2	F_0	0
	T_3	F_2	0
	T_4	F_0	0
	T_5	F_1	0
	T_6	F_0	0
	T_7	F_2	0
	T_8	F_0	0
	T_9	F_1	0
	T_{10}	F_0	0
	T_{11}	F_2	0
	T_{12}	F_0	0
	T_{13}	F_1	0
	T_{14}	F_0	0
	T_{15}	F_2	0
	T_{16}	F_0	0
	T_{17}	F_1	0
	T_{18}	F_0	0
	T_{19}	F_2	0
	T_{20}	F_0	0
	T_{21}	F_1	0
	T_{22}	F_0	0
	T_{23}	F_2	0



NOTES

1 $f_1 = f_b / 90$ (Hz)
$f_2 = f_b / 60$ (Hz)
f_b =The frequency whose period is a time interval of one channel bit(Hz)
Resolution bandwidth $=f_b/20925$(Hz)
Data is obtained by integration over 30 repeated cycles

2 CNR =[S - (N1 + N2) / 2] (dB)
Depth of Notch with peak = [(N1+N2) / 2 - (D1+D2) / 2] (dB)
Depth of Notch without peak = [(N1+N2) / 2 - D] (dB)

N1 is defined as an average value over $f_L \pm f_b / 2000$ (dB)
N2 is defined as an average value over $f_H \pm f_b / 2000$ (dB)
f_L is defined as $f_C - f_b / 400$ (Hz)
f_H is defined as $f_C + f_b / 400$ (Hz)
fc means a peak or notch frequency (Hz)

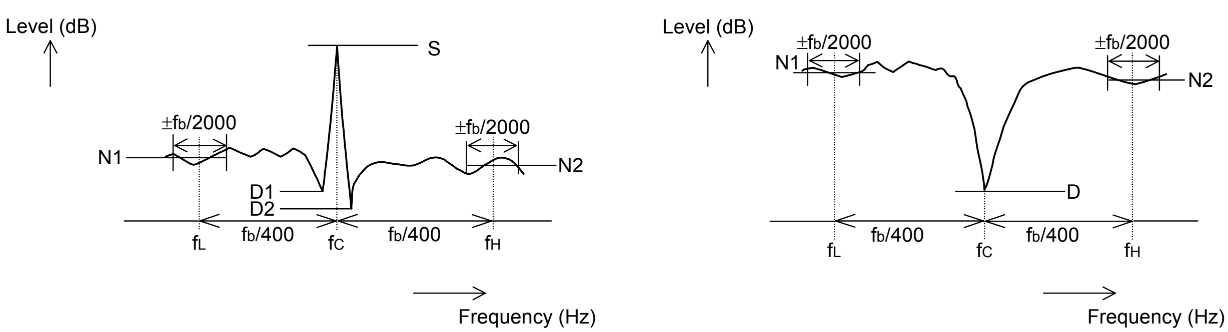


Figure 14 – Frequency characteristics of tracks

6.1.3 Signal processing

Figures 15 to 17 show the processing of modulation related to the recorded signals. The program track data with the exception of ID0 shall be processed through three operations as shown below:

- Randomization;
- 24-25 modulation;
- Pre-coding.

The program track data of ID0 shall be processed through two operations as shown below:

- Randomization;
- Pre-coding.

Figure 18 shows a possible block diagram of the process.

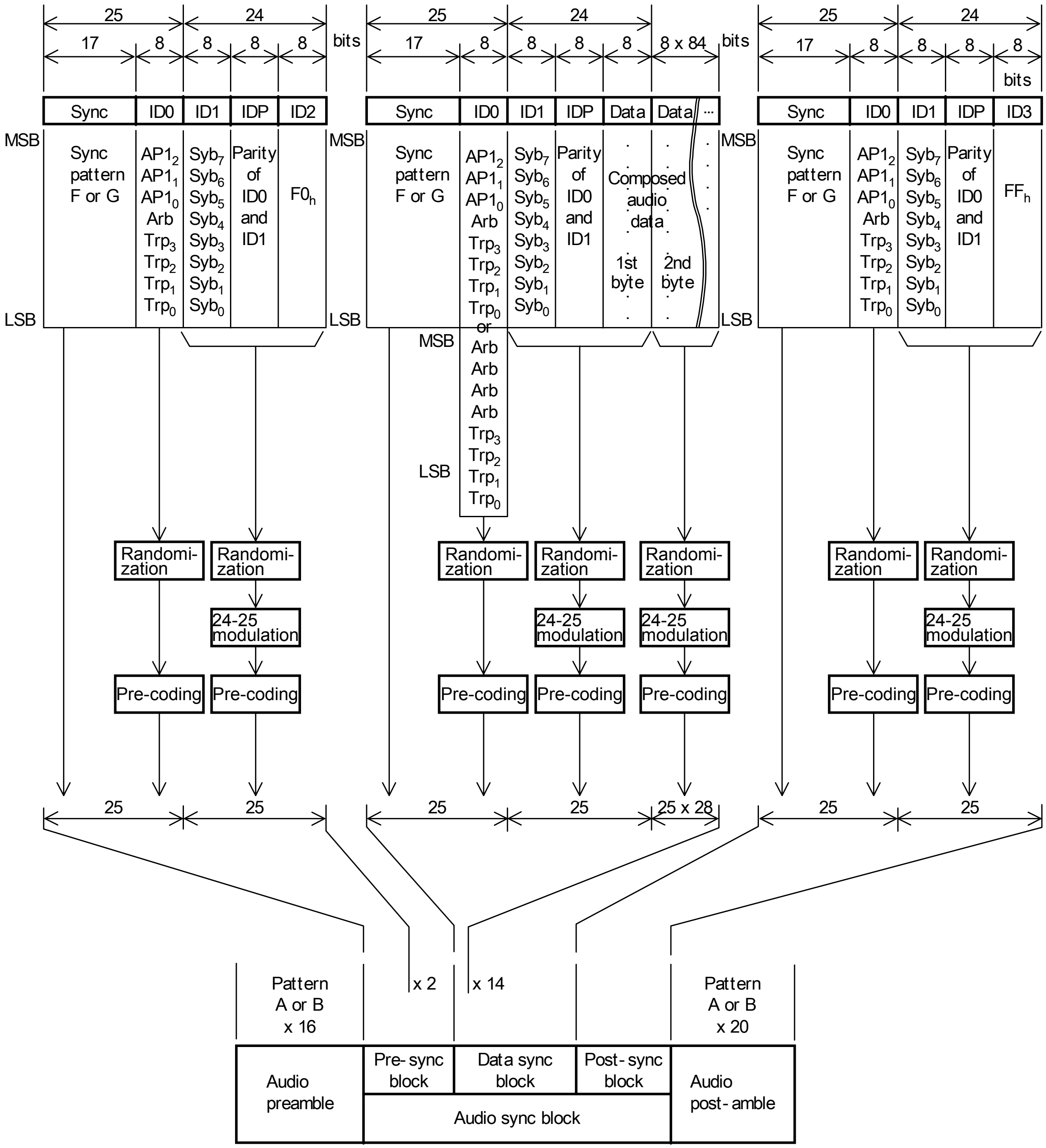


Figure 15 – Modulation for audio sector

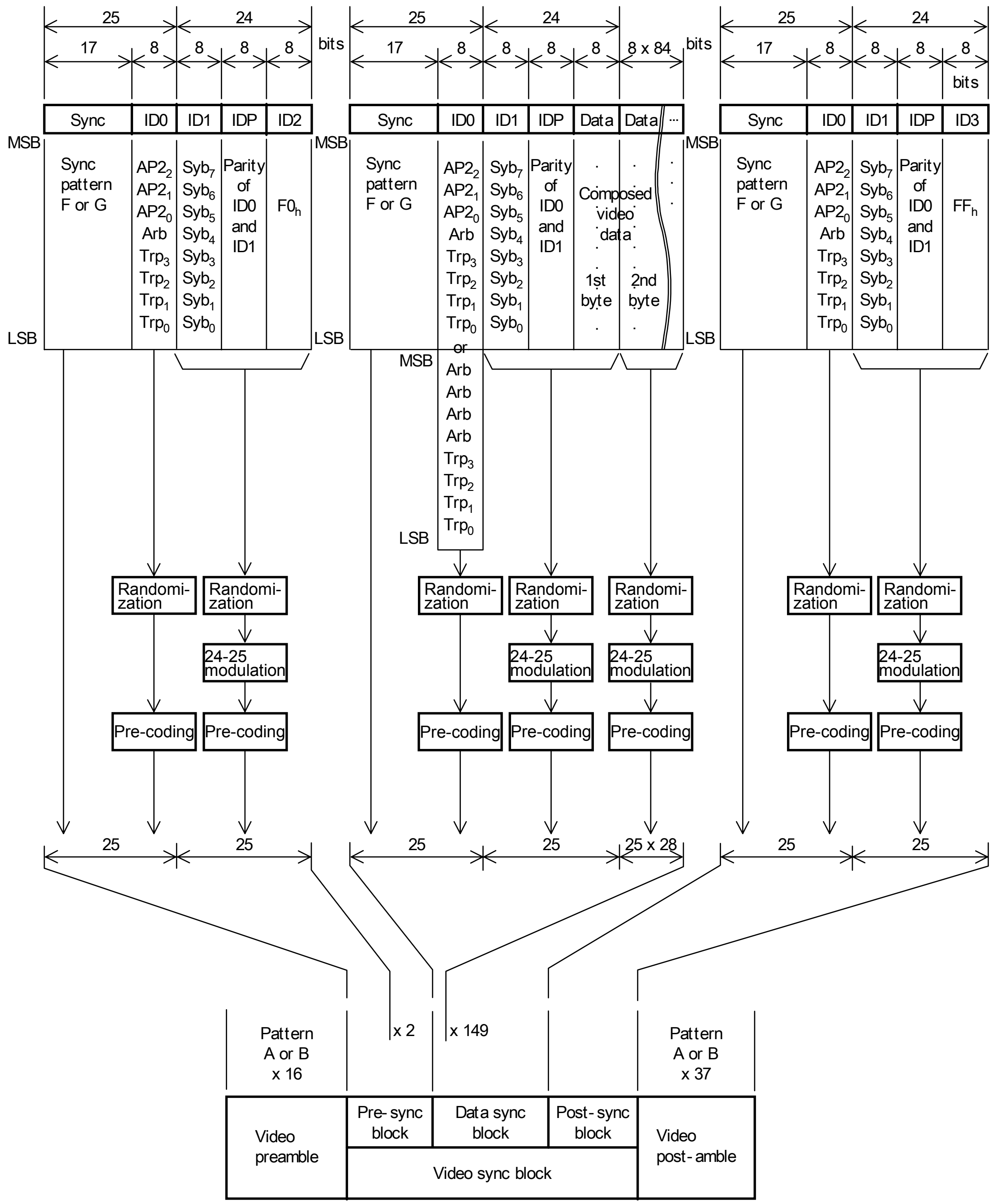


Figure 16 – Modulation for video sector

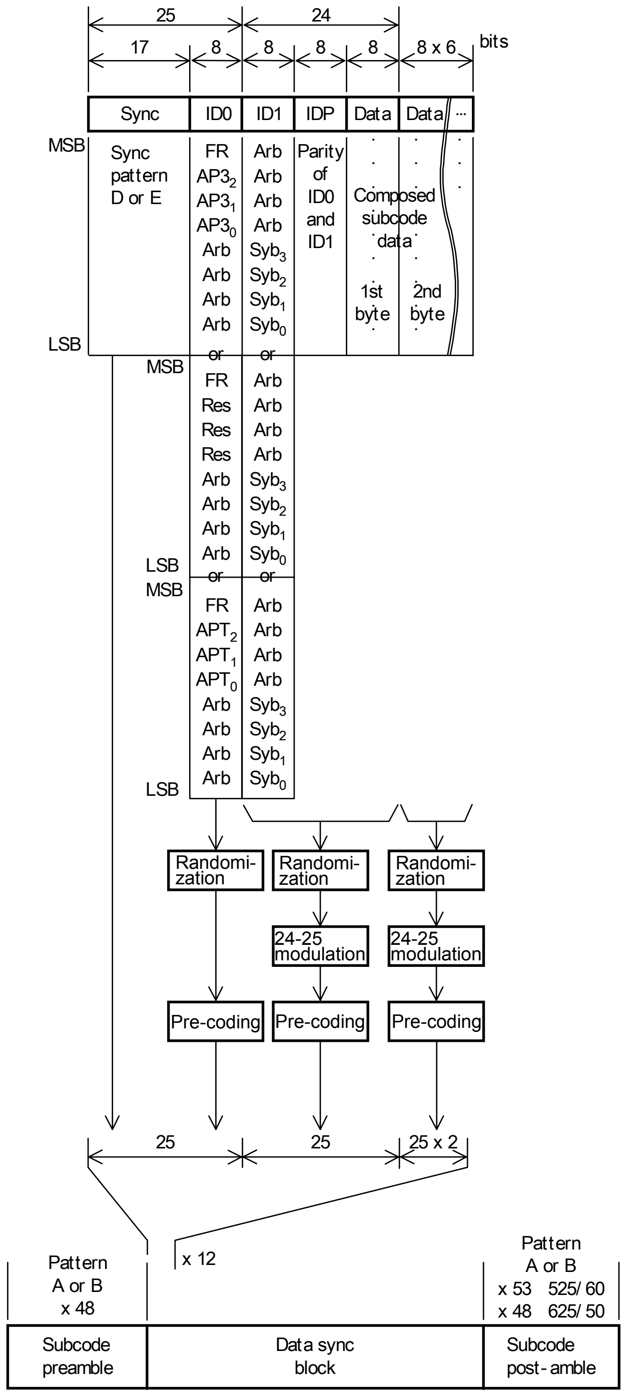


Figure 17 – Modulation for subcode sector

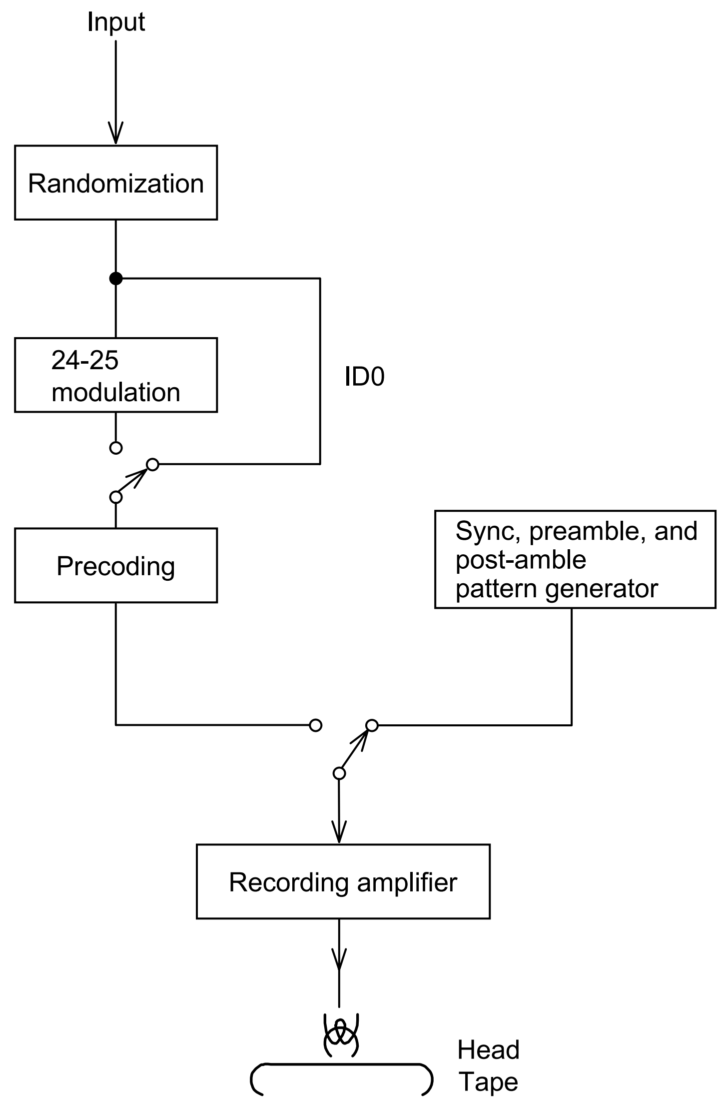


Figure 18 – Possible block diagram for signal processing

6.1.3.1 Randomization

Bit streams of data except sync patterns shall be randomized. The randomizing is equivalent to performing the exclusive-or operation between the serial data stream and the serial stream generated by the polynomial function below:

$$X^7 + X^3 + 1$$

where X^i are place-keeping variables in GF(2), the binary field. The first term is the most significant and the first to enter the division computation. The randomizing is reset at ID0.
The randomization limits the run length of the same binary value.

6.1.3.2 24-25 modulation

The 24-25 modulation is applied to the randomized data bit stream. An extra bit is inserted into the bit stream at the beginning of three consecutive randomized bytes, as shown in figure 19. The modulation output, 25 bits data, is referred to as a code word. The following criteria are used to insert a bit 1 or 0 at the beginning of each three consecutive bytes:

1) If the run length of 1s or 0s, including the extra bit to be inserted at the junction, is shorter than 9, a bit generating the required pilot frequency is inserted.

2) If the run length of 1s or 0s, including the extra bit to be inserted at the junction, exceeds 10, a bit which breaks the run continuation is inserted.

3) Including the extra bit to be inserted at the junction, and the run length of both 1s and 0s exceeds 10, a bit generating the required pilot frequency is inserted.

6.1.3.3 Pre-coding

The modulated bit stream shall be converted to interleaved NRZI as shown in figures 15 to 17 and figure 20.

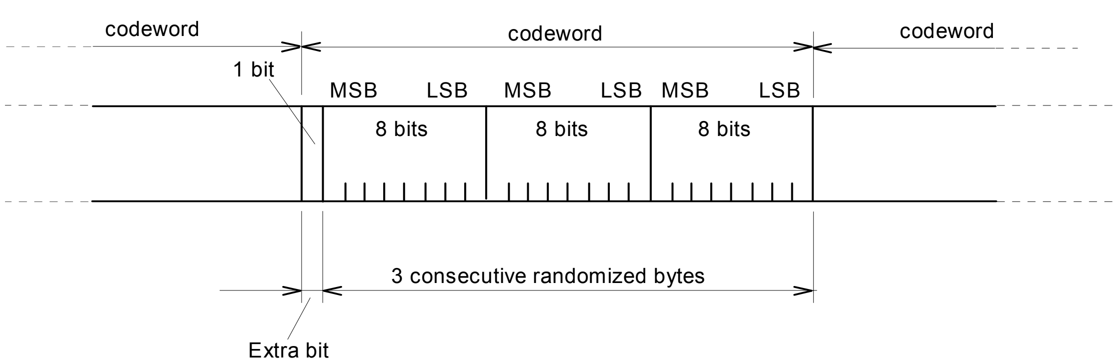


Figure 19 – Bit stream before interleaved NRZI modulation

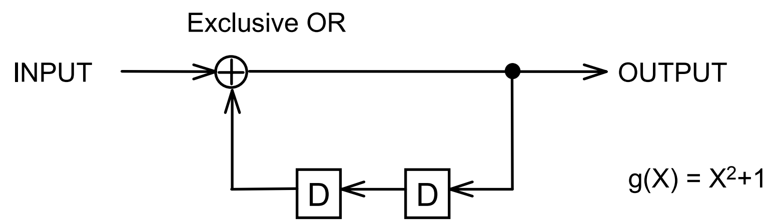


Figure 20 – Pre-coding

6.1.4 Magnetization

6.1.4.1 Polarity

The recorder shall operate in reproduction without regard to the polarity of the recorded flux on the helical tracks.

6.1.4.2 Record equalization

The record current shall generate a record head gap flux level that is constant within ± 1 dB between f_1 and fb/2.

6.1.4.3 Record current level

The optimum record current is 6 dB higher than the lower side of the current value producing 1 dB below the maximum playback output at fb/2.

6.2 Insert and track information (ITI) sector

6.2.1 Structure

The ITI sector is located at the entrance side of each track for accurate placement of the reproducing head. The ITI sector, after initial recording, is not replaced in an editing operation.

The ITI sector contains the following elements:

- ITI preamble;
- Start sync area (SSA);
- Track information area (TIA);
- ITI post-amble.

Figure 21 shows the structure of the ITI sector.

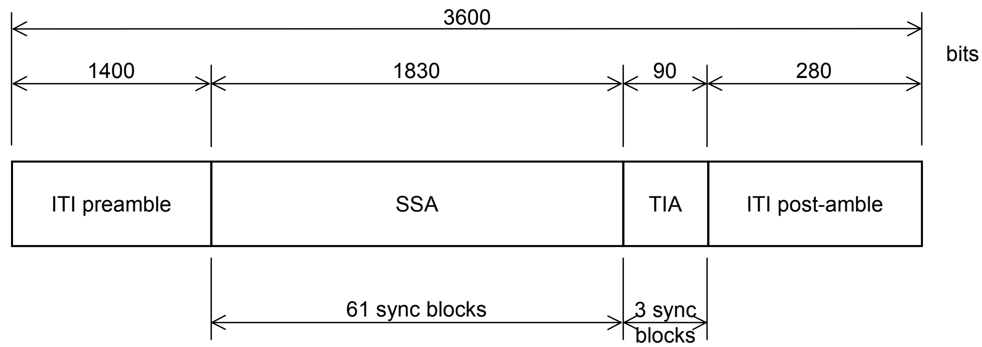
6.2.2 Insert and track information (ITI) preamble

The bit stream of the ITI preamble before the recording shall be defined in tables 11 to 13 in accordance with the low frequency appropriate pilot tone signal for each track. The length of the ITI preamble shall be 1400 bits as recorded on tape.

6.2.3 Start Sync Area (SSA)

SSA consists of 61 sync blocks and each sync block consists of 30 bits. Every start-sync block has a number which indicates the position of the sync block from the beginning of the SSA from zero.

The bit stream of the SSA after the modulation shall be as defined in tables 14 to 16 in accordance with the low frequency pilot signals. The length of the SSA shall be 1830 bits as recorded on tape.



NOTE – Each sync block has 30 bits.

Figure 21 - Structure of ITI sector

Table 11 – Bit stream of ITI preamble for servo information F_0

Order of recording	Codeword MSB LSB	Order of recording	Codeword MSB LSB	Order of recording	Codeword MSB LSB	Order of recording	Codeword MSB LSB
0	1000101110	40	1000101110	80	1000101110	120	1000101110
1	1000101110	41	1000101110	81	1000101110	121	1000101110
2	1000101110	42	1000101110	82	1000101110	122	1000101110
3	1000101110	43	1000101110	83	1000101110	123	1000101110
4	1000101110	44	1000101110	84	1000101110	124	1000101110
5	1000101110	45	1000101110	85	1000101110	125	1000101110
6	1000101110	46	1000101110	86	1000101110	126	1000101110
7	1000101110	47	1000101110	87	1000101110	127	1000101110
8	1000101110	48	1000101110	88	1000101110	128	1000101110
9	1000101110	49	1000101110	89	1000101110	129	1000101110
10	1000101110	50	1000101110	90	1000101110	130	1000101110
11	1000101110	51	1000101110	91	1000101110	131	1000101110
12	1000101110	52	1000101110	92	1000101110	132	1000101110
13	1000101110	53	1000101110	93	1000101110	133	1000101110
14	1000101110	54	1000101110	94	1000101110	134	1000101110
15	1000101110	55	1000101110	95	1000101110	135	1000101110
16	1000101110	56	1000101110	96	1000101110	136	1000101110
17	1000101110	57	1000101110	97	1000101110	137	1000101110
18	1000101110	58	1000101110	98	1000101110	138	1000101110
19	1000101110	59	1000101110	99	1000101110	139	1000101110
20	1000101110	60	1000101110	100	1000101110		
21	1000101110	61	1000101110	101	1000101110		
22	1000101110	62	1000101110	102	1000101110		
23	1000101110	63	1000101110	103	1000101110		
24	1000101110	64	1000101110	104	1000101110		
25	1000101110	65	1000101110	105	1000101110		
26	1000101110	66	1000101110	106	1000101110		
27	1000101110	67	1000101110	107	1000101110		
28	1000101110	68	1000101110	108	1000101110		
29	1000101110	69	1000101110	109	1000101110		
30	1000101110	70	1000101110	110	1000101110		
31	1000101110	71	1000101110	111	1000101110		
32	1000101110	72	1000101110	112	1000101110		
33	1000101110	73	1000101110	113	1000101110		
34	1000101110	74	1000101110	114	1000101110		
35	1000101110	75	1000101110	115	1000101110		
36	1000101110	76	1000101110	116	1000101110		
37	1000101110	77	1000101110	117	1000101110		
38	1000101110	78	1000101110	118	1000101110		
39	1000101110	79	1000101110	119	1000101110		

Table 12 – Bit stream of ITI preamble for servo information F_1

Order of recording	Codeword MSB LSB	Order of recording	Codeword MSB LSB	Order of recording	Codeword MSB LSB	Order of recording	Codeword MSB LSB
0	1101110001	40	1000101110	80	0010001110	120	1101110001
1	1101110001	41	0010001110	81	1101110001	121	1000101110
2	1101110001	42	0010001110	82	1101110001	122	0010001110
3	1101110001	43	0010001110	83	1101110001	123	0010001110
4	1000101110	44	0010001110	84	1101110001	124	0010001110
5	0010001110	45	1101110001	85	1000101110	125	0010001110
6	0010001110	46	1101110001	86	0010001110	126	1101110001
7	0010001110	47	1101110001	87	0010001110	127	1101110001
8	0010001110	48	1101110001	88	0010001110	128	1101110001
9	1101110001	49	1000101110	89	0010001110	129	1101110001
10	1101110001	50	0010001110	90	1101110001	130	1000101110
11	1101110001	51	0010001110	91	1101110001	131	0010001110
12	1101110001	52	0010001110	92	1101110001	132	0010001110
13	1000101110	53	0010001110	93	1101110001	133	0010001110
14	0010001110	54	1101110001	94	1000101110	134	0010001110
15	0010001110	55	1101110001	95	0010001110	135	1101110001
16	0010001110	56	1101110001	96	0010001110	136	1101110001
17	0010001110	57	1101110001	97	0010001110	137	1101110001
18	1101110001	58	1000101110	98	0010001110	138	1101110001
19	1101110001	59	0010001110	99	1101110001	139	1000101110
20	1101110001	60	0010001110	100	1101110001		
21	1101110001	61	0010001110	101	1101110001		
22	1000101110	62	0010001110	102	1101110001		
23	0010001110	63	1101110001	103	1000101110		
24	0010001110	64	1101110001	104	0010001110		
25	0010001110	65	1101110001	105	0010001110		
26	0010001110	66	1101110001	106	0010001110		
27	1101110001	67	1000101110	107	0010001110		
28	1101110001	68	0010001110	108	1101110001		
29	1101110001	69	0010001110	109	1101110001		
30	1101110001	70	0010001110	110	1101110001		
31	1000101110	71	0010001110	111	1101110001		
32	0010001110	72	1101110001	112	1000101110		
33	0010001110	73	1101110001	113	0010001110		
34	0010001110	74	1101110001	114	0010001110		
35	0010001110	75	1101110001	115	0010001110		
36	1101110001	76	1000101110	116	0010001110		
37	1101110001	77	0010001110	117	1101110001		
38	1101110001	78	0010001110	118	1101110001		
39	1101110001	79	0010001110	119	1101110001		

Table 13 – Bit stream of ITI preamble for servo information F_2

Order of recording	Codeword MSB LSB	Order of recording	Codeword MSB LSB	Order of recording	Codeword MSB LSB	Order of recording	Codeword MSB LSB
0	1101110001	40	0010001110	80	1101110001	120	1101110001
1	1101110001	41	0010001110	81	0010001110	121	1101110001
2	1101110001	42	1101110001	82	0010001110	122	1101110001
3	0010001110	43	1101110001	83	0010001110	123	0010001110
4	0010001110	44	1101110001	84	1101110001	124	0010001110
5	0010001110	45	0010001110	85	1101110001	125	0010001110
6	1101110001	46	0010001110	86	1101110001	126	1101110001
7	1101110001	47	0010001110	87	0010001110	127	1101110001
8	1101110001	48	1101110001	88	0010001110	128	1101110001
9	0010001110	49	1101110001	89	0010001110	129	0010001110
10	0010001110	50	1101110001	90	1101110001	130	0010001110
11	0010001110	51	0010001110	91	1101110001	131	0010001110
12	1101110001	52	0010001110	92	1101110001	132	1101110001
13	1101110001	53	0010001110	93	0010001110	133	1101110001
14	1101110001	54	1101110001	94	0010001110	134	1101110001
15	0010001110	55	1101110001	95	0010001110	135	0010001110
16	0010001110	56	1101110001	96	1101110001	136	0010001110
17	0010001110	57	0010001110	97	1101110001	137	0010001110
18	1101110001	58	0010001110	98	1101110001	138	1101110001
19	1101110001	59	0010001110	99	0010001110	139	1101110001
20	1101110001	60	1101110001	100	0010001110		
21	0010001110	61	1101110001	101	0010001110		
22	0010001110	62	1101110001	102	1101110001		
23	0010001110	63	0010001110	103	1101110001		
24	1101110001	64	0010001110	104	1101110001		
25	1101110001	65	0010001110	105	0010001110		
26	1101110001	66	1101110001	106	0010001110		
27	0010001110	67	1101110001	107	0010001110		
28	0010001110	68	1101110001	108	1101110001		
29	0010001110	69	0010001110	109	1101110001		
30	1101110001	70	0010001110	110	1101110001		
31	1101110001	71	0010001110	111	0010001110		
32	1101110001	72	1101110001	112	0010001110		
33	0010001110	73	1101110001	113	0010001110		
34	0010001110	74	1101110001	114	1101110001		
35	0010001110	75	0010001110	115	1101110001		
36	1101110001	76	0010001110	116	1101110001		
37	1101110001	77	0010001110	117	0010001110		
38	1101110001	78	1101110001	118	0010001110		
39	0010001110	79	1101110001	119	0010001110		

Table 14 – Bit stream of SSA for servo information F_0

Order of recording	Codeword MSB LSB	Order of recording	Codeword MSB LSB	Order of recording	Codeword MSB LSB	Order of recording	Codeword MSB LSB
0	0010011101	50	0101010101	100	0110101001	150	0010011101
1	0101010101	51	0010011101	101	0101011001	151	0110010101
2	0101010101	52	0101101001	102	0010011101	152	0101101001
3	0010011101	53	0101011001	103	0110101001	153	0010011101
4	0101010101	54	0010011101	104	0101101001	154	0110010101
5	0101011001	55	0101101001	105	0010011101	155	0101100101
6	0010011101	56	0101101001	106	0110101001	156	0010011101
7	0101010101	57	0010011101	107	0101100101	157	0110010101
8	0101101001	58	0101101001	108	0010011101	158	0110101001
9	0010011101	59	0101100101	109	0110101001	159	0010011101
10	0101010101	60	0010011101	110	0110101001	160	0110010101
11	0101100101	61	0101101001	111	0010011101	161	0110100101
12	0010011101	62	0110101001	112	0110101001	162	0010011101
13	0101010101	63	0010011101	113	0110100101	163	0110010101
14	0110101001	64	0101101001	114	0010011101	164	0110010101
15	0010011101	65	0110100101	115	0110101001	165	0010011101
16	0101010101	66	0010011101	116	0110010101	166	0110010101
17	0110100101	67	0101101001	117	0010011101	167	0110011001
18	0010011101	68	0110010101	118	0110101001	168	0010011101
19	0101010101	69	0010011101	119	0110011001	169	0110011001
20	0110010101	70	0101101001	120	0010011101	170	0101010101
21	0010011101	71	0110011001	121	0110100101	171	0010011101
22	0101010101	72	0010011101	122	0101010101	172	0110011001
23	0110011001	73	0101100101	123	0010011101	173	0101011001
24	0010011101	74	0101010101	124	0110100101	174	0010011101
25	0101011001	75	0010011101	125	0101011001	175	0110011001
26	0101010101	76	0101100101	126	0010011101	176	0101101001
27	0010011101	77	0101011001	127	0110100101	177	0010011101
28	0101011001	78	0010011101	128	0101101001	178	0110011001
29	0101011001	79	0101100101	129	0010011101	179	0101100101
30	0010011101	80	0101101001	130	0110100101	180	0010011101
31	0101011001	81	0010011101	131	0101100101	181	0110011001
32	0101101001	82	0101100101	132	0010011101	182	0110101001
33	0010011101	83	0101100101	133	0110100101		
34	0101011001	84	0010011101	134	0110101001		
35	0101100101	85	0101100101	135	0010011101		
36	0010011101	86	0110101001	136	0110100101		
37	0101011001	87	0010011101	137	0110100101		
38	0110101001	88	0101100101	138	0010011101		
39	0010011101	89	0110100101	139	0110100101		
40	0101011001	90	0010011101	140	0110010101		
41	0110100101	91	0101100101	141	0010011101		
42	0010011101	92	0110010101	142	0110100101		
43	0101011001	93	0010011101	143	0110011001		
44	0110010101	94	0101100101	144	0010011101		
45	0010011101	95	0110011001	145	0110010101		
46	0101011001	96	0010011101	146	0101010101		
47	0110011001	97	0110101001	147	0010011101		
48	0010011101	98	0101010101	148	0110010101		
49	0101101001	99	0010011101	149	0101011001		

Table 15 – Bit stream of SSA for servo information F_1

Order of recording	Codeword MSB LSB	Order of recording	Codeword MSB LSB	Order of recording	Codeword MSB LSB	Order of recording	Codeword MSB LSB
0	0111001000	50	0101010111	100	1001010100	150	1000110111
1	1010101000	51	1000110111	101	1010100100	151	0110010111
2	1010101000	52	0101101011	102	0111001000	152	0101101001
3	0111001000	53	0101011001	103	0110101011	153	0111001000
4	0101010111	54	0111001000	104	0101101011	154	1001101000
5	0101011011	55	1010010100	105	1000110111	155	1010011000
6	1000110111	56	1010010100	106	0110101011	156	0111001000
7	0101010111	57	0111001000	107	0101100101	157	0110010111
8	0101101001	58	0101101011	108	0111001000	158	0110101011
9	0111001000	59	0101100111	109	1001010100	159	1000110111
10	1010101000	60	1000110111	110	1001010100	160	0110010111
11	1010011000	61	0101101011	111	0111001000	161	0110100101
12	0111001000	62	0110101001	112	0110101011	162	0111001000
13	0101010111	63	0111001000	113	0110100111	163	1001101000
14	0110101011	64	1010010100	114	1000110111	164	1001101000
15	1000110111	65	1001011000	115	0110101011	165	0111001000
16	0101010111	66	0111001000	116	0110010101	166	0110010111
17	0110100101	67	0101101011	117	0111001000	167	0110011011
18	0111001000	68	0110010111	118	1001010100	168	1000110111
19	1010101000	69	1000110111	119	1001100100	169	0110011011
20	1001101000	70	0101101011	120	0111001000	170	0101010101
21	0111001000	71	0110011001	121	0110100111	171	0111001000
22	0101010111	72	0111001000	122	0101010111	172	1001100100
23	0110011011	73	1010011000	123	1000110111	173	1010100100
24	1000110111	74	1010101000	124	0110100111	174	0111001000
25	0101011011	75	0111001000	125	0101011001	175	0110011011
26	0101010101	76	0101100111	126	0111001000	176	0101101011
27	0111001000	77	0101011011	127	1001011000	177	1000110111
28	1010100100	78	1000110111	128	1010010100	178	0110011011
29	1010100100	79	0101100111	129	0111001000	179	0101100101
30	0111001000	80	0101101001	130	0110100111	180	0111001000
31	0101011011	81	0111001000	131	0101100111	181	1001100100
32	0101101011	82	1010011000	132	1000110111	182	1001010100
33	1000110111	83	1010011000	133	0110100111		
34	0101011011	84	0111001000	134	0110101001		
35	0101100101	85	0101100111	135	0111001000		
36	0111001000	86	0110101011	136	1001011000		
37	1010100100	87	1000110111	137	1001011000		
38	1001010100	88	0101100111	138	0111001000		
39	0111001000	89	0110100101	139	0110100111		
40	0101011011	90	0111001000	140	0110010111		
41	0110100111	91	1010011000	141	1000110111		
42	1000110111	92	1001101000	142	0110100111		
43	0101011011	93	0111001000	143	0110011001		
44	0110010101	94	0101100111	144	0111001000		
45	0111001000	95	0110011011	145	1001101000		
46	1010100100	96	1000110111	146	1010101000		
47	1001100100	97	0110101011	147	0111001000		
48	0111001000	98	0101010101	148	0110010111		
49	0101101011	99	0111001000	149	0101011011		

Table 16 – Bit stream of SSA for servo information F_2

Order of recording	Codeword MSB LSB	Order of recording	Codeword MSB LSB	Order of recording	Codeword MSB LSB	Order of recording	Codeword MSB LSB
0	1000110111	50	1010101000	100	0110101011	150	1000110111
1	1010101000	51	0111001000	101	0101011011	151	1001101000
2	1010101000	52	0101101011	102	1000110111	152	1010010100
3	0111001000	53	0101011011	103	1001010100	153	0111001000
4	0101010111	54	1000110111	104	1010010100	154	0110010111
5	0101011011	55	1010010100	105	0111001000	155	0101100111
6	1000110111	56	1010010100	106	0110101011	156	1000110111
7	1010101000	57	0111001000	107	0101100111	157	1001101000
8	1010010100	58	0101101011	108	1000110111	158	1001010100
9	0111001000	59	0101100111	109	1001010100	159	0111001000
10	0101010111	60	1000110111	110	1001010100	160	0110010111
11	0101100111	61	1010010100	111	0111001000	161	0110100111
12	1000110111	62	1001010100	112	0110101011	162	1000110111
13	1010101000	63	0111001000	113	0110100111	163	1001101000
14	1001010100	64	0101101011	114	1000110111	164	1001101000
15	0111001000	65	0110100111	115	1001010100	165	0111001000
16	0101010111	66	1000110111	116	1001101000	166	0110010111
17	0110100111	67	1010010100	117	0111001000	167	0110011011
18	1000110111	68	1001101000	118	0110101011	168	1000110111
19	1010101000	69	0111001000	119	0110011011	169	1001100100
20	1001101000	70	0101101011	120	1000110111	170	1010101000
21	0111001000	71	0110011011	121	1001011000	171	0111001000
22	0101010111	72	1000110111	122	1010101000	172	0110011011
23	0110011011	73	1010011000	123	0111001000	173	0101011011
24	1000110111	74	1010101000	124	0110100111	174	1000110111
25	1010100100	75	0111001000	125	0101011011	175	1001100100
26	1010101000	76	0101100111	126	1000110111	176	1010010100
27	0111001000	77	0101011011	127	1001011000	177	0111001000
28	0101011011	78	1000110111	128	1010010100	178	0110011011
29	0101011011	79	1010011000	129	0111001000	179	0101100111
30	1000110111	80	1010010100	130	0110100111	180	1000110111
31	1010100100	81	0111001000	131	0101100111	181	1001100100
32	1010010100	82	0101100111	132	1000110111	182	1001010100
33	0111001000	83	0101100111	133	1001011000		
34	0101011011	84	1000110111	134	1001010100		
35	0101100111	85	1010011000	135	0111001000		
36	1000110111	86	1001010100	136	0110100111		
37	1010100100	87	0111001000	137	0110100111		
38	1001010100	88	0101100111	138	1000110111		
39	0111001000	89	0110100111	139	1001011000		
40	0101011011	90	1000110111	140	1001101000		
41	0110100111	91	1010011000	141	0111001000		
42	1000110111	92	1001101000	142	0110100111		
43	1010100100	93	0111001000	143	0110011011		
44	1001101000	94	0101100111	144	1000110111		
45	0111001000	95	0110011011	145	1001101000		
46	0101011011	96	1000110111	146	1010101000		
47	0110011011	97	1001010100	147	0111001000		
48	1000110111	98	1010101000	148	0110010111		
49	1010010100	99	0111001000	149	0101011011		

6.2.4 Track information area (TIA)

Track information area (TIA) consists of three sync blocks. Each sync block consists of 30 bits as shown in figure 22. Every sync block has the same track information. Before the randomization, application ID of the track information shall be defined as in table 17. The pilot frame shall be assigned as in table 18.

Before the recording, the bit stream of the TIA shall be as defined in tables 19 to 21 in accordance with the low frequency pilot signals. The length of the TIA shall be 90 bits as recorded on tape.

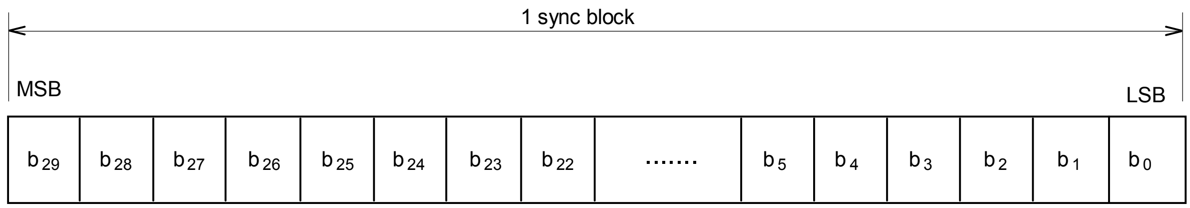


Figure 22 – Structure of sync block of TIA

Table 17 – Application ID of track information

b_{17}	b_{16}	b_{15}	b_{14}	b_{13}	b_{12}	b_7	b_6	b_5	b_4	
APT_2	APT_2	APT_1	APT_1	APT_0	APT_0	TP_1	TP_1	TP_0	TP_0	ID
0	0	0	0	1	1	0	0	1	1	D-7 standard format
Others										Reserved

Table 18 – Pilot frame

	b_3	b_2
PF = 0	0	0
PF = 1	1	1

Table 19 – Bit stream of TIA for servo information F_0

PF = 0		PF = 1	
Order of recording	Codeword MSB LSB	Order of recording	Codeword MSB LSB
0	0010011101	0	0010011101
1	0101011001	1	0101011001
2	0101101001	2	0101100101
3	0010011101	3	0010011101
4	0101011001	4	0101011001
5	0101101001	5	0101100101
6	0010011101	6	0010011101
7	0101011001	7	0101011001
8	0101101001	8	0101100101

Table 20 – Bit stream of TIA for servo information F_1

PF = 0		PF = 1	
Order of recording	Codeword MSB LSB	Order of recording	Codeword MSB LSB
0	0111001000	0	0111001000
1	0101011011	1	0101011011
2	0101101011	2	0101100111
3	1000110111	3	1000110111
4	0101011011	4	0101011011
5	0101101001	5	0101100101
6	0111001000	6	0111001000
7	1010100100	7	1010100100
8	1010010100	8	1010011000

Table 21 – Bit stream of TIA for servo information F_2

PF = 0		PF = 1	
Order of recording	Codeword MSB LSB	Order of recording	Codeword MSB LSB
0	0111001000	0	0111001000
1	0101011011	1	0101011011
2	0101101011	2	0101100111
3	1000110111	3	1000110111
4	1010100100	4	1010100100
5	1010010100	5	1010011000
6	0111001000	6	0111001000
7	0101011011	7	0101011011
8	0101101011	8	0101100111

6.2.5 Insert and track information (ITI) post-amble

The bit stream of the ITI post-amble before recording shall be as defined in tables 22 to 24 in accordance with the low frequency pilot signals. The length of the ITI post-amble shall be 280 bits as recorded on tape.

Table 22 – Bit stream of ITI post-amble for servo information F_0

Order of recording	Codeword MSB LSB	Order of recording	Codeword MSB LSB	Order of recording	Codeword MSB LSB
0	1000101110	10	1000101110	20	1000101110
1	1000101110	11	1000101110	21	1000101110
2	1000101110	12	1000101110	22	1000101110
3	1000101110	13	1000101110	23	1000101110
4	1000101110	14	1000101110	24	1000101110
5	1000101110	15	1000101110	25	1000101110
6	1000101110	16	1000101110	26	1000101110
7	1000101110	17	1000101110	27	1000101110
8	1000101110	18	1000101110		
9	1000101110	19	1000101110		

Table 23 – Bit stream of ITI post-amble for servo information F_1

Order of recording	Codeword MSB LSB	Order of recording	Codeword MSB LSB	Order of recording	Codeword MSB LSB
0	0010001110	10	1101110001	20	1101110001
1	1101110001	11	1101110001	21	1101110001
2	1101110001	12	1101110001	22	1101110001
3	1101110001	13	1101110001	23	1000101110
4	1101110001	14	1000101110	24	0010001110
5	1000101110	15	0010001110	25	0010001110
6	0010001110	16	0010001110	26	0010001110
7	0010001110	17	0010001110	27	0010001110
8	0010001110	18	0010001110		
9	0010001110	19	1101110001		

Table 24 – Bit stream of ITI post-amble for servo information F_2

Order of recording	Codeword MSB LSB	Order of recording	Codeword MSB LSB	Order of recording	Codeword MSB LSB
0	1101110001	10	1101110001	20	0010001110
1	0010001110	11	1101110001	21	0010001110
2	0010001110	12	1101110001	22	1101110001
3	0010001110	13	0010001110	23	1101110001
4	1101110001	14	0010001110	24	1101110001
5	1101110001	15	0010001110	25	0010001110
6	1101110001	16	1101110001	26	0010001110
7	0010001110	17	1101110001	27	0010001110
8	0010001110	18	1101110001		
9	0010001110	19	0010001110		

6.3 Audio sector

6.3.1 Structure

The audio sector consists of the following elements:

- audio preamble;
- audio sync block;
- audio post-amble.

The audio sync block contains the following elements:

- pre-sync block;
- data sync block;
- post--sync block.

Figure 23 shows the structure of an audio sector.

The audio data in data sync block are described in clause 7. The audio pre and post-amble are described in 6.3.2 and 6.3.4 respectively. The audio sync block are described in 6.3.3.

6.3.2 Audio preamble

Two types of the audio preamble pattern are defined as shown below:

```
             MSB                                                LSB
Pattern A :  0 0 0 1 1 1 0 0 0 1 1 1 0 0 0 0 0 1 1 1 0 0 0 1 1
Pattern B :  1 1 1 0 0 0 1 1 1 0 0 0 1 1 1 1 1 0 0 0 1 1 1 0 0
```

Before the recording, a preamble pattern shall be chosen from the above two sequences according to the criteria as described in 6.1.3.2. The length of the audio preamble shall be 400 bits as recorded on tape.

6.3.3 Audio sync block

Three components, two pre-sync blocks, 14 data sync blocks, and one post-sync block constitute the overall audio sync block structure. Each of the two pre-sync blocks consists of a two-byte sync word and a four-byte ID word comprising ID0, ID1, IDP, and ID2. The post-sync block consists of a two-byte sync word and a four-byte ID word comprising ID0, ID1, IDP, and ID3. The audio data sync block consists of a two-byte sync word, a three-byte ID, and 85 bytes of audio data including inner parity, or 85 bytes of outer and inner parity data, as shown in figure 24.

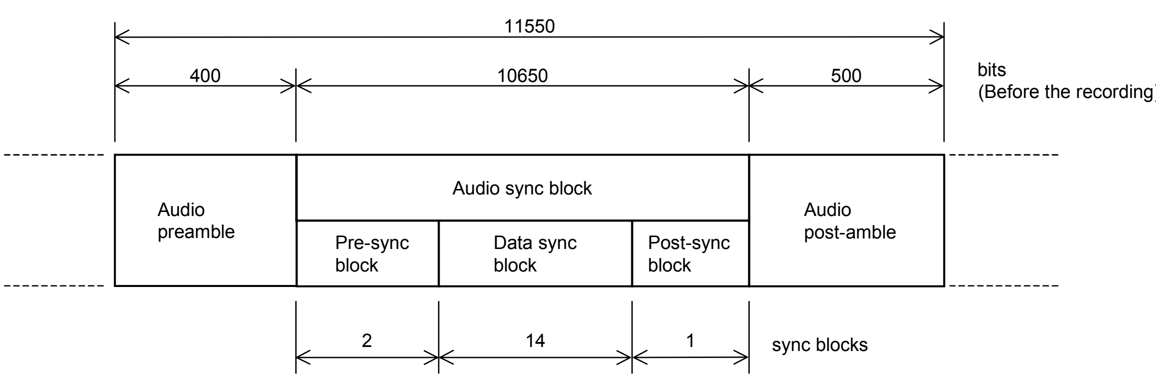
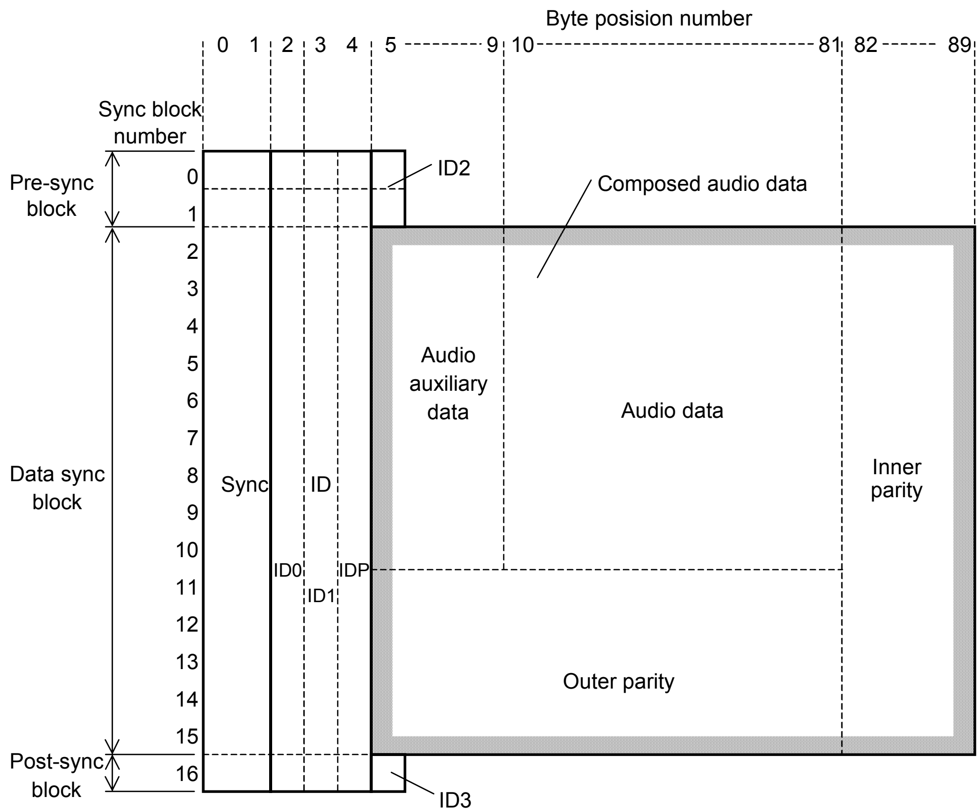


Figure 23 – Structure of audio sector



NOTE – Sync in byte position 0 and 1 shows the position. It is 17 bit pattern as specified in 6.3.3.1.

Figure 24 – Structure of sync blocks in audio sector

6.3.3.1 Sync

Two types of sync patterns are defined as shown below:

	MSB																LSB
Sync pattern F :	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	1
Sync pattern G :	1	1	1	0	0	0	0	0	0	0	0	0	0	1	1	1	0

A sync pattern to be recorded shall be chosen from the above two sequences according to the criteria as described in 6.1.3.2. The length of the sync shall be 17 bits as recorded on tape.

6.3.3.2 ID

The ID consists of ID data (ID0, ID1) of 2 bytes, and ID parity (IDP) of 1 byte. As shown in tables 25 to 28, the ID data consists of the audio application ID ($AP1_2$, $AP1_1$, $AP1_0$), track pair number (Trp_3, Trp_2, Trp_1, Trp_0), and sync block number (Syb_7, Syb_6, Syb_5, Syb_4, Syb_3, Syb_2, Syb_1, Syb_0).

– ID0

ID0 contains the information defined in table 25. The length of ID0 shall be 8 bits before modulation. Audio application ID shall be as given in table 26. The track pair number shall be as defined in table 27 or 28.

Table 25 – ID0 in audio sector

	Sync block number 0, 1, 11 to 16	Sync block number 2 to 10
Bit 7	$AP1_2$	Arb
Bit 6	$AP1_1$	Arb
Bit 5	$AP1_0$	Arb
Bit 4	Arb	Arb
Bit 3	Trp_3	Trp_3
Bit 2	Trp_2	Trp_2
Bit 1	Trp_1	Trp_1
Bit 0	Trp_0	Trp_0

Table 26 – Audio application ID

Audio application ID			Format type
$AP1_2$	$AP1_1$	$AP1_0$	
0	0	0	Not used
0	0	1	D-7 format
0	1	0	Reserved
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	Not used

Table 27 – Track pair number for 25 Mb/s format

Track number	Track pair number							
	525/60 system				625/50 system			
	Trp_3	Trp_2	Trp_1	Trp_0	Trp_3	Trp_2	Trp_1	Trp_0
0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0
2	0	0	0	1	0	0	0	1
3	0	0	0	1	0	0	0	1
4	0	0	1	0	0	0	1	0
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
9	0	1	0	0	0	1	0	0
10	Nonexistent				0	1	0	1
11					0	1	0	1
NOTE – Track numbers as shown in figure 10 or 11.								

Table 28 – Track pair number for 50 Mb/s format

Track number	Track pair number							
	525/60 system				625/50 system			
	Trp_3	Trp_2	Trp_1	Trp_0	Trp_3	Trp_2	Trp_1	Trp_0
0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0
2	0	0	0	1	0	0	0	1
3	0	0	0	1	0	0	0	1
4	0	0	1	0	0	0	1	0
:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:
19	1	0	0	1	1	0	0	1
20	Nonexistent				1	0	1	0
21					1	0	1	0
22					1	0	1	1
23					1	0	1	1
NOTE – Track numbers as shown in figure 12 or 13.								

– ID1

ID1 contains the sync block number defined as follows:

MSB							LSB
Syb_7	Syb_6	Syb_5	Syb_4	Syb_3	Syb_2	Syb_1	Syb_0

The length of ID1 shall be 8 bits before modulation.
The sync block numbers shall be numbered from 0 to 16 as shown in figure 24.
Modulation shall be applied together with ID1, IDP, and ID2 or ID3 or the first audio data as shown in figure 15.

- Randomization: See 6.1.3.1;
- 24-25 modulation: See 6.1.3.2;
- Pre-coding: See 6.1.3.3.

– IDP

IDP is a parity byte of ID0 and ID1. The length of the IDP shall be 8 bits before modulation.

IDP is defined as a (12, 8, 3) BCH code of which the generator polynomial is $X^4 + X + 1$. The ID code is divided into two ID codewords (ID-CW0, ID-CW1). The bit assignment of ID codewords is shown in table 29.

ID-CW0 : C14, C12, C10, C8, C6, C4, C2, C0, P6, P4, P2, P0
ID-CW1 : C15, C13, C11, C9, C7, C5, C3, C1, P7, P5, P3, P1

Parity bits P0 to P7 are given by the following equations:

$P6 = C14 \oplus C10 \oplus C6 \oplus C4$
$P4 = C14 \oplus C12 \oplus C8 \oplus C4 \oplus C2$
$P2 = C14 \oplus C12 \oplus C10 \oplus C6 \oplus C2 \oplus C0$
$P0 = C12 \oplus C8 \oplus C6 \oplus C0$
$P7 = C15 \oplus C11 \oplus C7 \oplus C5$
$P5 = C15 \oplus C13 \oplus C9 \oplus C5 \oplus C3$
$P3 = C15 \oplus C13 \oplus C11 \oplus C7 \oplus C3 \oplus C1$
$P1 = C13 \oplus C9 \oplus C7 \oplus C1$

where ⊕ is the symbol of an exclusive -or.

Modulation shall be done together with ID1, IDP, and ID2 or ID3 or the first audio data as shown in figure 15.

- Randomization: See 6.1.3.1;
- 24-25 modulation: See 6.1.3.2;
- Pre-coding: See 6.1.3.3.

Table 29 – Bit assignment of ID codewords

	Byte position number		
	2 ID0	3 ID1	4 IDP
MSB	C15	C7	P7
	C14	C6	P6
	C13	C5	P5
	C12	C4	P4
	C11	C3	P3
	C10	C2	P2
	C9	C1	P1
LSB	C8	C0	P0

6.3.3.3 Additional ID (ID2, ID3)

Byte position number 5 of the pre-sync blocks (ID2) shall be set to $F0_h$ before modulation. Byte position number 5 of the post-sync block (ID3) shall be set to FF_h before modulation.

The following operations shall be performed on additional ID together with ID1, IDP, and ID2 or ID3 or the first audio data.

- Randomization: See 6.1.3.1;
- 24-25 modulation: See 6.1.3.2;
- Pre-coding: See 6.1.3.3.

6.3.3.4 Composed audio data

As shown in figure 24, composed audio data contain the audio data, audio auxiliary data, inner error code, and outer error code.

The composed audio data length shall be 85 bytes. By including the last two bytes of the ID, the length of the composed audio data shall be 87 bytes, divisible into 3-byte length sections for additional processing as described below:

- Randomization: See 6.1.3.1;
- 24-25 modulation: See 6.1.3.2;
- Pre-coding: See 6.1.3.3.

6.3.4 Audio post-amble

The audio post-amble shall be the same as the audio preamble described in 6.3.2 except for the length. The length of the audio post-amble shall be 500 bits as recorded on tape.

- Randomization: None;
- 24-25 modulation: See 6.1.3.2;
- Pre-coding: None.

6.4 Video sector

6.4.1 Structure

The video sector contains the following elements:

- video preamble;
- video sync block;
- video post-amble.

The video sync block contains the following elements:

- pre-sync block;
- data sync block;
- post-sync block.

Figure 25 shows the structure of the video sector.

The video data in data sync block are described in clause 8. The video pre and post-amble are described in 6.4.2 and 6.4.3.5 respectively. The video sync block are described in 6.4.3

6.4.2 Video preamble

The video preamble pattern shall be the same as that of the audio preamble described in 6.3.2. The length of the video preamble shall be 400 bits as recorded on tape.

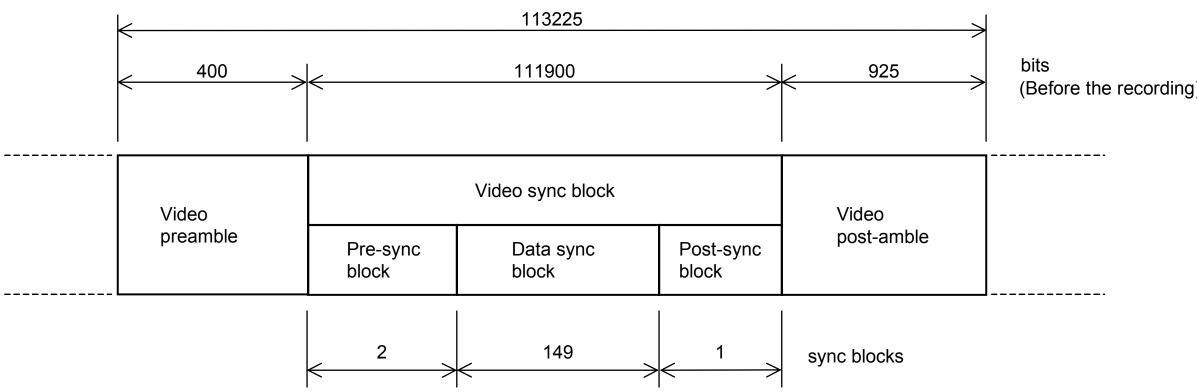


Figure 25 – Structure of video sector

6.4.3 Video sync block

Three components, two pre-sync blocks, 149 data sync blocks, and one post-sync block constitute the overall video sync block structure. Each of the two pre-sync blocks consists of a 2-byte sync word and a 4-byte ID word comprising ID0, ID1, IDP, and ID2. The post-sync block consists of a 2-byte sync word and a 4-byte ID word comprising ID0, ID1, IDP, and ID3. Each data sync block is comprised of either 1) 2-byte sync block word, 3-byte ID, 77 bytes of data, and 8 inner parity bytes; or 2) 2-byte sync block word, 3-byte ID, 77 bytes of outer parity, and 8 inner parity bytes, as shown in figure 26.

6.4.3.1 Sync

Sync shall be the same as the audio sync described in 6.3.3.1. The length of the sync shall be 17 bits as recorded on tape.

6.4.3.2 ID

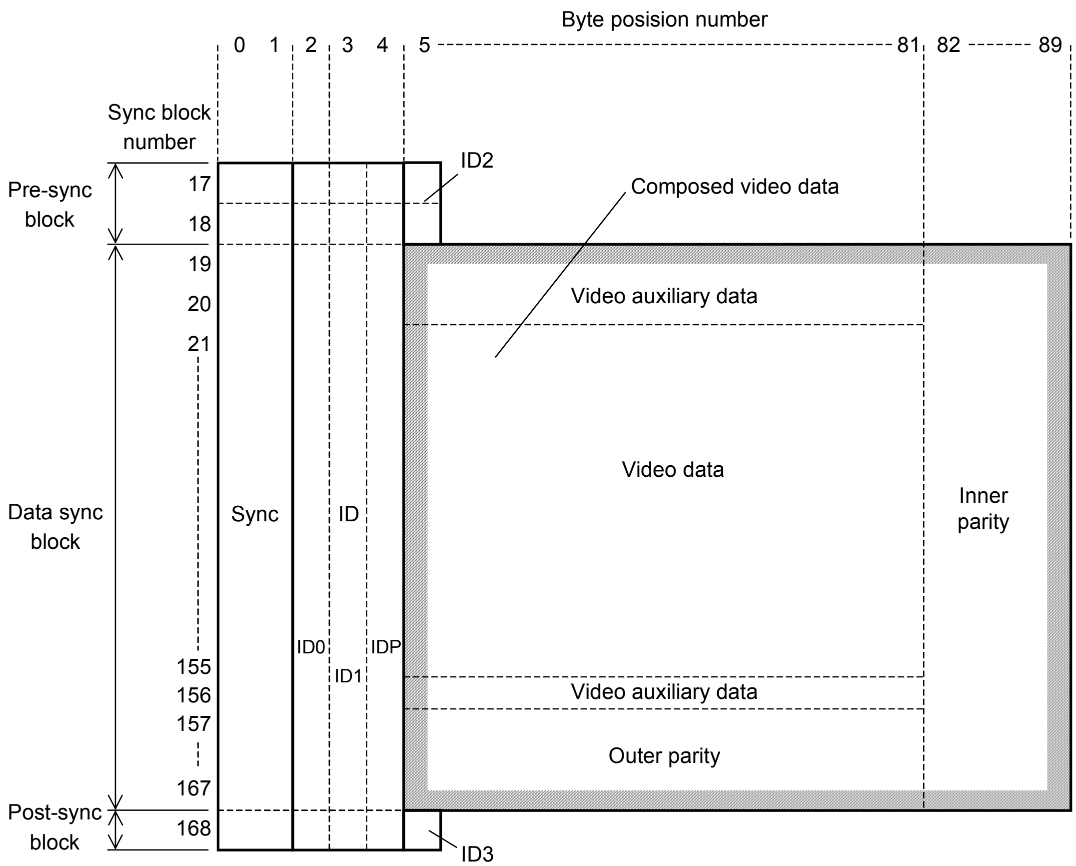
ID consists of ID data (ID0, ID1) of 2 bytes and ID parity (IDP) of 1 byte. ID data consist of the video application ID ($AP2_2$, $AP2_1$, $AP2_0$), track pair number (Trp_3, Trp_2, Trp_1, Trp_0), and sync block number (Syb_7, Syb_6, Syb_5, ……, Syb_0).

– **ID0**

ID0 contains the information given in table 30. The length of ID0 shall be 8 bits before modulation.

Video application ID shall be as specified in table 31. The track pair number shall be the same as that in table 27 or 28.

- Randomization: See 6.1.3.1;
- 24-25 modulation: None;
- Pre-coding: See 6.1.3.3.



NOTE – Sync in byte position 0 and 1 shows the position. It is 17 bit pattern as specified in 6.3.3.1.

Figure 26 – Structure of sync blocks in video sector

Table 30 – ID data in video sector

Bit position	Sync block number 17 to 18 and 157 to 168		Sync block number 19 to 156	
	ID0	ID1	ID0	ID1
b7	$AP2_2$	Syb_7	Arb	Syb_7
b6	$AP2_1$	Syb_6	Arb	Syb_6
b5	$AP2_0$	Syb_5	Arb	Syb_5
b4	Arb	Syb_4	Arb	Syb_4
b3	Trp_3	Syb_3	Trp_3	Syb_3
b2	Trp_2	Syb_2	Trp_2	Syb_2
b1	Trp_1	Syb_1	Trp_1	Syb_1
b0	Trp_0	Syb_0	Trp_0	Syb_0

– ID1

ID1 contains the sync block number defined as follows:

MSB LSB

Syb_7	Syb_6	Syb_5	Syb_4	Syb_3	Syb_2	Syb_1	Syb_0

The length of ID1 shall be 8 bits before modulation. The sync block numbers shall be numbered from 17 to 168 as shown in figure 26. The length of the composed video data shall be 85 bytes before modulation. Modulation shall be done together with ID1, IDP, and ID2 or ID3 or the first video data, and/or followed every 3 video data bytes as shown in figure 16.

- Randomization: See 6.1.3.1;
- 24-25 modulation: See 6.1.3.2;
- Pre-coding: See 6.1.3.3.

– IDP

IDP shall be the same as that in 6.3.3.1. The length of the IDP shall be 8 bits before modulation. The length of the composed video data shall be 85 bytes before modulation. Modulation shall be done together with ID1, IDP, and ID2 or ID3 or the first video data, and/or followed every three video data bytes as shown in figure 16.

- Randomization: See 6.1.3.1;
- 24-25 modulation: See 6.1.3.2;
- Pre-coding: See 6.1.3.3.

Table 31 – Video application ID

Video application ID			Format type
$AP2_2$	$AP2_1$	$AP2_0$	
0	0	0	Not used
0	0	1	D-7
0	1	0	Reserved
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	Not used

6.4.3.3 Additional ID (ID2, ID3)

Byte position number 5 of pre-sync blocks (ID2) shall be set to $F0_h$ before modulation. Byte position number 5 of post-sync block (ID3) shall be set to FF_h before modulation.

6.4.3.4 Composed video data

Composed video data contains the video data, video auxiliary data, inner error code, and outer error code as shown in figure 26.

The composed video data length shall be 85 bytes. By including the last two bytes of ID, the length of the composed video data shall be 87 bytes, divisible into 3 byte-length sections for additional processing as described below:

- Randomization: See 6.1.3.1;
- 24-25 modulation: See 6.1.3.2;
- Pre-coding: See 6.1.3.3.

6.4.3.5 Video post-amble

The video post-amble shall be the same as the audio preamble described in 6.3.2 except for the length.
The length of the video post-amble shall be 925 bits as recorded on tape.

6.5 Subcode sector

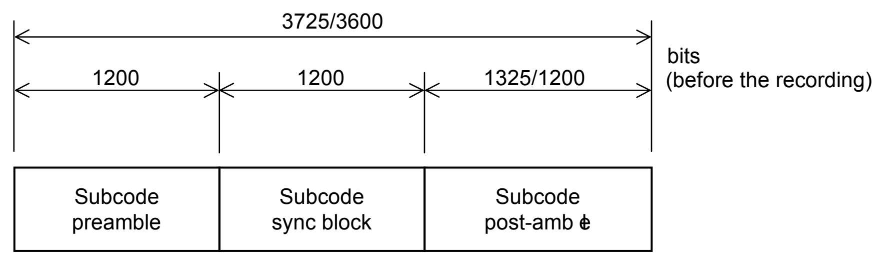
6.5.1 Structure

The subcode sector contains the following elements:

- subcode preamble;
- subcode sync block;
- subcode postamble.

Figure 27 shows the structure of a subcode sector.

The subcode data in data sync block are described in clause 9. The subcode preamble and post-amble are described in 6.5.2 and 6.5.3.4 respectively. The subcode sync block are described in 6.5.3.



NOTE - 525/60 system / 625/50 system

Figure 27 – Structure of subcode sector

6.5.2 Subcode preamble

The subcode preamble pattern shall be the same as the audio preamble pattern described in 6.3.2 except for the length.
The length of the subcode preamble shall be 1200 bits as recorded on tape.

6.5.3 Subcode sync block

The subcode sync block contains 12 sync blocks. Each sync block contains sync of 2 bytes, ID of 3 bytes, and composed subcode data of 7 bytes. Figure 28 shows a structure of the subcode sync block.

6.5.3.1 Sync

Two types of sync patterns are defined as shown below:

```
                   MSB                                LSB
Sync pattern D  :  0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 0 1
Sync pattern E  :  1 1 1 1 1 0 0 0 0 0 0 0 0 0 0 1 0
```

A sync pattern to be recorded shall be chosen from the above two sequences according to the criteria described in 6.1.3.2. The length of the sync shall be 17 bits as recorded on tape.

6.5.3.2 ID

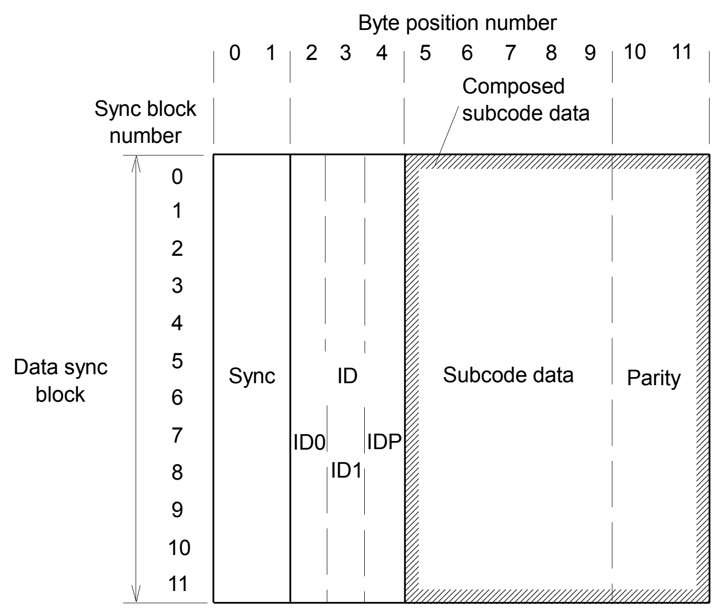
The ID consists of ID data (ID0, ID1) of 2 bytes and ID parity (IDP) of 1 byte. ID data consists of the FRID, sync block number (Syb_3, Syb_2, Syb_1, Syb_0), and/or subcode application ID ($AP3_2$, $AP3_1$, $AP3_0$), and/or track application ID (APT_2, APT_1, APT_0).

Table 32 defines the contents of ID0 and ID1. The subcode application ID shall be as defined in table 33. The length of the ID shall be as follows:

- ID0: 8 bits;
- ID1: 8 bits;
- IDP: 8 bits before modulation.

Modulation shall be applied together with ID1, IDP, and the first subcode data as shown in figure 17.

- Randomization: See 6.1.3.1;
- 24-25 modulation: See 6.1.3.2;
- Pre-coding: See 6.1.3.3.



NOTE – Sync in byte position 0 and 1 shows the position. It is 17 bit pattern as specified in 6.5.3.1.

Figure 28 – Structure of sync blocks in subcode sector

–Table 32 – ID data in subcode sector

Bit position	Sync block number 0 and 6		Sync block number 1 to 5 and 7 to 10		Sync block number 11	
	ID0	ID1	ID0	ID1	ID0	ID1
b7 (MSB)	FR	Arb	FR	Arb	FR	Arb
b6	$AP3_2$	Arb	Res	Arb	APT_2	Arb
b5	$AP3_1$	Arb	Res	Arb	APT_1	Arb
b4	$AP3_0$	Arb	Res	Arb	APT_0	Arb
b3	Arb	Syb_3	Arb	Syb_3	Arb	Syb_3
b2	Arb	Syb_2	Arb	Syb_2	Arb	Syb_2
b1	Arb	Syb_1	Arb	Syb_1	Arb	Syb_1
b0 (LSB)	Arb	Syb_0	Arb	Syb_0	Arb	Syb_0

FR : The identification for the first or second half of each channel:

1 = the first half of each channel;
0 = the second half of each channel.

Table 33 – Subcode application ID

Subcode application ID $AP3_2$	$AP3_1$	$AP3_0$	Format type
0	0	0	Not used
0	0	1	D-7
0	1	0	Reserved
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	Not used

IDP shall be the same as that in 6.3.3.2.

Modulation shall be applied together with ID1, IDP, and the first video data as shown in figure 17.

- Randomization: See 6.1.3.1;
- 24-25 modulation: See 6.1.3.2;
- Pre-coding: See 6.1.3.3.

6.5.3.3 Composed subcode data

Composed subcode data structure consists of 12 subcode data blocks. Each subcode data block is composed of a 2-byte sync word, 3-byte ID, and 7 bytes of subcode data and parity. Three bytes consisting of ID1, IDP, and the first video data byte shall be processed through the following three operations:

- Randomization: See 6.1.3.1;
- 24-25 modulation: See 6.1.3.2;
- Pre-coding: See 6.1.3.3.

6.5.3.4 Subcode post-amble

The subcode post-amble shall be the same as the audio preamble described in 6.3.2 except for the length. The length of the subcode post-amble shall be 1325 bits for the 525/60 system and 1200 bits for the 625/50 system as recorded on tape.

6.6 Edit gap

The space between areas on a track is used to accommodate timing errors during editing. In an original recording the edit gap shall record concatenations of run patterns A and B defined as follows:

```
                 MSB                                                    LSB
Run pattern A :  0 0 0 1 1 1 0 0 0 1 1 1 0 0 0 0 0 1 1 1 0 0 0 1 1
Run pattern B :  1 1 1 0 0 0 1 1 1 0 0 0 1 1 1 1 1 0 0 0 1 1 1 0 0
```

During an edit, the edit gap may be partially rewritten with the above concatenations provided that the preamble and post-amble of adjacent unedited areas are not overwritten.

Each preamble of areas except area 0 begins with run-up. Each postamble of areas except area 0 ends with the guard area. The run-up and the guard area shall be recorded concatenations of run patterns A and B.

Run patterns A and B are already modulated patterns under the rule of interleaved NRZI modulation. The choice of a run pattern between A and B depends on the restriction described in 6.1.3.2.
The length of the edit gaps shall be as follows:

– edit gap 1: 625 bits;
– edit gap 2: 700 bits;
– edit gap 3: 1550 bits as recorded on tape.

7 Audio processing

7.1 Introduction

Audio data accompanying the video frame is processed simultaneously. The audio data shall be recorded on 10 consecutive tracks in each frame for the 525/60 system and 12 consecutive tracks in each frame for the 625/50 system for 25 Mb/s format. The audio data shall be recorded on 20 consecutive tracks in each frame for the 525/60 system and 24 consecutive tracks in each frame for the 625/50 system for 50 Mb/s format.

Each audio sector consists of audio data, audio auxiliary data (AAUX), and inner and outer parity data as shown in figure 24. Audio data are shuffled within the audio data block of 77 columns x 9 rows prior to the addition of parity data. Each audio channel is identically but independently processed. Audio data are modulated by 24-25 code prior to recording. The total audio data processing sequence is shown in figure 8.

7.2 Encoding mode

7.2.1 Source coding

Each audio input signal is sampled at 48kHz, which is locked to the video signal, with 16-bit quantization. The system provides two-channels simultaneous recording for 25 Mb/s format and four-channels simultaneous recording for 50 Mb/s format.

Audio data is processed in frames. Each frame contains 1602 or 1600 audio samples (525/60 system) or 1920 audio samples (625/50 system) for an audio channel with associated status, user, and validity data. For the 525/60 system, the number of audio samples per frame shall follow the five-frame sequence as shown below:

1600, 1602, 1602, 1602, 1602 samples.

Audio recording capacity is 1620 samples per frame for the 525/60 system or 1944 samples per frame for the 625/50 system. The unused space at the end of each frame is filled with arbitrary values.
In addition, a number of control and user words are added to the data.

7.2.2 Emphasis

Audio encoding is carried out with the first order pre-emphasis of 50/15μs. For the analog-input recording, emphasis should be off in the default state.

7.2.3 Audio error code

In the audio encoded data, 8000_h shall be assigned as the audio error code to indicate the invalid audio sample. This code corresponds to the negative full-scale value in ordinary twos complement representation. When the encoded data include 8000_h, it shall be converted to 8001h before audio processing and recording.

7.2.4 Relative audio-video timing

The audio frame duration equals the video frame period. An audio frame begins with the audio sample acquired within the duration of minus 50 samples to zero samples from the first pre-equalizing pulse of the vertical blanking period of the input video signal. The first pre-equalizing pulse means the beginning of line number 1 for the 525-60 system, and the middle of line number 623 for the 625/50 system.

7.3 Audio shuffling

The 16-bit audio data word is divided into two bytes: the upper byte which contains the MSB and the lower byte with the LSB, as shown in figure 29. Audio data shall be shuffled over tracks and data-sync blocks within a frame. The data bytes are defined as D_n (n = 0, 1, 2, ...) which is sampled at nth order within a frame and shuffled by each D_n unit.

The data shall be shuffled through a process as expressed by the following equations:

525/60 system:

Track number:	(INT (n/3) + 2 x (n mod 3)) mod 5	for CH1
	(INT (n/3) + 2 x (n mod 3)) mod 5 + 5	for CH2
	(INT (n/3) + 2 x (n mod 3)) mod 5 + 10	for CH3
	(INT (n/3) + 2 x (n mod 3)) mod 5 + 15	for CH4
Sync block number:	2 + 3 x (n mod 3) + INT ((n mod 45) / 15)	
Byte position number:	10 + 2 x INT(n/45)	for the most significant byte
	11 + 2 x INT(n/45)	for the least significant byte
	where n = 0 to 1619	

625/50 system:

Track number:	(INT (n/3) + 2 x (n mod 3)) mod 6	for CH1
	(INT (n/3) + 2 x (n mod 3)) mod 6 + 6	for CH2
	(INT (n/3) + 2 x (n mod 3)) mod 6 + 12	for CH3
	(INT (n/3) + 2 x (n mod 3)) mod 6 + 18	for CH4

Sync block number: 2 + 3 x (n mod 3) + INT ((n mod 54) / 18)

Byte position number: 10 + 2 x INT(n/54) for the most significant byte
11 + 2 x INT(n/54) for the least significant byte

where n = 0 to 1943

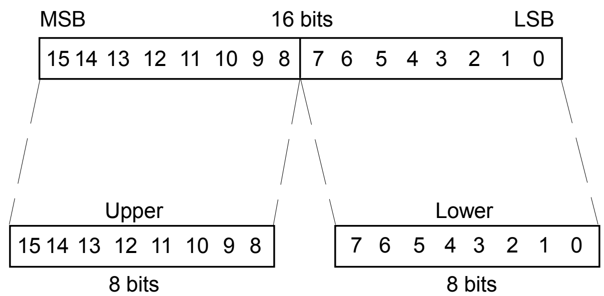


Figure 29 – Sample to audio data bytes conversion

7.4 Audio auxiliary data (AAUX)

AAUX shall be added to the shuffled audio data as shown in figure 24. The AAUX packet shall include a pack header, the data of the AAUX source pack (AS), and AAUX source control pack (ASC). The length of AS and ASC shall be a fixed value of 5 bytes as shown in figure 30, which shows the AAUX pack arrangement for each track. One audio auxiliary data packet consists of nine sync blocks, numbers 2 through 10. Byte positions 5 through 9 of each sync block constitute the data, with byte position 5 the pack header. Therefore, there are nine packs in each track. Packs are numbered 0 to 8 from the entrance side of the audio sector in the order as shown in figure 30. This number is called the audio pack number.

Table 34 shows the AAUX data which include the AAUX source pack and the AAUX source control pack.
AAUX has a reserved data area as shown below:

25 Mb/s format

-525/60 system
5 bytes x 7 packs x 10 tracks x 30 frames = 10500 bytes/s

-625/50 system
5 bytes x 7 packs x 12 tracks x 25 frames = 10500 bytes/s

50 Mb/s format

-525/60 system
5 bytes x 7 packs x 20 tracks x 30 frames = 21000 bytes/s

-625/50 system
5 bytes x 7 packs x 24 tracks x 25 frames = 21000 bytes/s

The reserved area shall be filled up by FFh.

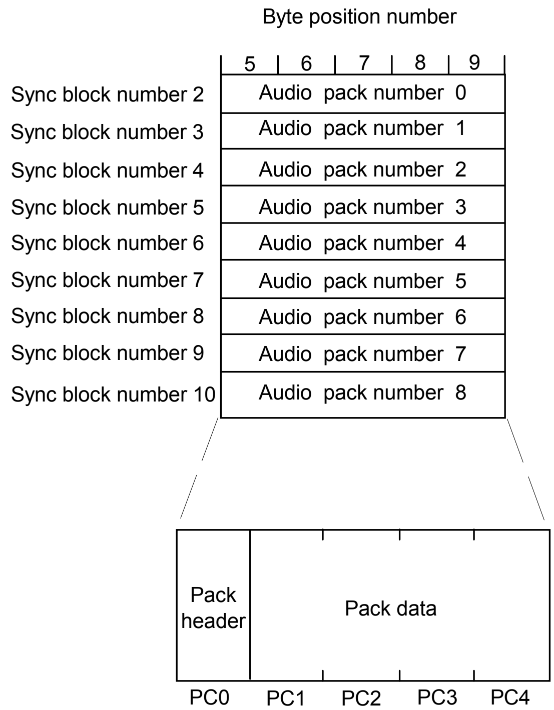


Figure 30 – Arrangement of AAUX packs in audio auxiliary data

Table 34 – AAUX data

Audio pack number		AAUX data of a video frame
Track A	Track B	
3	0	AS
4	1	ASC

NOTES
AS: AAUX source pack (pack header = 50h)
ASC: AAUX source control pack (pack header = 51h)
Unused AAUX packs shall be reserved.

25 Mb/s format
525/60 system
Track A: Track number 0, 2, 4, 6, 8
Track B: Track number 1, 3, 5, 7, 9
625/50 system
Track A: Track number 0, 2, 4, 6, 8, 10
Track B: Track number 1, 3, 5, 7, 9, 11

50 Mb/s format
525/60 system
Track A: Track number 0, 1, 4, 5, 8, 9, 12, 13, 16, 17
Track B: Track number 2, 3, 6, 7, 10, 11, 14, 15, 18, 19
625/50 system
Track A: Track number 0, 1, 4, 5, 8, 9, 12, 13, 16, 17, 20, 21
Track B: Track number 2, 3, 6, 7, 10, 11, 14, 15, 18, 19, 22, 23

7.4.1 AAUX source pack (AS)

The AAUX source pack shall be configured as shown in table 35.

Table 35 - Mapping of AAUX source pack

<table>
<tr><td></td><td>MSB</td><td></td><td></td><td></td><td></td><td></td><td></td><td>LSB</td></tr>
<tr><td>PC0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>PC1</td><td>LF</td><td>Res</td><td colspan="6">AF SIZE</td></tr>
<tr><td>PC2</td><td>0</td><td colspan="2">CHN</td><td>0</td><td colspan="4">AUDIO MODE</td></tr>
<tr><td>PC3</td><td>Res</td><td>Res</td><td>50/60</td><td colspan="5">STYPE</td></tr>
<tr><td>PC4</td><td>Arb</td><td>Res</td><td colspan="3">SMP</td><td colspan="3">QU</td></tr>
<tr><td colspan="9">NOTES - Res means reservation for future use. Hereafter, the default value of Res shall be set to 1.</td></tr>
</table>

LF : Locked mode flag
Locking condition of audio sampling frequency with video signal
0 = Locked mode
1 = Reserved

AF SIZE : The number of audio samples per frame
0 1 0 1 0 0 b = 1600 samples / frame (525/60 system)
0 1 0 1 1 0 b = 1602 samples / frame (525/60 system)
0 1 1 0 0 0 b = 1920 samples / frame (625/50 system)

CHN : The number of audio channels within an audio block
0 0b = One channel per audio block
Others = Reserved
The audio block is composed of five audio sectors in five consecutive tracks for the 525/60 system; six audio sectors in six consecutive tracks for the 625/50 system.

AUDIO MODE: The contents of the audio signal on each channel
0 0 0 0 b = CH1(CH3)
0 0 0 1 b = CH2(CH4)
1 1 1 1 b = Invalid audio data
Others = Reserved

50/60:
0 = 60-field system
1 = 50-field system

STYPE: STYPE defines audio blocks per video frame
0 0 0 0 0 b = 2 audio blocks
0 0 0 1 0 b = 4 audio blocks
Others = Reserved

SMP: Sampling frequency
0 0 0 b = 48 kHz
Others = Reserved

QU: Quantization
0 0 0 b = 16 bits linear
Others = Reserved

7.4.2 AAUX source control pack (ASC)

Table 36 shows a mapping of the AAUX source control pack.

Table 36 - Mapping of AAUX source control pack

	MSB							LSB
PC0	0	1	0	1	0	0	0	1
PC1	EDIT ST		EDIT END		CGMS		EFC	
PC2	Arb	Arb	0	0	Res	Res	Res	Res
PC3	Res	0	Res	0	0	0	0	0
PC4	Arb	Res	Res	Res	Res	Res	Res	Res

EDIT ST : Start position of insert edit
0 0 b = Unedited portion
0 1 b = Editing point without fading
1 0 b = Editing point with fading
1 1 b = Reserved
The duration of recording EDIT ST shall be one audio block period for each channel.

EDIT END : End position of insert edit
0 0 b = Unedited portion
0 1 b = Editing point without fading
1 0 b = Editing point with fading
1 1 b = Reserved
The duration of recording EDIT END shall be one audio block period for each channel.

CGMS : Copy generation management system

CGMS	Copy possible generation
0 0	Copy Free
0 1 1 0 1 1	TBA

EFC : Emphasis channel flag
0 0 b = Emphasis off
0 1 b = Emphasis on
Others = Reserved
EFC shall be set for each audio block.

7.5 Error correction code addition

Audio data are protected by inner and outer error correction codes.

7.5.1 Inner error correction code

The inner parity as shown in figure 24 is defined as the codeword of an inner error correction code. The inner error correction code is a (85, 77) Reed-Solomon code in GF(256) of which the field generator polynomial is:

$$X^8 + X^4 + X^3 + X^2 + 1$$

where X^i are place-keeping variables in GF(2), the binary field.

The generator polynomial of the code in GF(256) is:

$$g_{in}(X) = (X + 1)(X + \alpha)(X + \alpha^2)(X + \alpha^3)(X + \alpha^4)(X + \alpha^5)(X + \alpha^6)(X + \alpha^7)$$

where α is given by 2_h in GF(256).

The inner parity bytes K_7, K_6, K_5, K_4, K_3, K_2, K_1, K_0 as shown in figure 31 are given by the equation:

$$K_7X^7 + K_6X^6 + K_5X^5 + K_4X^4 + K_3X^3 + K_2X^2 + K_1X + K_0$$

which is a residue of $X^8D(X)$ divided by $g_{in}(X)$, where the data polynomial D(X) is defined as:

$$D(X) = D_{76}X^{76} + D_{75}X^{75} + \text{........} + D_2X^2 + D_1X + D_0$$

and the codeword polynomial is given by the following equation for every column of the byte position number 5 to 81:

$$D_{76}X^{84} + D_{75}X^{83} + \text{........} + D_1X^9 + D_0X^8 + K_7X^7 + K_6X^6 + \text{.........} + K_1X + K_0$$

7.5.2 Outer error correction code

The outer parity as shown in figure 24 is defined as a codeword of an outer error correction code. The outer error correction code is a (14, 9) Reed-Solomon code in GF(256) of which the field generator polynomial is:

$$X^8 + X^4 + X^3 + X^2 + 1$$

where X^i are place-keeping variables in GF(2), the binary field.

The generator polynomial of the code in GF(256) is:

$$g_{aout}(X) = (X + 1)(X + \alpha)(X + \alpha^2)(X + \alpha^3)(X + \alpha^4)$$

where α is given by 2_h in GF(256).

The outer parity bytes K_4, K_3, K_2, K_1, K_0 as shown in figure 32, are given by the equation:

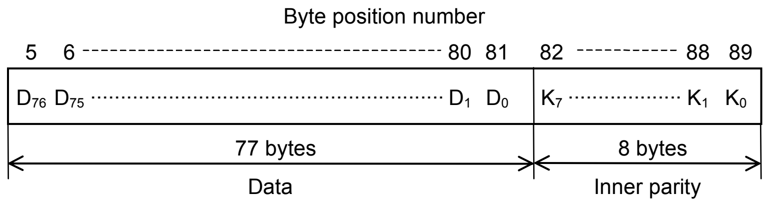
$$K_4X^4 + K_3X^3 + K_2X^2 + K_1X + K_0$$

which is a residue of $X^5D(X)$ divided by $g_{aout}(X)$, where the data polynomial D(X) is defined as:

$$D(X) = D_8X^8 + D_7X^7 + \text{........} + D_2X^2 + D_1X + D_0$$

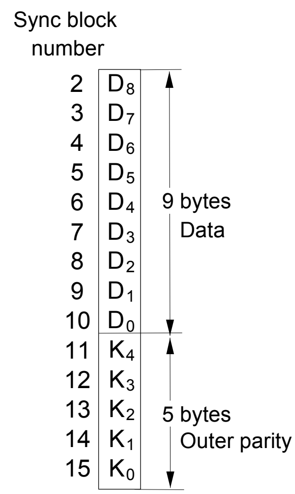
and the codeword polynomial is given by the following equation:

$$D_8X^{13} + D_7X^{12} + \text{........} + D_1X^6 + D_0X^5 + K_4X^4 + K_3X^3 + \text{.......} + K_1X + K_0$$



NOTE - D and K are in GF (256)

Figure 31 – Data and inner parity of a data sync block



NOTES - D and K are in GF(256).

Figure 32 – Data and outer parity of a data sync block for audio sector

8 Video processing

8.1 Introduction

The video component signals are sampled by 13.5 MHz for luminance (Y) and by 6.75 MHz for color difference (C_R, C_B) signals. Sampled data in vertical and horizontal blanking periods are discarded.
Active video data, after a shuffling process within the video frame, are bit rate reduced through adaptive DCT and VLC processes.

The shuffled video samples, mapped as a video frame of active samples from consecutive horizontal lines, are divided into DCT blocks. One DCT block contains 8 samples of 8 consecutive horizontal lines. Four luminance DCT blocks and two color difference DCT blocks of 4:1:1 compression or two luminance DCT blocks and two color difference DCT blocks of 4:2:2 compression form a macro block. Five macro blocks form a video segment. The data in the video segment are compressed into five compressed macro blocks through DCT and VLC processing.

Video auxiliary data (VAUX) are multiplexed with the compressed video data, and the multiplexed data are processed in a product block of 77 columns by 138 rows. The data in the product block are protected with the error correction codes added to the product block. Prior to recording, 24-25 modulation is applied (see figure 8).

8.2 Video structure

8.2.1 Sampling structure

The sampling structure is the same as that of 4:2:2 component television signals described in ITU-R BT.601. Sampling structures of luminance (Y) and the two color-difference signals (C_R, C_B) in the 4:2:2 structure are described in table 37.

– Pixel structure in one frame

Each pixel shall be converted to the code of twos complement (-508 to 507) by inverting the MSB of the input video signal.

4:1:1 compression

All sampled luminance pixels, 720 pixels per line, are retained for processing. Of 360 color-difference pixels sampled per line, every other pixel is discarded, leaving 180 pixels for processing. The number of active lines is 480 for 525/60 and 576 for 625/50 systems. Sampling processes start simultaneously for both luminance and color-difference signals. Figures 33 and 34 show the sampling process in detail. The template of the filtering for 4:2:2 / 4:1:1 conversion is defined in annex E.

4:2:2 compression

All sampled luminance pixels, 720 pixels per line and 360 color-difference pixels, are retained for processing as shown in figures 35 and 36. Sampling processes start simultaneously for both luminance and color-difference signals. As shown in figure 8, there is no pre-filtering for 50Mb/sformat.

– Line structure in one frame

For the 525/60 system, 240 lines of Y, C_R, and C_B signals from each field shall be transmitted.

For the 625/50 system, 288 lines of Y, C_R, and C_B signals from each field shall be transmitted. The transmitted active lines from each of two fields are described in table 37.

Table 37 – Construction of input video

		525/60 system	625/50 system
Sampling	Y	13.5 MHz	
	C_R, C_B	6.75 MHz	
Total number of pixels per line	Y	858	864
	C_R, C_B	429	432
Number of active pixels per line	Y	720	
	C_R, C_B	360	
Total number of lines per frame		525	625
Number of active lines per frame		480	576
Active line numbers	Field 1	23 to 262	23 to 310
	Field 2	285 to 524	335 to 622
Quantization		Each sample is linearly quantized to 10 bits for Y, C_R and C_B.	
Relation between video signal level and quantized level	Scale	4 to 1019	
	Y	Video signal level of white: 940 Video signal level of black: 64	Quantized level 877
	C_R, C_B	Video signal level of gray : 512	Quantized level 897

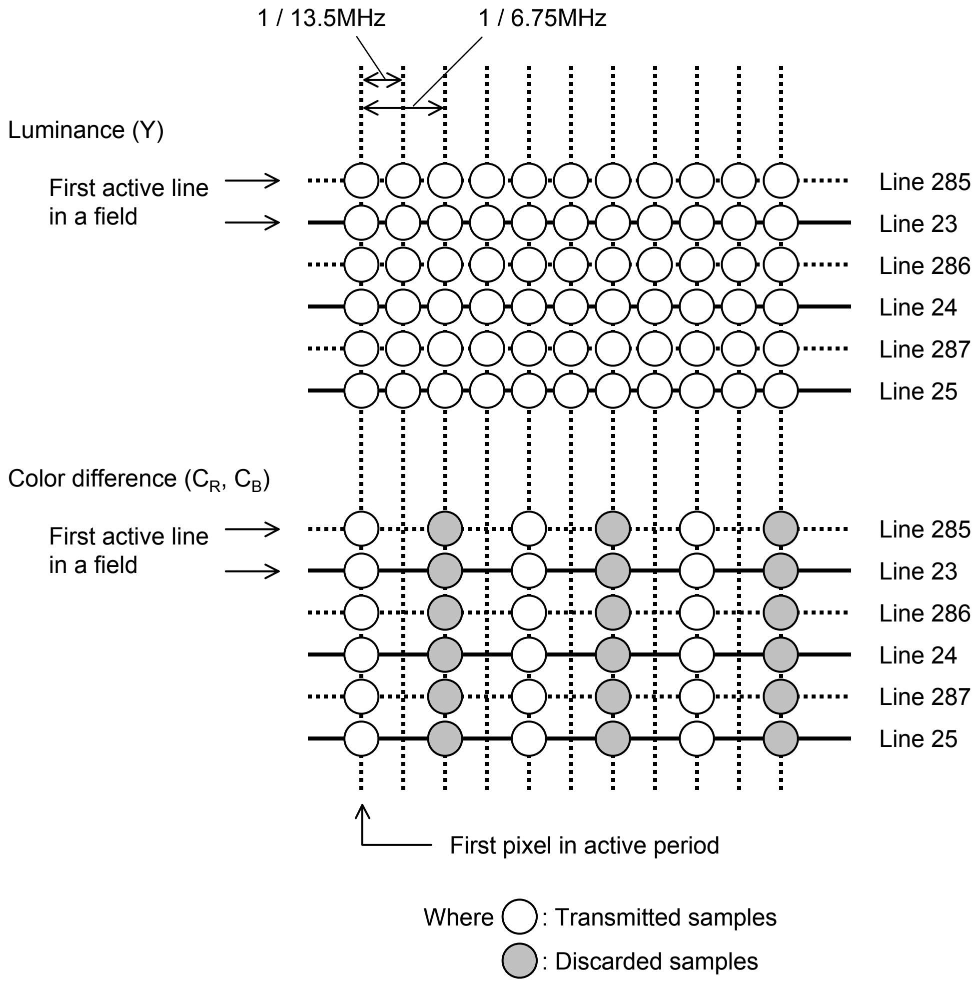


Figure 33 – Transmitted samples for 525/60 system with 4:1:1 compression

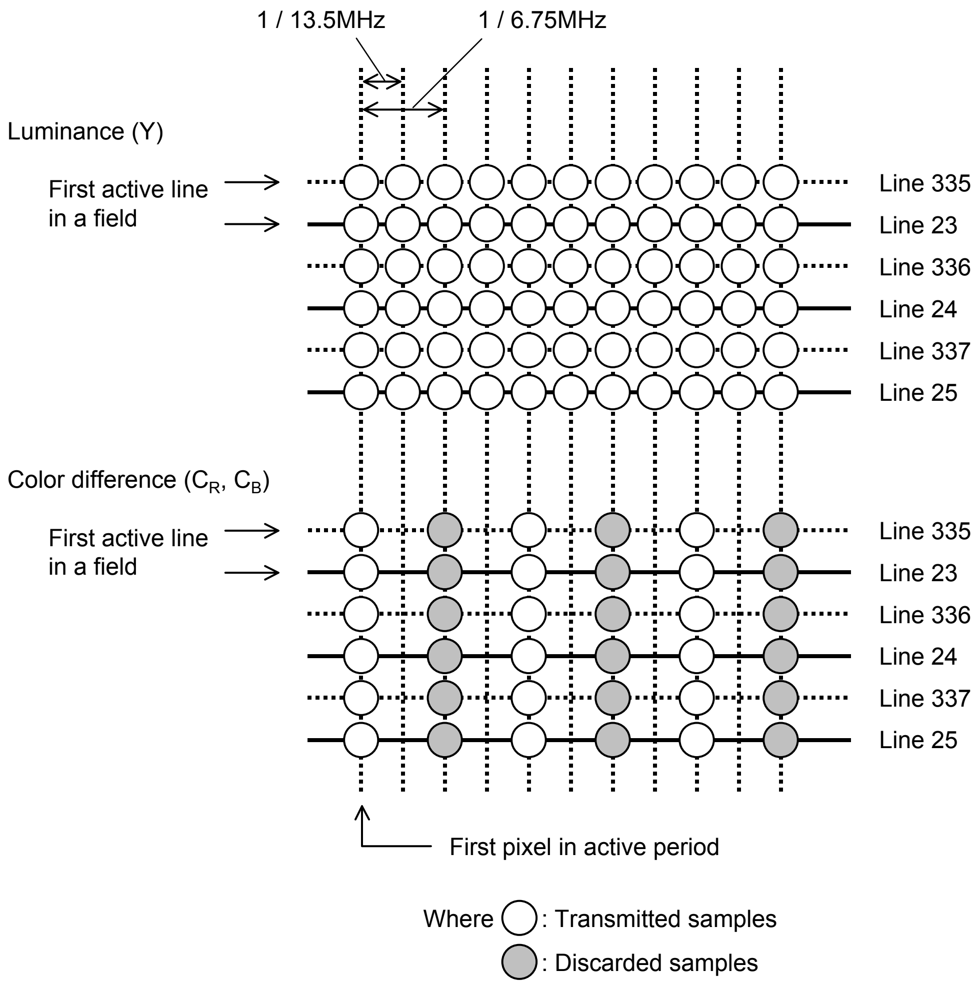


Figure 34 – Transmitted samples for 625/50 system with 4:1:1 compression

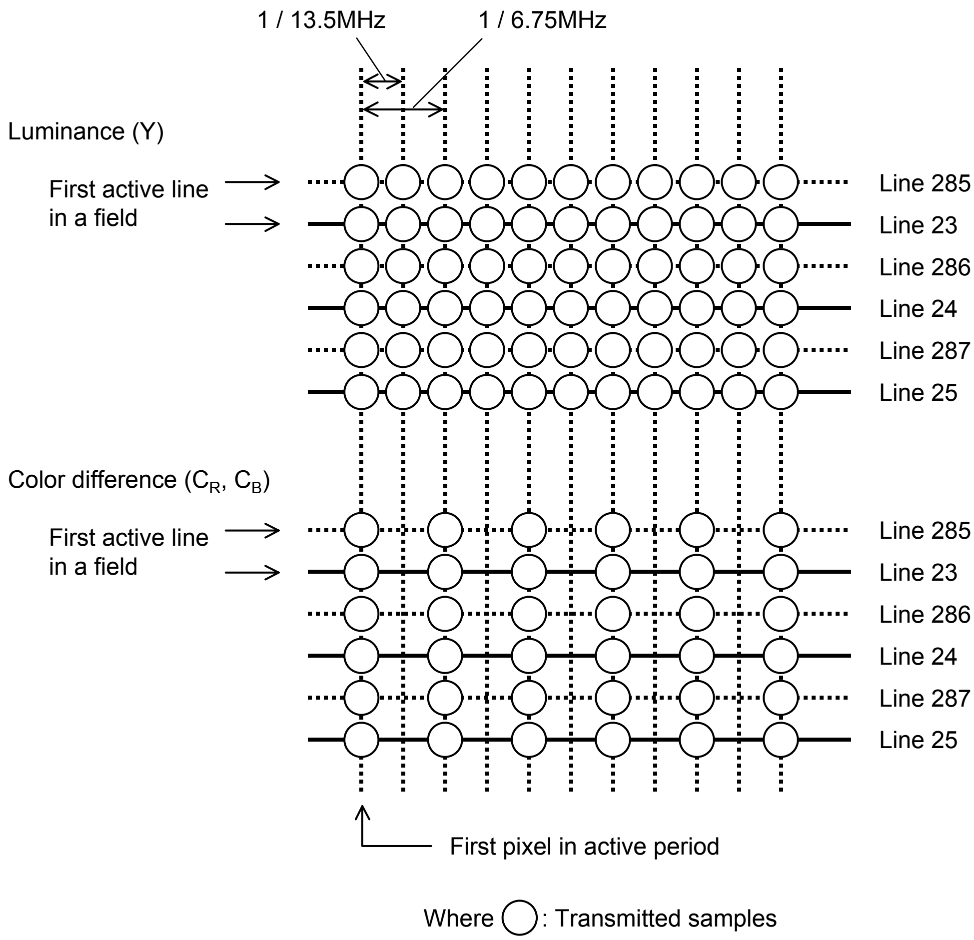


Figure 35 – Transmitted samples of 525/60 system with 4:2:2 compression

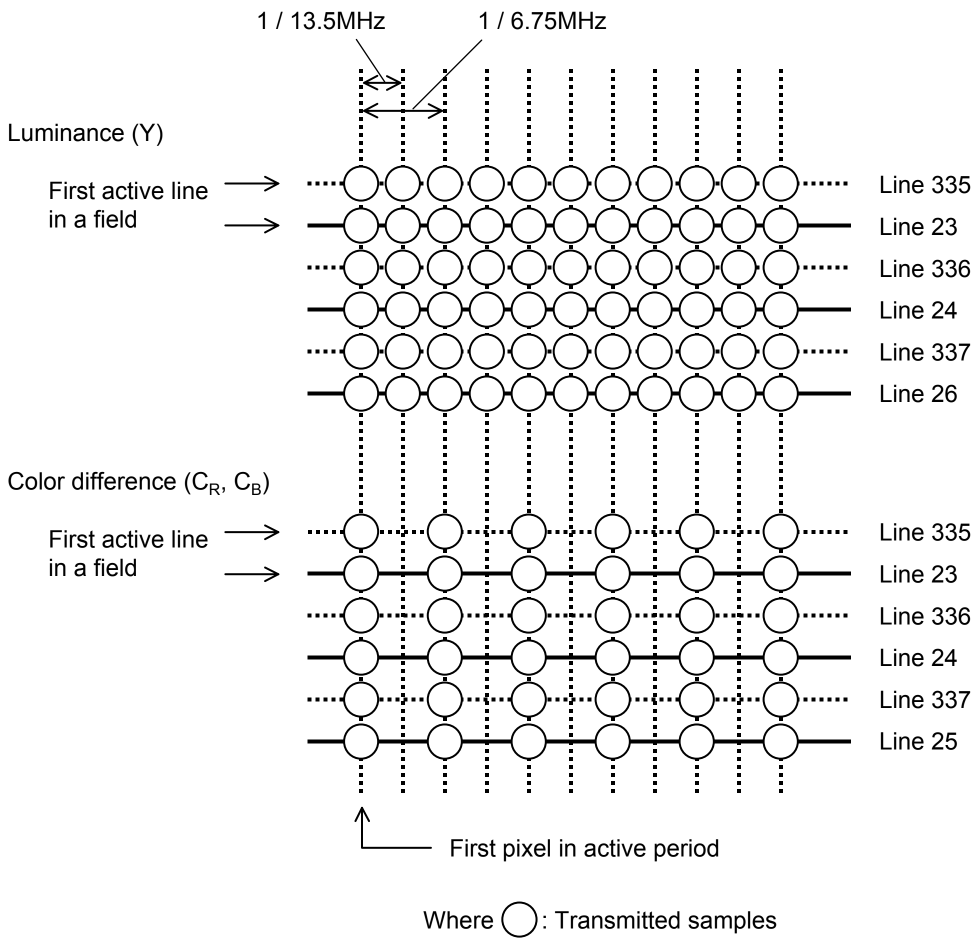


Figure 36 –Transmitted samples of 625/50 system with 4:2:2 compression

8.2.2 DCT block

The Y, C_R and C_B pixels in one frame shall be divided into DCT blocks as shown in figure 37. All DCT blocks for 4:2:2 compression, and DCT blocks for 4:1:1 compression with the exception for the rightmost DCT blocks in C_R and C_B for 4:1:1 compression, are structured as a rectangular area of eight vertical lines and eight horizontal pixels in each DCT block. The value of x shows the horizontal coordinate from the left and the value of y shows the vertical coordinate from the top. Odd lines of y = 1, 3, 5, 7 are the horizontal lines of field one, and even lines of y = 0, 2, 4, 6 are those of field two.

In 4:1:1 compression mode, the rightmost DCT blocks in C_R and C_B are structured with 16 vertical lines and four horizontal pixels. The rightmost DCT block shall be constructed of eight vertical lines and eight horizontal pixels by moving the lower part of eight vertical lines and four horizontal pixels to the higher part of eight vertical lines and four horizontal pixels as shown in figure 38.

– DCT block arrangement in one frame for 525/60 system

The arrangement of horizontal DCT blocks in each frame in 4:1:1 compression mode is shown in figure 39, and of 4:2:2 compression in figure 40. The same horizontal arrangement is repeated with 60 DCT blocks in vertical direction. Pixels in one frame are divided into to 8100 DCT blocks for 4:1:1 compression and 10800 DCT blocks for 4:2:2 compression.

4:1:1 compression

- Y: 60 vertical DCT blocks x 90 horizontal DCT blocks = 5400 DCT blocks;
- C_R: 60 vertical DCT blocks x 22.5 horizontal DCT blocks = 1350 DCT blocks;
- C_B: 60 vertical DCT blocks x 22.5 horizontal DCT blocks = 1350 DCT blocks.

4:2:2 compression

- Y: 60 vertical DCT blocks x 90 horizontal DCT blocks = 5400 DCT blocks;
- C_R: 60 vertical DCT blocks x 45 horizontal DCT blocks = 2700 DCT blocks;
- C_B: 60 vertical DCT blocks x 45 horizontal DCT blocks = 2700 DCT blocks.

– DCT block arrangement in one frame for 625/50 system

The arrangement of horizontal DCT blocks in each frame of 4:1:1 compression mode is shown in figure 39, and of 4:2:2 compression mode in figure 40. The same horizontal arrangement is repeated to 72 DCT blocks in the vertical direction. The pixels in each frame are divided into 9720 DCT blocks for 4:1:1 compression and 12960 DCT blocks for 4:2:2 compression

4:1:1 compression

- Y: 72 vertical DCT blocks x 90 horizontal DCT blocks = 6480 DCT blocks;
- C_R: 72 vertical DCT blocks x 22.5 horizontal DCT blocks = 1620 DCT blocks;
- C_B: 72 vertical DCT blocks x 22.5 horizontal DCT blocks = 1620 DCT blocks.

4:2:2 compression

- Y: 72 vertical DCT blocks x 90 horizontal DCT blocks = 6480 DCT blocks;
- C_R: 72 vertical DCT blocks x 45 horizontal DCT blocks = 3240 DCT blocks;
- C_B: 72 vertical DCT blocks x 45 horizontal DCT blocks = 3240 DCT blocks.

8.2.3 Macro block

As shown in figure 41, each macro block in the 4:1:1 compression mode consists of six DCT blocks. As shown in figure 42, each macro block in the 4:2:2 compression mode consists of four DCT blocks. In the 4:1:1 compression mode, each macro block consists of four horizontally adjacent DCT blocks of Y, one DCT block of C_R and one DCT block of C_B in the television image. The rightmost macro blocks in the television image consist of four vertically and horizontally adjacent DCT blocks of Y, one DCT block of $C_{R,}$ and one DCT block of C_B.

– Macro block arrangement in one frame for 525/60 system

The arrangement of macro blocks in one frame is shown in figure 43 for 4:1:1 compression and figure 45 for 4:2:2 compression. The small rectangle shows a macro block. Pixels in one frame are divided into 1350 macro blocks for 4:1:1 compression or 1620 macro blocks for 4:2:2 compression.

4:1:1 compression

60 vertical macro blocks x 22.5 horizontal macro blocks = 1350 macro blocks.

4:2:2 compression

60 vertical macro blocks x 45 horizontal macro blocks = 2700 macro blocks.

– Macro block arrangement in one frame for 625/50 system

The arrangement of macro blocks in one frame is shown in figure 44 for 4:1:1 compression and figure 46 for 4:2:2 compression. The small rectangle shows a macro block. Pixels in one frame are divided into 1620 macro blocks for 4:1:1 compression and 3240 macro blocks for 4:2:2 compression.

4:1:1 compression

72 vertical macro blocks x 22.5 horizontal macro blocks = 1620 macro blocks.

4:2:2 compression

72 vertical macro blocks x 45 horizontal macro blocks = 3240 macro blocks.

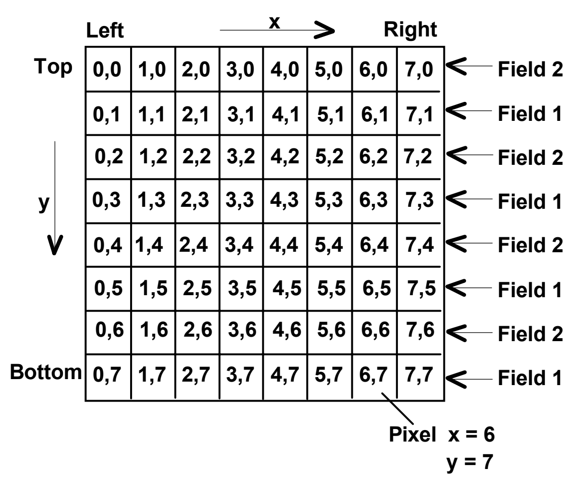


Figure 37 – DCT block and pixel coordinate

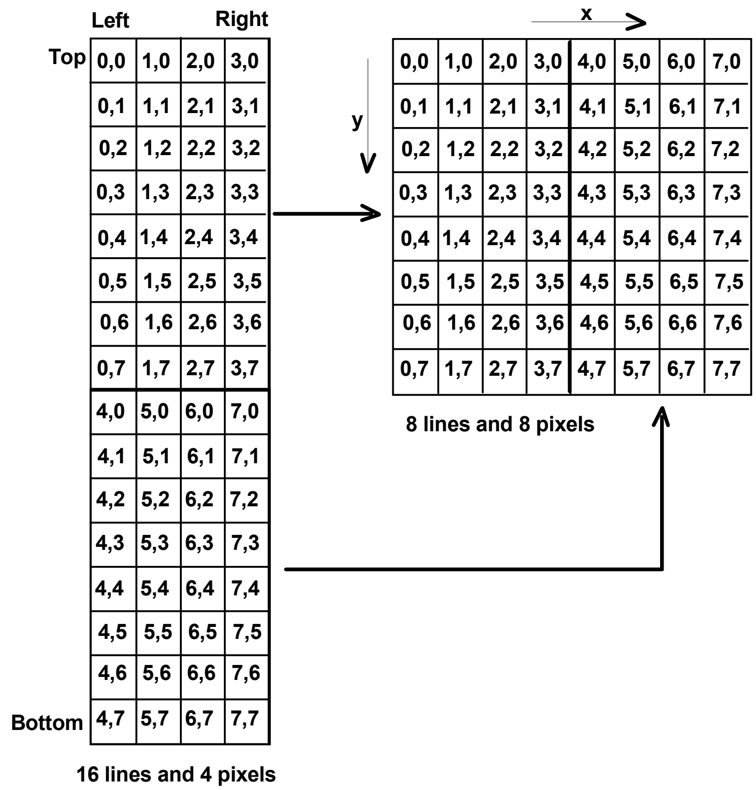


Figure 38 – Rightmost DCT block for color-difference signals

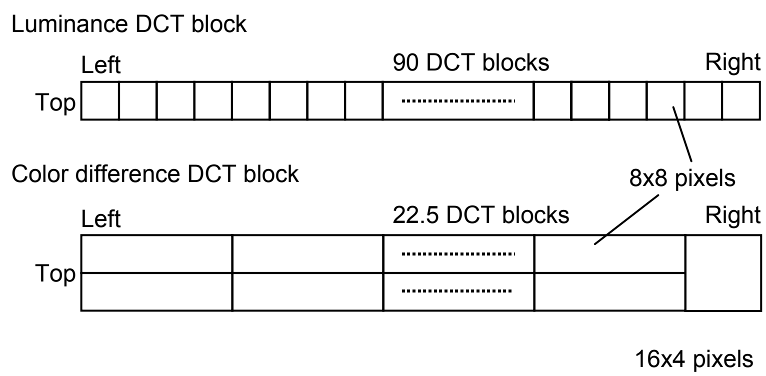


Figure 39 – DCT block arrangement with 4:1:1 compression

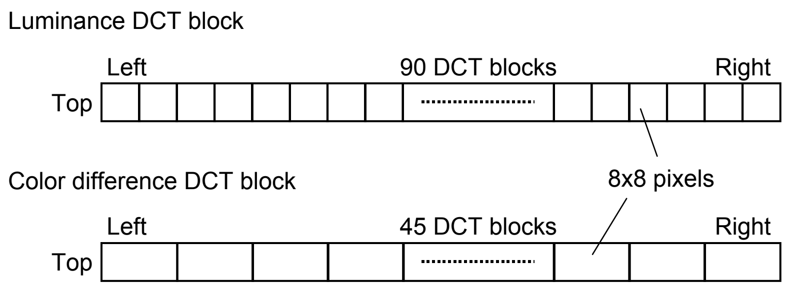
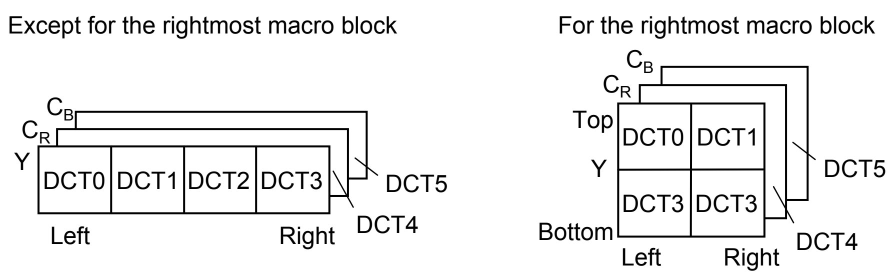
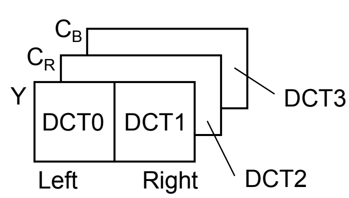


Figure 40 – DCT block arrangement with 4:2:2 compression



NOTES - DCTI: DCT block order
I = 0, 1, 2, 3, 4, 5

Figure 41 – Macro block and DCT blocks with 4:1:1 compression



NOTES - DCTI: DCT block order
I = 0, 1, 2, 3

Figure 42 – Macro block and DCT blocks with 4:2:2 compression

8.2.4 Super block

Each super block consists of 27 macro blocks.

– Super block arrangement in one frame for 525/60 system

The arrangement of super blocks in one frame is shown in figure 43 for 4:1:1 compression and figure 45 for 4:2:2 compression. Each super block consists of 27 adjacent macro blocks, and its boundary is marked by a heavy line. The total pixels in a frame are divided into 50 super blocks for 4:1:1 compression or 100 super blocks for 4:2:2 compression.

4:1:1 compression
    10 vertical super blocks x 5 horizontal super blocks = 50 super blocks.
4:2:2 compression
    20 vertical super blocks x 5 horizontal super blocks = 100 super blocks.

– Super block arrangement in one frame for 625/50 system

The arrangement of super blocks in one frame is shown in figure 44 for 4:1:1 compression and figure 46 for 4:2:2 compression. Each super block consists of 27 adjacent macro blocks, and its boundary is marked by a heavy line. The total pixels in a frame are divided into 60 super blocks for 4:1:1 compression or 120 super blocks for 4:2:2 compression.

4:1:1 compression
    12 vertical super blocks x 5 horizontal super blocks = 60 super blocks.

4:2:2 compression
    24 vertical super blocks x 5 horizontal super blocks = 120 super blocks.

8.2.5 Definition of super block number, macro block number and value of the pixel

– Super block number

The super block number in a frame is expressed as S i, j as shown in figures 43 to 46.

S i, j where i: the vertical order of the super block
    i = 0, …, n-1
    where
        n : the number of vertical super blocks in video frame
            n = 10 x m for 525/60 system
            n = 12 x m for 625/50 system
        m : the compression type
            m = 1 for 4:1:1 compression
            m = 2 for 4:2:2 compression
    j: the horizontal order of the super block
    j = 0, …, 4

– Macro block number

The macro block number is expressed as M i, j, k. The symbol k is the macro block order in the super block as shown in figure 47 for 4:1:1 compression and figure 48 for 4:2:2 compression. The small rectangle in these figures shows a macro block, and a number in the small rectangle indicates k.

M i, j, k where i, j: the super block number
k: the macro block order in the super block
k = 0, …, 26

– Pixel location

The pixel location is expressed as P i, j, k, l (x, y). The pixel is indicated as the suffix of i, j, k, l (x, y). The symbol l is the DCT block order in a macro block as shown in figures 41 and 42. The rectangle in the figure shows a DCT block, and a DCT number in the rectangle expresses l. The symbols x and y are the pixel coordinate in the DCT block as described in 8.2.2.

P i, j, k, l (x, y) where i, j, k: the macro block number
l: the DCT block order in the macro block
(x, y): the pixel coordinate in the DCT block
x = 0, …, 7
y = 0, …, 7

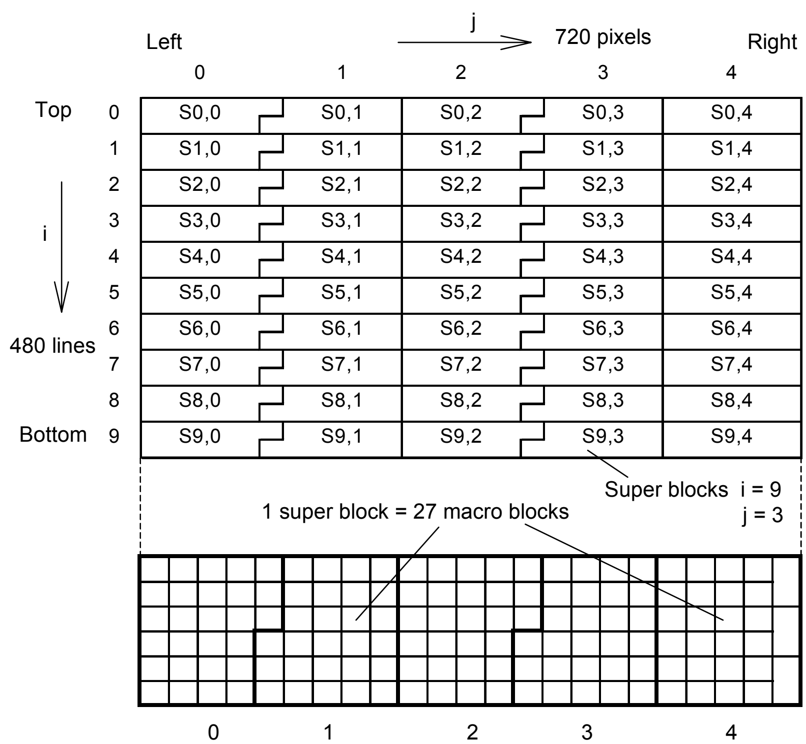


Figure 43 – Super blocks and macro blocks in one television frame for 525/60 system with 4:1:1 compression

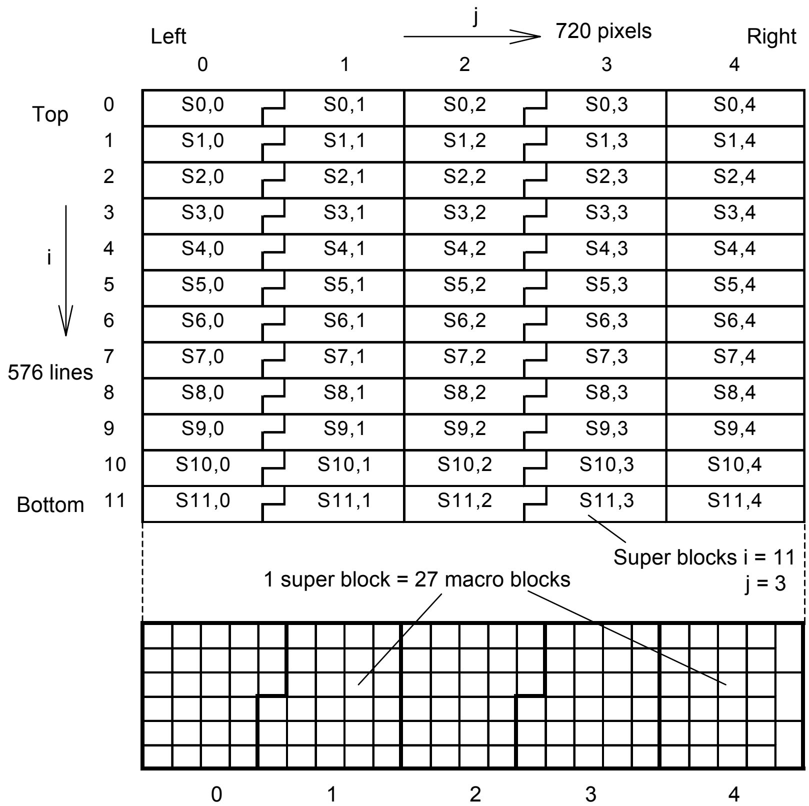
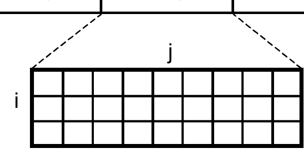


Figure 44 – Super blocks and macro blocks in one television frame for 625/50 system with 4:1:1 compression

Left → j → 720 pixels → Right

i \ j	0	1	2	3	4
Top 0	S0,0	S0,1	S0,2	S0,3	S0,4
1	S1,0	S1,1	S1,2	S1,3	S1,4
2	S2,0	S2,1	S2,2	S2,3	S2,4
3	S3,0	S3,1	S3,2	S3,3	S3,4
4	S4,0	S4,1	S4,2	S4,3	S4,4
5	S5,0	S5,1	S5,2	S5,3	S5,4
6	S6,0	S6,1	S6,2	S6,3	S6,4
7	S7,0	S7,1	S7,2	S7,3	S7,4
8	S8,0	S8,1	S8,2	S8,3	S8,4
9	S9,0	S9,1	S9,2	S9,3	S9,4
10	S10,0	S10,1	S10,2	S10,3	S10,4
480 line 11	S11,0	S11,1	S11,2	S11,3	S11,4
12	S12,0	S12,1	S12,2	S12,3	S12,4
13	S13,0	S13,1	S13,2	S13,3	S13,4
14	S14,0	S14,1	S14,2	S14,3	S14,4
15	S15,0	S15,1	S15,2	S15,3	S15,4
16	S16,0	S16,1	S16,2	S16,3	S16,4
17	S17,0	S17,1	S17,2	S17,3	S17,4
18	S18,0	S18,1	S18,2	S18,3	S18,4
Bottom 19	S19,0	S19,1	S19,2	S19,3	S19,4

Super block i = 19 j = 3



1 super block = 27 macro blocks

Figure 45 – Super blocks and macro blocks in one television frame for 525/60 system with 4:2:2 compression

Left — j → 720 pixels — Right

		0	1	2	3	4
Top	0	S0,0	S0,1	S0,2	S0,3	S0,4
	1	S1,0	S1,1	S1,2	S1,3	S1,4
	2	S2,0	S2,1	S2,2	S2,3	S2,4
	3	S3,0	S3,1	S3,2	S3,3	S3,4
	4	S4,0	S4,1	S4,2	S4,3	S4,4
i ↓	5	S5,0	S5,1	S5,2	S5,3	S5,4
	6	S6,0	S6,1	S6,2	S6,3	S6,4
	7	S7,0	S7,1	S7,2	S7,3	S7,4
	8	S8,0	S8,1	S8,2	S8,3	S8,4
	9	S9,0	S9,1	S9,2	S9,3	S9,4
	10	S10,0	S10,1	S10,2	S10,3	S10,4
	11	S11,0	S11,1	S11,2	S11,3	S11,4
576 line	12	S12,0	S12,1	S12,2	S12,3	S12,4
	13	S13,0	S13,1	S13,2	S13,3	S13,4
	14	S14,0	S14,1	S14,2	S14,3	S14,4
	15	S15,0	S15,1	S15,2	S15,3	S15,4
	16	S16,0	S16,1	S16,2	S16,3	S16,4
	17	S17,0	S17,1	S17,2	S17,3	S17,4
	18	S18,0	S18,1	S18,2	S18,3	S18,4
	19	S19,0	S19,1	S19,2	S19,3	S19,4
	20	S20,0	S20,1	S20,2	S20,3	S20,4
	21	S21,0	S21,1	S21,2	S21,3	S21,4
	22	S22,0	S22,1	S22,2	S22,3	S22,4
Bottom	23	S23,0	S23,1	S23,2	S23,3	S23,4

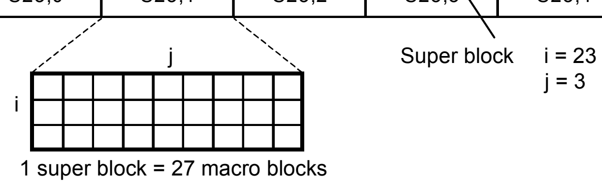


Figure 46 – Super blocks and macro blocks in one television frame for 625/50 system with 4:2:2 compression

Super block Si,0, Si,2 (i = 0, ..., n - 1)

0	11	12	23	24
1	10	13	22	25
2	9	14	21	26
3	8	15	20	
4	7	16	19	
5	6	17	18	

Super block Si,1, Si,3 (i = 0, ..., n - 1)

	8	9	20	21
	7	10	19	22
	6	11	18	23
0	5	12	17	24
1	4	13	16	25
2	3	14	15	26

Super block Si,4 (i = 0, ..., n - 1)

<table>
<tr><td>0</td><td>11</td><td>12</td><td>23</td><td rowspan="2">24</td></tr>
<tr><td>1</td><td>10</td><td>13</td><td>22</td></tr>
<tr><td>2</td><td>9</td><td>14</td><td>21</td><td rowspan="2">25</td></tr>
<tr><td>3</td><td>8</td><td>15</td><td>20</td></tr>
<tr><td>4</td><td>7</td><td>16</td><td>19</td><td rowspan="2">26</td></tr>
<tr><td>5</td><td>6</td><td>17</td><td>18</td></tr>
</table>

Where n = 10: 525/60 system
n = 12: 625/50 system

Figure 47 – Macro block order in a super block with 4:1:1 compression

Super block Si,j, (i=0, ..., n-1, j=0, ..., 4)

0	5	6	11	12	17	18	23	24
1	4	7	10	13	16	19	22	25
2	3	8	9	14	15	20	21	26

Where n = 20: 525/60 system
n = 24: 625/50 system

Figure 48 – Macro block order in a super block with 4:2:2 compression

8.2.6 Definition of video segment and compressed macro block

A video segment consists of five macro blocks assembled from various areas within the video frame:

Ma, 2, k where a = (i+2m) mod n
Mb, 1, k where b = (i+6m) mod n
Mc, 3, k where c = (i+8m) mod n
Md, 0, k where d = (i+0) mod n
Me, 4, k where e = (i+4m) mod n

where i: the vertical order of the super block
i = 0, …, n-1
n: the number of vertical super blocks in a video frame
n = 10 x m for 525/60 system
n = 12 x m for 625/50 system
m: the compression type
m = 1 for 4:1:1 compression
m = 2 for 4:2:2 compression
k: the macro block order in the super block
k = 0, …, 26

Each video segment before the bit rate reduction is expressed as Vi, k which consists of Ma, 2, k; Mb, 1, k; Mc, 3, k; Md, 0, k; and Me, 4, k.

The bit-rate reduction process is operated sequentially from Ma, 2, k to Me, 4, k. The data in a video segment are compressed and transformed to a 385-byte data stream. A compressed video data segment consists of five compressed macro blocks. Each compressed macro block consists of 77 bytes and is expressed as CM. Each video segment after the bit-rate reduction is expressed as CV i, k which consists of CMa, 2, k; CMb, 1, k; CMc, 3, k; CMd, 0, k; and CMe, 4, k as shown below:

CMa, 2, k:
This block includes all parts or most parts of the compressed data from the macro block Ma, 2, k and may include the compressed data of the macro block Mb, 1, k or Mc, 3, k or Md, 0, k or Me, 4, k.

CMb, 1, k:
This block includes all parts or most parts of the compressed data from the macro block Mb, 1, k and may include the compressed data of the macro block Ma, 2, k or Mc, 3, k or Md, 0, k or Me, 4, k.

CMc, 3, k:
This block includes all parts or most parts of the compressed data from the macro block Mc, 3, k and may include the compressed data of the macro block Ma, 2, k or Mb, 1, k or Md, 0, k or Me, 4, k.

CMd, 0, k:
This block includes all parts or most parts of the compressed data from the macro block Md, 0, k and may include the compressed data of the macro block Ma, 2, k or Mb, 1, k or Mc, 3, k or Me, 4, k.

CMe, 4, k:
This block includes all parts or most parts of the compressed data from the macro block Me, 4, k and may include the compressed data of the macro block Ma, 2, k or Mb, 1, k or Mc, 3, k or Md, 0, k.

8.3 DCT processing

A DCT block is comprised of pixels from two fields. It has a structure consisting of 4 consecutive horizontal lines and 8 pixels per line per field. A DCT block of 64 pixels, identified as i,j,k,l (x,y), is transformed into 64 coefficients identified as i,j,k,l (h,v). The value of the pixels is Pi,j,k,l (x,y) and the transformed coefficient has a value of Ci,j,k,l. When h = 0 and v = 0, the coefficient is called a DC coefficient. Other coefficients are called AC coefficients.

8.3.1 DCT mode

Two modes, 8-8 DCT and 2-4-8 DCT, are selectively used to optimize the data-reduction process, depending upon the degree of content variation between the two fields of a video frame. Two DCT mode are defined:

8-8 DCT mode

DCT:

$$C, i, j, k, l\,(h, v) = C(v)\,C(h) \sum_{y=0}^{7} \sum_{x=0}^{7} (P\, i, j, k, l\,(x, y)\ \ COS(\pi v(2y + 1) / 16)\ \ COS(\pi h(2x + 1) / 16))$$

Inverse DCT:

$$P, i, j, k, l\,(x, y) = \sum_{v=0}^{7} \sum_{h=0}^{7} (C(v)\,C(h)\,C\, i, j, k, l\,(h, v)\ \ COS(\pi v(2y + 1) /16)\ \ COS(\pi h(2x + 1) / 16))$$

where:

$C(h) = 0, 5 / \sqrt{2}$ for h = 0
$C(h) = 0, 5$ for h = 1 to 7
$C(v) = 0, 5 / \sqrt{2}$ for v = 0
$C(v) = 0, 5$ for v = 1 to 7

2-4-8 DCT mode

DCT:

$$C\, i, j, k, l\,(h, u) = C(u)\,C(h) \sum_{z=0}^{3} \sum_{x=0}^{7} ((P\, i, j, k, l\,(x, 2z) + P\, i, j, k, l\,(x, 2z + 1))\, KC)$$

$$C\, i, j, k, l\,(h, u + 4) = C(u)\,C(h) \sum_{z=0}^{3} \sum_{x=0}^{7} ((P\, i, j, k, l\,(x, 2z) - P\, i, j, k, l\,(x, 2z + 1))\, KC)$$

Inverse DCT:

$$P\, i, j, k, l\,(x, 2z) = \sum_{u=0}^{3} \sum_{h=0}^{7} (C(u)\,C(h)\,(C\, i, j, k, l\,(h, u) + C\, i, j, k, l\,(h, u + 4))\, KC)$$

$$P\, i, j, k, l\,(x, 2z + 1) = \sum_{u=0}^{3} \sum_{h=0}^{7} (C(u)\,C(h)\,(C\, i, j, k, l\,(h, u) - C\, i, j, k, l\,(h, u + 4))\, KC)$$

where

$u = 0, \ldots, 3$
$z = INT(y / 2)$
$KC = COS(\pi u(2z + 1) / 8)\ COS(\pi h(2x + 1) / 16)$
$C(h) = 0, 5 / \sqrt{2}$ for h = 0
$C(h) = 0, 5$ for h = 1 to 7
$C(u) = 0, 5 / \sqrt{2}$ for u = 0
$C(u) = 0, 5$ for u = 1 to 7

8.3.2 Weighting

DCT coefficients shall be weighted by the process described below. W(h, v) expresses weight for C i, j, k, l (h, v) of the DCT coefficient.

8-8 DCT mode

For h = 0 and v = 0 $W(h, v) = 1 / 4$
For others $W(h, v) = w(h)\, w(v) / 2$

2-4-8 DCT mode

For h = 0 and v = 0 $W(h, v) = 1 / 4$
For v < 4 $W(h, v) = w(h)\, w(2 v) / 2$
For others $W(h, v) = w(h)\, w(2 (v - 4)) / 2$

where

$w(0) = 1$
$w(1) = CS4 / (4 \times CS7 \times CS2)$
$w(2) = CS4 / (2 \times CS6)$
$w(3) = 1 / (2 \times CS5)$
$w(4) = 7 / 8$
$w(5) = CS4 / CS3$
$w(6) = CS4 / CS2$
$w(7) = CS4 / CS1$

where

$CSm = COS(m\pi /16)$ m = 1 to 7

8.3.3 Output order

Figure 49 shows the output order of the weighted coefficients.

8-8-DCT (horizontal →, Vertical ↓)

	0	1	2	3	4	5	6	7
0	1	2	6	7	15	16	28	29
1	3	5	8	14	17	27	30	43
2	4	9	13	18	26	31	42	44
3	10	12	19	25	32	41	45	54
4	11	20	24	33	40	46	53	55
5	21	23	34	39	47	52	56	61
6	22	35	38	48	51	57	60	62
7	36	37	49	50	58	59	63	64

2-4-8-DCT (horizontal →, Vertical ↓; rows 0–3 (sum), rows 4–7 (difference))

	0	1	2	3	4	5	6	7
0	1	3	7	19	21	35	37	51
1	5	9	17	23	33	39	49	53
2	11	15	25	31	41	47	55	61
3	13	27	29	43	45	57	59	63
4	2	4	8	20	22	36	38	52
5	6	10	18	24	34	40	50	54
6	12	16	26	32	42	48	56	62
7	14	28	30	44	46	58	60	64

Figure 49 – Output order of a weighted DCT block

8.3.4 Tolerance of DCT with weighting

Output error between the reference DCT and the tested DCT should satisfy the tolerances of the following cases:

- Probability of occurrence of error;
- Mean square errors for all coefficients;
- Maximum value of mean square error for each DCT block;
- All input pixel values of a DCT block are the same.

8.4 Quantization

8.4.1 Introduction

Weighted DCT coefficients are first quantized to 9-bit words, then divided by the quantization step in order to limit the amount of data in one video segment to five compressed macro blocks.

8.4.2 Bit assignment for quantization

Weighted DCT coefficients are represented as follows:

DC coefficient value (9 bits):	b8 b7 b6 b5 b4 b3 b2 b1 b0 twos complement (-255 to 255)
AC coefficient value (10 bits):	s b8 b7 b6 b5 b4 b3 b2 b1 b0 1 sign bit + 9 bits of absolute value (-511 to 511)

8.4.3 Class number

Each DCT block shall be classified into four classes by the definitions described in table 38. For selecting the quantization step, the class number is used. Both c1 and c0 express the class number and are stored in the DC coefficient of the compressed DCT block, as described in 8.6. For reference, table 39 shows an example of the classification.

8.4.4 Initial scaling

Initial scaling is an operation for AC coefficients to transform from 10 bits to 9 bits. Initial scaling shall be done as follows:

For class number = 0, 1, 2

input data: s b8 b7 b6 b5 b4 b3 b2 b1 b0
output data: s b7 b6 b5 b4 b3 b2 b1 b0

For class number = 3

input data: s b8 b7 b6 b5 b4 b3 b2 b1 b0
output data: s b8 b7 b6 b5 b4 b3 b2 b1

8.4.5 Area number

The area number is used for selection of the quantization step. AC coefficients within a DCT block shall be classified into four areas with the area numbers as shown in figure 50.

Table 38 – Class number and DCT block

Class number			DCT block	
	c1	c0	Quantization noises	Maximum absolute value of AC coefficient
0	0	0	visible	Less than or equal to 255
1	0	1	Lower than class 0	
2	1	0	Lower than class 1	
3	1	1	Lower than class 2	
			———	Greater than 255

Table 39 – Example of the classification for reference

	Maximum absolute value of AC coefficient			
	0 to 11	12 to 23	24 to 35	> 35
Y	0	1	2	3
C_R	1	2	3	3
C_B	2	3	3	3

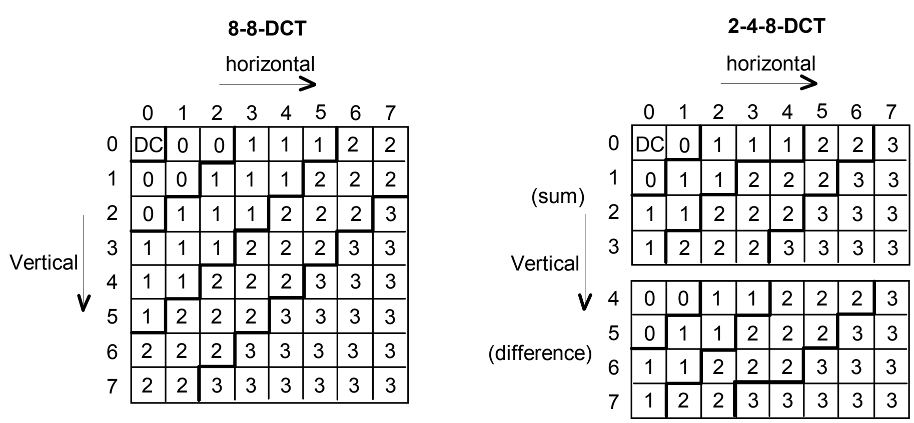


Figure 50 – Area numbers

8.4.6 Quantization step

The quantization step shall be decided by the class number, area number, and quantization number (QNO) as specified in table 40. QNO is selected in order to limit the amount of data in one video segment to five compressed macro blocks.

Table 40 – Quantization step

	Class number				Area number			
	0	1	2	3	0	1	2	3
Quantization number (QNO)	15				1	1	1	1
	14				1	1	1	1
	13				1	1	1	1
	12	15			1	1	1	1
	11	14			1	1	1	1
	10	13		15	1	1	1	1
	9	12	15	14	1	1	1	1
	8	11	14	13	1	1	1	2
	7	10	13	12	1	1	2	2
	6	9	12	11	1	1	2	2
	5	8	11	10	1	2	2	4
	4	7	10	9	1	2	2	4
	3	6	9	8	2	2	4	4
	2	5	8	7	2	2	4	4
	1	4	7	6	2	4	4	8
	0	3	6	5	2	4	4	8
		2	5	4	4	4	8	8
		1	4	3	4	4	8	8
		0	3	2	4	8	8	16
			2	1	4	8	8	16
			1	0	8	8	16	16
			0		8	8	16	16

8.5 Variable length coding (VLC)

Variable length coding is an operation for transforming quantized AC coefficients to variable length codes. One or some successive AC coefficients within a DCT block are coded into one variable length code according to the order as shown in figure 49. Run length and amplitude are defined as follows:

Run length: The number of successive AC coefficients quantized to 0 (run = 0, … 61);
Amplitude: Absolute value just after successive AC coefficients quantized to 0 (amp = 0, … 255);
(run, amp): The pair of run length and amplitude.

Table 41 shows the length of codewords corresponding to (run, amp). In the table, the sign bit is not included in the length of the codewords. When the amplitude is not zero, the code length shall be plus 1, because sign bit is needed. For empty columns, the length of codewords of the (run, amp) equals that of the (run-1, 0) plus that of the (0, amp).

The code of the variable length coding shall be as shown in table 42. The leftmost bit of codewords is MSB and the rightmost bit of codewords is LSB in table 42. The MSB of the subsequent codeword is next to the LSB of the codeword just before. The sign bit s shall be as follows:

– For the quantized AC coefficient greater than zero: s = 0;
– For the quantized AC coefficient less than zero: s = 1.

When the value of all remaining quantized coefficients is zero within a DCT block, the coding process is ended by adding an EOB (End of block) codeword of 0110b just after the last codeword.

Table 41 – Length of codewords

	Amplitude																									
Run length	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	....	255
0	11	2	3	4	4	5	5	6	6	7	7	7	8	8	8	8	8	8	9	9	9	9	9	15	....	15
1	11	4	5	7	7	8	8	8	9	10	10	10	11	11	11	12	12	12								
2	12	5	7	8	9	9	10	12	12	12	12	12														
3	12	6	8	9	10	10	11	12																		
4	12	6	8	9	11	12																				
5	12	7	9	10																						
6	13	7	9	11																						
7	13	8	12	12																						
8	13	8	12	12																						
9	13	8	12																							
10	13	8	12																							
11	13	9																								
12	13	9																								
13	13	9																								
14	13	9																								
15	13																									
⋮	⋮																									
61	13																									

NOTES

1 Sign bit is not included.
2 The length of EOB = 4.

Table 42 – Codewords of variable length coding

(run,	amp)	Code	Length
0	1	0 0 s	2+1
0	2	0 1 0 s	3+1
EOB		0 1 1 0	4
1	1	0 1 1 1 s	4+1
0	3	1 0 0 0 s	
0	4	1 0 0 1 s	
2	1	1 0 1 0 0 s	5+1
1	2	1 0 1 0 1 s	
0	5	1 0 1 1 0 s	
0	6	1 0 1 1 1 s	
3	1	1 1 0 0 0 0 s	6+1
4	1	1 1 0 0 0 1 s	
0	7	1 1 0 0 1 0 s	
0	8	1 1 0 0 1 1 s	
5	1	1 1 0 1 0 0 0 s	7+1
6	1	1 1 0 1 0 0 1 s	
2	2	1 1 0 1 0 1 0 s	
1	3	1 1 0 1 0 1 1 s	
1	4	1 1 0 1 1 0 0 s	
0	9	1 1 0 1 1 0 1 s	
0	10	1 1 0 1 1 1 0 s	
0	11	1 1 0 1 1 1 1 s	
7	1	1 1 1 0 0 0 0 0 s	8+1
8	1	1 1 1 0 0 0 0 1 s	
9	1	1 1 1 0 0 0 1 0 s	
10	1	1 1 1 0 0 0 1 1 s	
3	2	1 1 1 0 0 1 0 0 s	
4	2	1 1 1 0 0 1 0 1 s	
2	3	1 1 1 0 0 1 1 0 s	
1	5	1 1 1 0 0 1 1 1 s	
1	6	1 1 1 0 1 0 0 0 s	
1	7	1 1 1 0 1 0 0 1 s	
0	12	1 1 1 0 1 0 1 0 s	
0	13	1 1 1 0 1 0 1 1 s	
0	14	1 1 1 0 1 1 0 0 s	
0	15	1 1 1 0 1 1 0 1 s	
0	16	1 1 1 0 1 1 1 0 s	
0	17	1 1 1 0 1 1 1 1 s	
11	1	1 1 1 1 0 0 0 0 0 s	9+1
12	1	1 1 1 1 0 0 0 0 1 s	
13	1	1 1 1 1 0 0 0 1 0 s	
14	1	1 1 1 1 0 0 0 1 1 s	
5	2	1 1 1 1 0 0 1 0 0 s	
6	2	1 1 1 1 0 0 1 0 1 s	
3	3	1 1 1 1 0 0 1 1 1 s	
4	3	1 1 1 1 0 0 1 1 1 s	
2	4	1 1 1 1 0 1 0 0 0 s	
2	5	1 1 1 1 0 1 0 0 1 s	
1	8	1 1 1 1 0 1 0 1 0 s	
0	18	1 1 1 1 0 1 0 1 1 s	
0	19	1 1 1 1 0 1 1 0 0 s	
0	20	1 1 1 1 0 1 1 0 1 s	
0	21	1 1 1 1 0 1 1 1 0 s	
0	22	1 1 1 1 0 1 1 1 1 s	
5	3	1 1 1 1 1 0 0 0 0 0 s	10+1
3	4	1 1 1 1 1 0 0 0 0 1 s	
3	5	1 1 1 1 1 0 0 0 1 0 s	
2	6	1 1 1 1 1 0 0 0 1 1 s	
1	9	1 1 1 1 1 0 0 1 0 0 s	
1	10	1 1 1 1 1 0 0 1 0 1 s	
1	11	1 1 1 1 1 0 0 1 1 0 s	
0	0	1 1 1 1 1 0 0 1 1 1 0	11
1	0	1 1 1 1 1 0 0 1 1 1 1	
6	3	1 1 1 1 1 0 1 0 0 0 0 s	11+1
4	4	1 1 1 1 1 0 1 0 0 0 1 s	
3	6	1 1 1 1 1 0 1 0 0 1 0 s	
1	12	1 1 1 1 1 0 1 0 0 1 1 s	
1	13	1 1 1 1 1 0 1 0 1 0 0 s	
1	14	1 1 1 1 1 0 1 0 1 0 1 s	
2	0	1 1 1 1 1 0 1 0 1 1 0 0	12
3	0	1 1 1 1 1 0 1 0 1 1 0 1	
4	0	1 1 1 1 1 0 1 0 1 1 1 0	
5	0	1 1 1 1 1 0 1 0 1 1 1 1	
7	2	1 1 1 1 1 0 1 1 0 0 0 0 s	12+1
8	2	1 1 1 1 1 0 1 1 0 0 0 1 s	
9	2	1 1 1 1 1 0 1 1 0 0 1 0 s	
10	2	1 1 1 1 1 0 1 1 0 0 1 1 s	
7	3	1 1 1 1 1 0 1 1 0 1 0 0 s	
8	3	1 1 1 1 1 0 1 1 0 1 0 1 s	
4	5	1 1 1 1 1 0 1 1 0 1 1 0 s	
3	7	1 1 1 1 1 0 1 1 0 1 1 1 s	
2	7	1 1 1 1 1 0 1 1 1 0 0 0 s	
2	8	1 1 1 1 1 0 1 1 1 0 0 1 s	
2	9	1 1 1 1 1 0 1 1 1 0 1 0 s	
2	10	1 1 1 1 1 0 1 1 1 0 1 1 s	
2	11	1 1 1 1 1 0 1 1 1 1 0 0 s	
1	15	1 1 1 1 1 0 1 1 1 1 0 1 s	
1	16	1 1 1 1 1 0 1 1 1 1 1 0 s	
1	17	1 1 1 1 1 0 1 1 1 1 1 1 s	
6	0	1 1 1 1 1 1 0 0 0 0 1 1 0	13
7	0	1 1 1 1 1 1 0 0 0 0 1 1 1	
R	0	1 1 1 1 1 1 0 Binary notation of R, R = 6 to 61	
61	0	1 1 1 1 1 1 0 1 1 1 1 0 1	
0	23	1 1 1 1 1 1 1 0 0 0 1 0 1 1 1 s	15+1
0	24	1 1 1 1 1 1 1 0 0 0 1 1 0 0 0 s	
0	A	1 1 1 1 1 1 1 Binary notation of A, A = 23 to 255 s	
0	255	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 s	

NOTES

1 (R, 0) : 1 1 1 1 1 1 0 r5 r4 r3 r2 r1 r0,
where 32r5 + 16r4 + 8r3 + 4r2 + 2r1 + r0 = R.

2 (0, A) : 1 1 1 1 1 1 1 a7 a6 a5 a4 a3 a2 a1 a0 s,
where 128a7 + 64a6 + 32a5 + 16a4 + 8a3 + 4a2 + 2a1 + a0 = A.

3 S is sign bit. EOB means End of block.

8.6 Arrangement of a compressed macro block

A compressed video segment consists of five compressed macro blocks. Each compressed macro block has 77 bytes of data. The arrangement of the compressed macro block shall be as shown in figure 51 for the 4:1:1 compression and figure 52 for the 4:2:2 compression.

STA (status of the compressed macro block)

STA expresses the error and concealment of the compressed macro blcok and consists of four bits: s3, s2, s1, s0. Table 44 shows the definition of STA.

QNO (quantization number)

QNO is the quantization number applied to the macro block. Code words of the QNO shall be as shown in table 43.

DC

DCI (where l is the DCT block order in the macro block, l = 0, …, 5 for 4:1:1 compression, l = 0, …, 3 for 4:2:2 compression) consists of a DC coefficient, the DCT mode, and the class number of the DCT block.

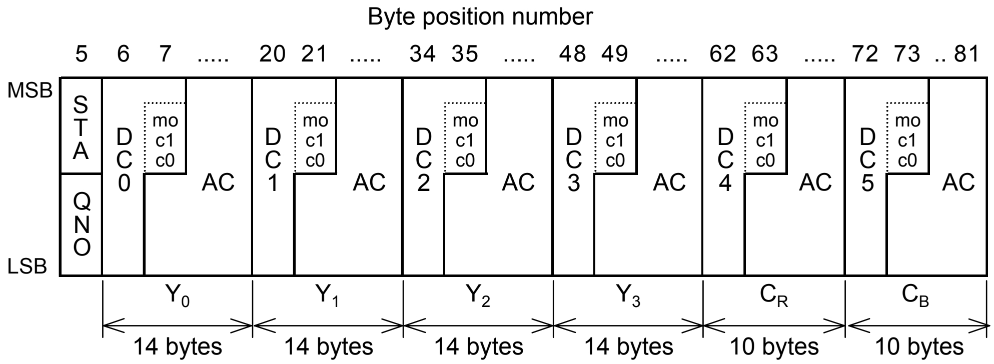
```
       MSB                                      LSB
DCI:  b8  b7  b6  b5  b4  b3  b2  b1  b0  mo  c1  c0
```

where

b8 to b0:	DC coefficient value	
mo:	DCT mode	mo = 0 for 8-8-DCT mode, mo = 1 for 2-4-8-DCT mode
c1 c0:	class number	

AC

AC is a generic term for variable length coded AC coefficients within the video segment Vi, k. For 4:1:1 compression, the areas of Y0, Y1, Y2, Y3, C_R and C_B are defined as compressed-data areas and each of Y0, Y1, Y2 and Y3 consists of 112 bits and each C_R and C_B consists of 80 bits as shown in figure 51. For 4:2:2 compression, the areas of Y0, Y1, C_R and C_B are defined as compressed-data areas and each of Y0 and Y1 consists of 112 bits and each C_R and C_B consists of 80 bits as shown in figure 52. DCI and variable length code for AC coefficients in the DCT block whose DCT block number is i, j, k, l are assigned from the beginning of the compressed data area in the compressed macro block CM i, j, k. In figures 51 and 52, the variable length codeword is located starting from MSB which is shown in the upper and left side, and LSB is shown in the lower and right side. Therefore, AC data are distributed from the upper left corner to the lower right corner.



NOTES
STA: Error status
QNO: Quantization number
DC: DC component
AC: AC component
EOB: End of block (0110)
mo: DCT mode
c0, c1: class number

Figure 51 – Arrangement of a compressed macro block with 4:1:1 compression

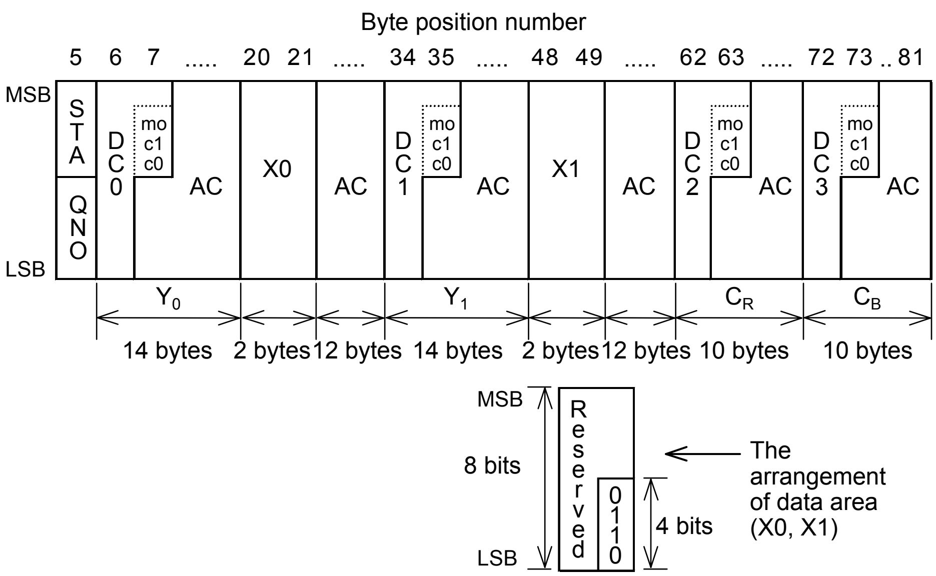


Figure 52 – Arrangement of a compressed macro block with 4:2:2 compression

Table 43 - Codewords of the QNO

q3	q2	q1	q0	QNO
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	11
1	1	0	0	12
1	1	0	1	13
1	1	1	0	14
1	1	1	1	15

Table 44 – Definition of STA

STA				Information of the compressed macro block		
s3	s2	s1	s0	Error	Error concealment	Continuity
0	0	0	0	No error	Not proceeded	————
0	0	1	0		Type A	Type a
0	1	0	0		Type B	
0	1	1	0		Type C	
0	1	1	1	Error exists	————	————
1	0	1	0	No error	Type A	Type b
1	1	0	0		Type B	
1	1	1	0		Type C	
1	1	1	1	Error exists	————	————
Others				Reserved		

NOTES
1 Type A: Replaced with a compressed macro block of the same compressed macro block number in the immediate previous frame.
2 Type B: Replaced with a compressed macro block of the same compressed macro block number in the next immediate frame.
3 Type C: This compressed macro block is concealed, but the concealment method is not specified.
4 Type a: The continuity of the data processing sequence with other compressed macro blocks whose s0 = 0 and s3 = 0 in the same video segment is guaranteed.
5 Type b: The continuity of the data processing sequence with another compressed macro block is not guaranteed.
6 For STA = 0111b, the error code is inserted in the compressed macro block. This is an option.
7 For STA = 1111b, the error position is unidentified.

8.7 Arrangement of a video segment

In this clause, the distribution method of quantized AC coefficients is described. Figures 53 and 54 shows the arrangement of a video segment CV i, k after bit-rate reduction. The column shows a compressed macro block, and symbol F i, j, k, l expresses the compressed data area for a DCT block whose DCT block number is i, j, k, l.

In the bit sequence which links together the DC mode information and the class number, the AC coefficient codeword for the DCT block i,j,k,l is shown as Bi,j,k,l. Codewords for AC coefficients of B i, j, k, l shall be concatenated according to the order as shown in figure 49 and the last codeword shall be EOB. The MSB of the subsequent codeword shall be next to the LSB of the codeword just before.

Byte position number

Compressed macro block number	5	6	20	34	48	62	72 ... 81
CM a, 2, k	STA a / QNO a	F a, 2, k, 0	F a, 2, k, 1	F a, 2, k, 2	F a, 2, k, 3	F a, 2, k, 4	F a, 2, k, 5
CM b, 1, k	STA b / QNO b	F b, 1, k, 0	F b, 1, k, 1	F b, 1, k, 2	F b, 1, k, 3	F b, 1, k, 4	F b, 1, k, 5
CM c, 3, k	STA c / QNO c	F c, 3, k, 0	F c, 3, k, 1	F c, 3, k, 2	F c, 3, k, 3	F c, 3, k, 4	F c, 3, k, 5
CM d, 0, k	STA d / QNO d	F d, 0, k, 0	F d, 0, k, 1	F d, 0, k, 2	F d, 0, k, 3	F d, 0, k, 4	F d, 0, k, 5
CM e, 4, k	STA e / QNO e	F e, 4, k, 0	F e, 4, k, 1	F e, 4, k, 2	F e, 4, k, 3	F e, 4, k, 4	F e, 4, k, 5
		Y0 14 bytes	Y1 14 bytes	Y2 14 bytes	Y3 14 bytes	C_R 10 bytes	C_B 10 bytes

NOTES

a = (i+2) mod n
b = (i+6) mod n
c = (i+8) mod n
d = (i+0) mod n
e = (i+4) mod n

i: the vertical order of the super block
i = 0, …, n-1
n: the number of vertical super block in a video frame
n = 10 for 525/60 system
n = 12 for 625/50 system
k: the macro block order in the super block
k = 0,…, 26

Figure 53 – Arrangement of a video segment after the bit-rate reduction with 4:1:1 compression

Compressed macro block number	5	6 …	20 …	34 …	48 …	62 …	72 … 81
CM a, 2, k	STAa / QNOa	F a, 2, k, 0	E a, 2, k, 1	F a, 2, k, 1	E a, 2, k, 1	F a, 2, k, 2	F a, 2, k, 3
CM b, 1, k	STAb / QNOb	F b, 1, k, 0	E b, 1, k, 1	F b, 1, k, 1	E b, 1, k, 1	F b, 1, k, 2	F b, 1, k, 3
CM c, 3, k	STAc / QNOc	F c, 3, k, 0	E c, 3, k, 1	F c, 3, k, 1	E c, 3, k, 1	F c, 3, k, 2	F c, 3, k, 3
CM d, 0, k	STAd / QNOd	F d, 0, k, 0	E d, 0, k, 1	F d, 0, k, 1	E d, 0, k, 1	F d, 0, k, 2	F d, 0, k, 3
CM e, 4, k	STAe / QNOe	F e, 4, k, 0	E e, 4, k, 1	F e, 4, k, 1	E e, 4, k, 1	F e, 4, k, 2	F e, 4, k, 3
		Y0		Y1		C_R	C_B
		14 bytes	14 bytes	14 bytes	14 bytes	10 bytes	10 bytes

Byte position number

NOTES

a = (i + 4) mod n
b = (i +12) mod n
c = (i +16) mod n
d = (i + 0) mod n
e = (i + 8) mod n

i : the vertical order of the super block
i = 0, …, n-1
n : the number of vertical super block in a video frame
n = 20 for 525/60 system
n = 24 for 625/50 system
k : the macro block order in the super block
k = 0,…, 26

Figure 54 – Arrangement of a video segment after the bit-rate reduction with 4:2:2 compression

The arrangement algorithm of a video segment shall be composed of three passes:

– Pass 1: The distribution of B i, j, k, l to the compressed-data area;

– Pass 2: The distribution of the B i, j, k, l which cannot be contained within the original compressed-data area after the pass 1 operation;

– Pass 3: The distribution of the excess B i, j, k, l after the pass 2 operation.

Distribution of all excess Bi,j,k,l data must be contained within the original video segment boundary. Any excess data beyond pass 3 shall be discarded.

Arrangement algorithm of a video segment

```
4:1:1 compression
        if (525/60 system) n = 10 else n = 12;
        for(i = 0;  i < n;  i ++) {
             a = (i + 2) mod n;
             b = (i + 6) mod n;
             c = (i + 8) mod n;
             d = (i + 0) mod n;
             e = (i + 4) mod n;
             for (k = 0;  k < 27; k ++) {
                   q = 2;
                   p = a;
                   VR = 0;
                   /* VR is the bit sequence for the data                                              */
                   /*    which are not distributed to video segment CV i, k by pass 2. */
/* pass 1 */
                    for(j = 0;  j < 5; j ++) {
                          MRq = 0;
                  /* MRq is the bit sequence for the data                                             */
                  /*    which are not distributed to macro block M i, q, k by pass 1.    */
                    for(l = 0;  l < 6; l ++) {
                          remain = distribute (B p, q, k, l,  F p, q, k, l);
                          MRq = connect (MRq,  remain);
                   }
                           if (q == 2)  {q = 1;  p = b;}
                   else if (q == 1)  {q = 3;  p = c;}
                   else if (q == 3)  {q = 0;  p = d;}
                   else if (q == 0)  {q = 4;  p = e;}
                   else if (q == 4)  {q = 2;  p = a;}
                   }
/* pass 2 */
                    for(j = 0;  j < 5; j ++) {
                        for(l = 0;  l < 6; l ++) {
                          MRq = distribute (MRq,  F p, q, k, l);
                        }
                        VR = connect (VR,  MRq);
                               if (q == 2)  {q = 1;  p = b;}
                       else if (q == 1)  {q = 3;  p = c;}
                       else if (q == 3)  {q = 0;  p = d;}
                       else if (q == 0)  {q = 4;  p = e;}
                       else if (q == 4)  {q = 2;  p = a;}
                   }
/* pass 3 */
                    for(j = 0;  j < 5; j ++) {
                        for(l = 0;  l < 6; l ++) {
                             VR = distribute (VR,  F p, q, k, l);
                        }
                                if (q == 2)  {q = 1;  p = b;}
                        else if (q == 1)  {q = 3;  p = c;}
                        else if (q == 3)  {q = 0;  p = d;}
                        else if (q == 0)  {q = 4;  p = e;}
                        else if (q == 4)  {q = 2;  p = a;}
                        }
                   }
             }
```

```
4:2:2 compression
    if (525/60 system) n = 20 else n = 24;
    for(i = 0;  i < n;  i ++) {
        a = (i +   4) mod n;
        b = (i + 12) mod n;
        c = (i + 16) mod n;
        d = (i +   0) mod n;
        e = (i +   8) mod n;
        for (k = 0;  k < 27; k ++) {
            q = 2;
            p = a;
            VR = 0;
            /* VR is the bit sequence for the data                                  */
            /*    which are not distributed to video segment CV i, k by pass 2.   */
    /* pass 1 */
            for(j = 0;  j < 5; j ++) {
                MRq = 0;
                /* MRq is the bit sequence for the data                               */
                /*    which are not distributed to macro block M i, q, k by pass 1. */
                for(l = 0;  l < 4; l ++) {
                    remain = distribute (B p, q, k, l,  F p, q, k, l);
                    MRq = connect (MRq,  remain);
                }
                      if (q == 2)  {q = 1;  p = b;}
                else if (q == 1)  {q = 3;  p = c;}
                else if (q == 3)  {q = 0;  p = d;}
                else if (q == 0)  {q = 4;  p = e;}
                else if (q == 4)  {q = 2;  p = a;}
            }
    /* pass 2 */
            for(j = 0;  j < 5; j ++) {
                for(l = 0;  l < 4; l ++) {
                    MRq = distribute (MRq,  F p, q, k, l);
                    if( (l == 0) || (l == 1) )
                        MRq = distribute (MRq,  E p, q, k, l);
                }
                VR = connect (VR,  MRq);
                      if (q == 2)  {q = 1;  p = b;}
                else if (q == 1)  {q = 3;  p = c;}
                else if (q == 3)  {q = 0;  p = d;}
                else if (q == 0)  {q = 4;  p = e;}
                else if (q == 4)  {q = 2;  p = a;}
            }
    /* pass 3 */
            for(j = 0;  j < 5; j ++) {
                for(l = 0;  l < 4; l ++) {
                    VR = distribute (VR,  F p, q, k, l);
                    if( (l == 0) || (l == 1) )
                        VR = distribute (VR,  E p, q, k, l);
                }
                      if (q == 2)  {q = 1;  p = b;}
                else if (q == 1)  {q = 3;  p = c;}
                else if (q == 3)  {q = 0;  p = d;}
                else if (q == 0)  {q = 4;  p = e;}
                else if (q == 4)  {q = 2;  p = a;}
            }
```

```
        }
    }
```

where

```
distribute (data 0 ,  area 0 ) {    /* Distribute data 0 from MSB into empty area of area 0.    */
                                    /* Area 0 is filled starting from the MSB.                  */
  remain = (remaining_data);        /* Remaining_data are the data which are not distributed.  */
  return (remain);
}
connect (data 1 ,  data 2 ) {       /* Connect the MSB of data 2 with the LSB of data 1.        */
    data 3 = (connecting_data);     /* Connecting_data are the data which are connected.        */
                                    /* data 2 with data 1.                                      */
  return (data 3);
}
```

The remaining data which cannot be distributed within the unused space of the macro block will be ignored. Therefore, when error concealment is performed for a compressed macro block, some distributed data by pass 3 may not be reproduced.

Video error code processing

If errors are detected in a compressed macro block which is reproduced and processed with error correction, the compressed data area containing these errors shall be replaced with the video error code. This process replaces the first two byte data of the compressed data area with the code:

MSB   LSB
1000000000000110b

The first 9 bits are DC error code, the next 3 bits are the information of DCT mode and class number, and the last 4 bits are the EOB as shown in figure 55. When the compressed macro blocks after error code processing are input to the decoder which does not operate with video error code, all data in this compressed macro block shall be processed as invalid.

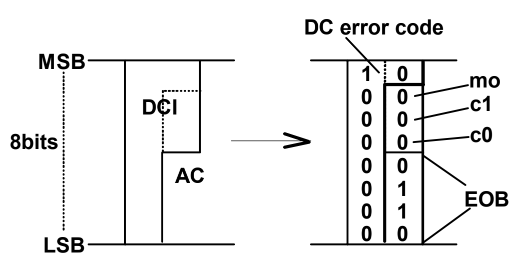


Figure 55 – Video error code

8.8 Intraframe deshuffling

Prior to recording, compressed video data shall be deshuffled to regain the original image structure. The operation is required for maximum data recovery at nonstandard playback speeds. A compressed macro block data is distributed to data-sync blocks as shown in figure 56. A compressed macro block whose compressed macro block number is CM i, j, k is distributed to a data-sync block of sync block numbers as follows:

27j + k + 21 of track i where i = 0, …, n-1
j = 0, …, 4
k = 0, …, 26
n = 10 x m for 525/60 system
n = 12 x m for 625/50 system
m = 1 for 4:1:1 compression
m = 2 for 4:2:2 compression

8.9 Video auxiliary data (VAUX)

VAUX shall be added to the compressed video data as shown in figure 26.

VAUX is formed using the fixed length pack structure. Figure 57 shows the VAUX pack arrangement of each track. There are 15 packs following the ID code of the data-sync block of which the sync block number is 19, 20, and 156. Therefore, there are 45 packs in each track, and there are two reserved bytes in each data-sync block for VAUX. The default value of the reserved bytes is FF_h. VAUX packs are sequentially numbered from 0 to 44 from the entrance side of the video sector in the order as shown in figure 57. This number is called the video pack number.

Table 45 shows the VAUX data. The VAUX source pack and VAUX source control pack include mandatory data for playback video signals and shall be recorded.

The other area of VAUX consists of 43 packs per track, 430 packs per frame for the 525/60 system and 516 packs per frame for the 625/50 system of 25 Mb/s format, and 860 packs per frame for the 525/60 system and 1032 packs per frame for the 625/50 system of 50 Mb/s format.

The reserved area of VAUX is as follows:

25 Mb/s format

- 525/60 system
  (5 bytes x 43 packs + 6 bytes) x 10 tracks x 30 frames = 66300 bytes

- 625/50 system
  (5 bytes x 43 packs + 6 bytes) x 12 tracks x 25 frames = 66300 bytes

50 Mb/s format

- 525/60 system
  (5 bytes x 43 packs + 6 bytes) x 20 tracks x 30 frames = 132600 bytes

- 625/50 system
  (5 bytes x 43 packs + 6 bytes) x 24 tracks x 25 frames = 132600 bytes

The reserved area shall be filled with FF_h.

Sync block number	Track number				
	0	1	······	n-2	n-1
156	VAUX	VAUX	······	VAUX	VAUX
155	CM 0, 4, 26	CM 1, 4, 26	······	CM n-2, 4, 26	CM n-1, 4, 26
154	CM 0, 4, 25	CM 1, 4, 25	······	CM n-2, 4, 25	CM n-1, 4, 25
⋮	⋮	⋮		⋮	⋮
129	CM 0, 4, 0	CM 1, 4, 0	······	CM n-2, 4, 0	CM n-1, 4, 0
128	CM 0, 3, 26	CM 1, 3, 26	······	CM n-2, 3, 26	CM n-1, 3, 26
127	CM 0, 3, 25	CM 1, 3, 25	······	CM n-2, 3, 25	CM n-1, 3, 25
⋮	⋮	⋮		⋮	⋮
102	CM 0, 3, 0	CM 1, 3, 0	······	CM n-2, 3, 0	CM n-1, 3, 0
101	CM 0, 2, 26	CM 1, 2, 26	······	CM n-2, 2, 26	CM n-1, 2, 26
100	CM 0, 2, 25	CM 1, 2, 25	······	CM n-2, 2, 25	CM n-1, 2, 25
⋮	⋮	⋮		⋮	⋮
75	CM 0, 2, 0	CM 1, 2, 0	······	CM n-2, 2, 0	CM n-1, 2, 0
74	CM 0, 1, 26	CM 1, 1, 26	······	CM n-2, 1, 26	CM n-1, 1, 26
73	CM 0, 1, 25	CM 1, 1, 25	······	CM n-2, 1, 25	CM n-1, 1, 25
⋮	⋮	⋮		⋮	⋮
48	CM 0, 1, 0	CM 1, 1, 0	······	CM n-2, 1, 0	CM n-1, 1, 0
47	CM 0, 0, 26	CM 1, 0, 26	······	CM n-2, 0, 26	CM n-1, 0, 26
46	CM 0, 0, 25	CM 1, 0, 25	······	CM n-2, 0, 25	CM n-1, 0, 25
⋮	⋮	⋮		⋮	⋮
21	CM 0, 0, 0	CM 1, 0, 0	······	CM n-2, 0, 0	CM n-1, 0, 0
20	VAUX	VAUX	······	VAUX	VAUX
19	VAUX	VAUX	······	VAUX	VAUX

NOTES
n = 10 x m for 525/60 system
n = 12 x m for 625/50 system
m = 1 for 4:1:1 compression
m = 2 for 4:2:2 compression

Figure 56 – Relation between the compressed macro block number and the data-sync block

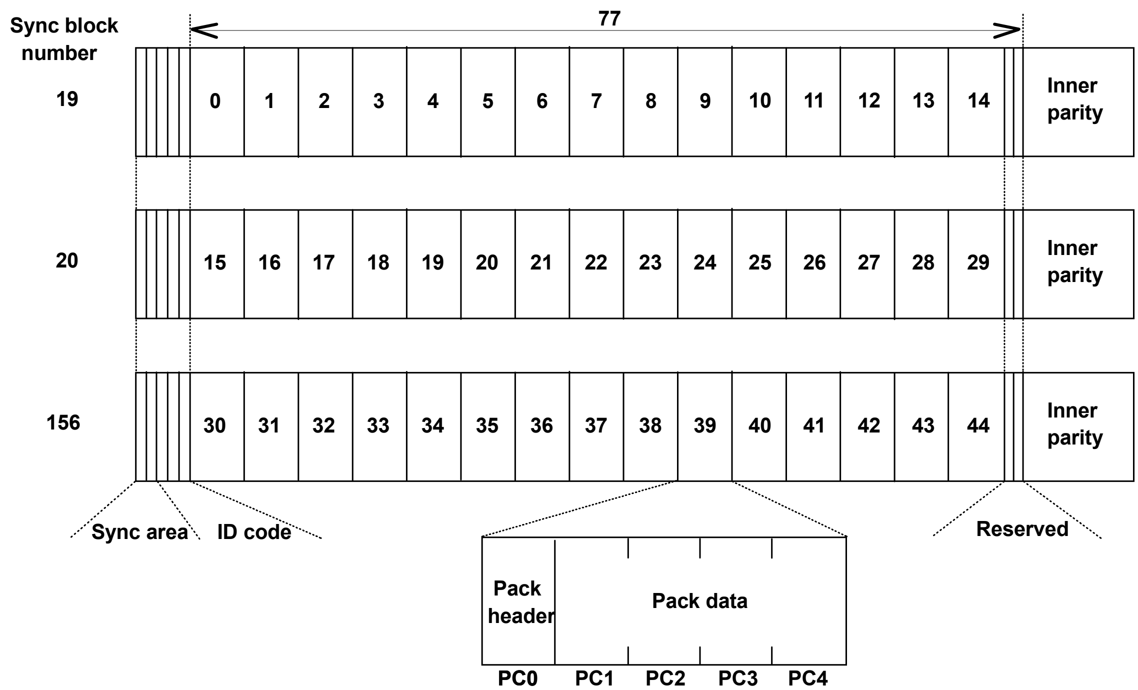


Figure 57 – Arrangement

Table 45 – VAUX data

Video pack number		**VAUX data of a video frame**
Track A	**Track B**	
39	**0**	**VS**
40	**1**	**VSC**

NOTES
VS: VAUX source pack (pack header = 60h)
VSC: VAUX source control pack (pack header = 61h)

25 Mb/s format
525/60 system
Track A: Track number 0, 2, 4, 6, 8
Track B: Track number 1, 3, 5, 7, 9
625/50 system
Track A: Track number 0, 2, 4, 6, 8, 10
Track B: Track number 1, 3, 5, 7, 9, 11

50 Mb/s format
525/60 system
Track A: Track number 0, 1, 4, 5, 8, 9, 12, 13, 16, 17
Track B: Track number 2, 3, 6, 7, 10, 11, 14, 15, 18, 19
625/50 system
Track A: Track number 0, 1, 4, 5, 8, 9, 12, 13, 16, 17, 20, 21
Track B: Track number 2, 3, 6, 7, 10, 11, 14, 15, 18, 19, 22, 23

8.9.1 VAUX source pack (VS)

Table 46 shows the mapping of the VAUX source pack.

Table 46 – Mapping of VAUX source pack

	MSB							LSB
PC0	0	1	1	0	0	0	0	0
PC1	Res	Res	RR		Res	Res	Res	Res
PC2	Res	Res	Res	Res	Res	Res	Res	Res
PC3	Arb	Arb	50/60	STYPE				
PC4	Res	Res	Res	Res	Res	Res	Res	Res

50/60 :
- 0 = 60-field system
- 1 = 50-field system

RR: Total recording rate
- 10b = 50Mb/s
- 11b = 25Mb/s

STYPE: STYPE defines a type of video signal.

STYPE	Type of video signal
0 0 0 0 0	4:1:1 compression (D-7, 25Mb/s)
0 0 0 0 1 ... 0 0 0 1 1	Reserved
0 0 1 0 0	4:2:2 compression (D-7, 50Mb/s)
0 0 1 0 1 ... 1 1 1 1 1	Reserved

8.9.2 VAUX source control pack (VSC)

Table 47 shows the mapping of the VAUX source control pack.

Table 47 – Mapping of VAUX source control pack

	MSB							LSB
PC0	0	1	1	0	0	0	0	1
PC1	CGMS		0	0	Res	Res	Res	Res
PC2	Arb	Res	0	0	Res	DISP		
PC3	FF	FS	FC	Res	Res	Res	0	0
PC4	Res	Res	Res	Res	Res	Res	Res	Res

CGMS: Copy generation management system

CGMS	Copy possible generation
0 0	Copy free
0 1	TBA
1 0	
1 1	

DISP: Display select mode

DISP	Aspect ratio and format	Position
0 0 0	4 : 3 full format	Not applicable
0 0 1	Reserved	Center
0 1 0	16 : 9 full format (squeeze)	Not applicable
0 1 1 ⋮ 1 1 1	Reserved	

FF: Frame/Field flag

FF indicates whether two consecutive fields are delivered, or one field is repeated twice during one frame period.

0 = Only one of two fields is delivered twice.

1 = Both fields are delivered in order.

FS: First/Second flag

FS indicates a field which should be delivered during field one period.

0 = Field 2 is delivered.

1 = Field 1 is delivered.

FF	FS	Output field
1	1	Field 1 and field 2 are output in this order
1	0	Field 2 and field 1 are output in this order
0	1	Field 1 is output twice
0	0	Field 2 is output twice

FC: Frame change flag

FC indicates whether the picture of the current frame is repeated on the immediately previous frame.

0 = Same picture as the immediate previous frame

1 = Different picture from the immediate previous frame

8.10 Error correction code addition

Video data are protected by inner and outer error correction codes.

8.10.1 Inner error correction code

The inner parity as shown in figure 26 is defined as the codeword of an inner error correction code. See Clause 7.5.1 for the specification of this error correction code.

8.10.2 Outer error correction code

The outer parity as shown in figure 26 is defined as a codeword of an outer error correction code. The outer error correction code is a (149, 138) Reed-Solomon code in GF(256) of which the field generator polynomial is shown as:

$$X^8 + X^4 + X^3 + X^2 + 1$$

where X^i are place-keeping variables in GF(2), the binary field.

The generator polynomial of the code in GF(256) is:

$$g_{vout}(X) = (X + 1)(X + \alpha)(X + \alpha^2)(X + \alpha^3) \ldots (X + \alpha^9)(X + \alpha^{10})$$

where α is given by 2h in GF(256). The outer parity bytes, K_{10}, K_9, K_8, K_7, K_6, K_5, K_4, K_3, K_2, K_1, K_0 as shown in figure 58 are given by the equation:

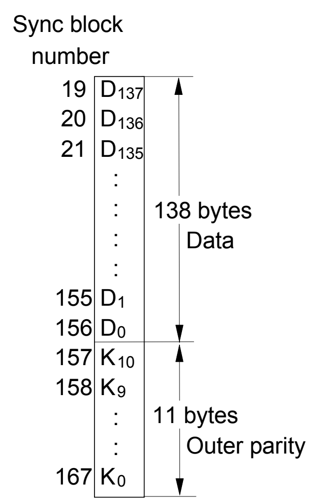
$$K_{10}X^{10} + K_9X^9 + K_8X^8 + K_7X^7 + K_6X^6 + K_5X^5 + K_4X^4 + K_3X^3 + K_2X^2 + K_1X + K_0$$

which is a residue of $X^{11}D(X)$ divided by $g_{vout}(X)$, where the data polynomial D(X) is defined as:

$$D(X) = D_{137}X^{137} + D_{136}X^{136} + \ldots\ldots + D_2X^2 + D_1X + D_0$$

and the codeword polynomial is given by the following equation for every column of the byte position number 5 to 81:

$$D_{137}X^{148} + D_{136}X^{147} + \ldots\ldots + D_1X^{12} + D_0X^{11} + K_{10}X^{10} + K_9X^9 + \ldots\ldots + K_1X + K_0$$



Where D and K are in GF(256)

Figure 58 – Data and outer parity of a data sync block for video sector

9 Subcode processing

9.1 Introduction

Subcode data is processed with every video frame. The subcode data shall be recorded 10 consecutive tracks in the frame for the 525/60 system and 12 consecutive tracks in the frame for the 625/50 system for 25 Mb/s format. The subcode data shall be recorded 20 consecutive tracks in the frame for the 525/60 system and 24 consecutive tracks in the frame for the 625/50 system for 50 Mb/s format. Each subcode sector is a block of 5 columns by 12 rows as shown in figure 28. Subcode data with the addition of an error correction code (ECC) shall be modulated prior to recording. A typical block diagram of the subcode processing is shown in figure 8.

9.2 Subcode data

As shown in figure 59, each subcode row consists of a pack header byte and 4 data bytes. Within the 12 columns of the subcode data pack, a time code pack (TC) and a binary group pack (BG) are included as shown in table 48.

The time and control code, which is internally generated or externally input, shall comply with SMPTE 12M.

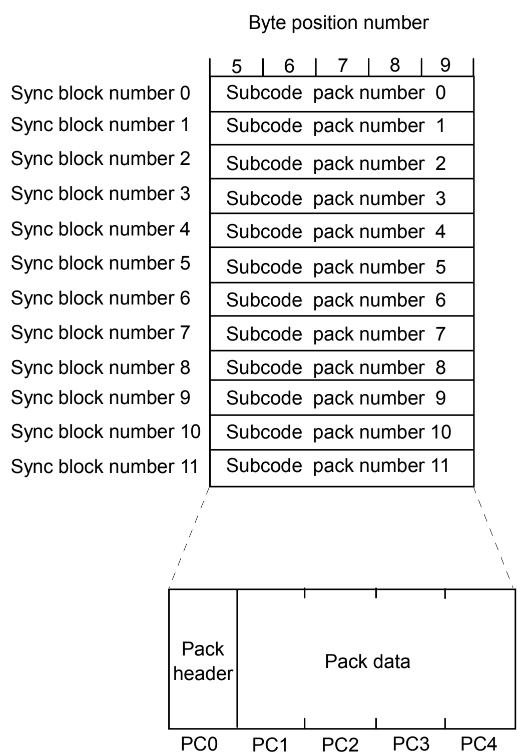


Figure 59 – Arrangement of subcode data

Table 48 – Mapping of subcode pack

Subcode pack number	First half of a video frame	Second half of a video frame
0	Reserved	Reserved
1	Reserved	Reserved
2	Reserved	Reserved
3	TC	TC
4	BG	Reserved
5	TC	Reserved
6	Reserved	Reserved
7	Reserved	Reserved
8	Reserved	Reserved
9	TC	TC
10	BG	Reserved
11	TC	Reserved

where TC: Time code pack (Pack header = 13_h)
BG: Binary group pack (Pack header = 14_h)

25 Mb/s format

525/60 system
The first half of a video frame: Track number 0, 1, ..., 4
The second half of a video frame: Track number 5, 6, ..., 9
625/50 system
The first half of a video frame: Track number 0, 1, ..., 5
The second half of a video frame: Track number 6, 7, ..., 11

50 Mb/s format

525/60 system
The first half of a video frame: Track number 0, 1, ..., 9
The second half of a video frame: Track number 10, 11, ..., 19
625/50 system
The first half of a video frame: Track number 0, 1, ..., 11
The second half of a video frame: Track number 12, 13, ..., 23

The subcode data frame is provided with a reserved area as follows:

25 Mb/s format

525/60 system
5 bytes x 16 packs x 5 track pairs x 30 frames = 12000 bytes
625/50 system
5 bytes x 16 packs x 6 track pairs x 25 frames = 12000 bytes

50 Mb/s format

525/60 system
5 bytes x 16 packs x 10 track pairs x 30 frames = 24000 bytes
625/50 system
5 bytes x 16 packs x 12 track pairs x 25 frames = 24000 bytes

9.2.1 Time code pack (TC)

Table 49 shows the mapping of the time code pack.

Table 49 – Mapping of time code pack

525/60 system								
	MSB							LSB
PC0	0	0	0	1	0	0	1	1
PC1	CF	DF	Tens of frames		Units of frames			
PC2	PC	Tens of seconds			Units of seconds			
PC3	BGF0	Tens of minutes			Units of minutes			
PC4	BGF2	BGF1	Tens of hours		Units of hours			
625/50 system								
	MSB							LSB
PC0	0	0	0	1	0	0	1	1
PC1	CF	NA	Tens of frames		Units of frames			
PC2	BGF0	Tens of seconds			Units of seconds			
PC3	BGF2	Tens of minutes			Units of minutes			
PC4	PC	BGF1	Tens of hours		Units of hours			
NOTE – Detailed information is given in ANSI/SMPTE 12M.								

DF: Drop frame flag
- DF = 0: Nondrop frame time code
- DF = 1: Drop frame time code

CF: Color frame
- CF = 0: Unsynchronized mode
- CF = 1: Synchronized mode

PC: Biphase mark polarity correction
- PC = 0: Even
- PC = 1: Odd

BGF: Binary group flag

NA: Not assigned

9.2.2 Binary group pack (BG)

Table 50 shows the mapping of a binary group pack.

Table 50 – Mapping of a binary group pack

	MSB							LSB
PC0	0	0	0	1	0	1	0	0
PC1	Binary group 2				Binary group 1			
PC2	Binary group 4				Binary group 3			
PC3	Binary group 6				Binary group 5			
PC4	Binary group 8				Binary group 7			

9.3 Error correction code addition

Subcode error correction code shall be a (14, 10) Reed - Solomon code on GF (16) of which the field generator polynomial is:

$$X^4 + X + 1$$

where X^i are place-keeping variables in GF(2) the binary field.

The generator polynomial of the code in GF (16) is:

$$g_{sub} (X) = (X+1) (X + \alpha) (X + \alpha^2) (X + \alpha^3)$$

where α is giving by 2h in GF (16).

The subcode parity bytes, K_3, K_2, K_1, K_0, as shown in figure 60, are given by the equation:

$$K_3 X^3 + K_2 X^2 + K_1 X + K_0$$

which is a residue of X^4 D (X) divided by g_{sub} (X), where the data polynomial D (X) is defined as:

$$D (X) = D_9X^9 + D_8X^8 + \text{---} + D_2X^2 + D_1X+D_0$$

and the codeword polynomial is given by the equation:

$$D_9X^{13} + D_8X^{12} + \text{---}\ D_1X^5 + D_0X^4 + K_3 X^3 + K_2 X^2 + K_1 X + K_0$$

Byte position number

	5	6	7	8	9	10	11
MSB	$d_{9,3}$	$d_{7,3}$	$d_{5,3}$	$d_{3,3}$	$d_{1,3}$	$k_{3,3}$	$k_{1,3}$
	$d_{9,2}$	$d_{7,2}$	$d_{5,2}$	$d_{3,2}$	$d_{1,2}$	$k_{3,2}$	$k_{1,2}$
	$d_{9,1}$	$d_{7,1}$	$d_{5,1}$	$d_{3,1}$	$d_{1,1}$	$k_{3,1}$	$k_{1,1}$
	$d_{9,0}$	$d_{7,0}$	$d_{5,0}$	$d_{3,0}$	$d_{1,0}$	$k_{3,0}$	$k_{1,0}$
	$d_{8,3}$	$d_{6,3}$	$d_{4,3}$	$d_{2,3}$	$d_{0,3}$	$k_{2,3}$	$k_{0,3}$
	$d_{8,2}$	$d_{6,2}$	$d_{4,2}$	$d_{2,2}$	$d_{0,2}$	$k_{2,2}$	$k_{0,2}$
	$d_{8,1}$	$d_{6,1}$	$d_{4,1}$	$d_{2,1}$	$d_{0,1}$	$k_{2,1}$	$k_{0,1}$
LSB	$d_{8,0}$	$d_{6,0}$	$d_{4,0}$	$d_{2,0}$	$d_{0,0}$	$k_{2,0}$	$k_{0,0}$
	Subcode data					Subcode parity	

Where Dn = (dn,3 dn,2 dn,1 dn,0) 9 >= n >= 0
Kn = (kn,3 kn,2 kn,1 kn,0) 3 >= n >= 0

Figure 60 – Bit assignment for subcode data and parity

10 Longitudinal tracks

10.1 Control track

10.1.1 Method of recording

The control track shall be recorded using the hysteresis (direct recording) method.

10.1.2 Servo reference pulse

The control track servo reference pulse, as recorded on the tape, shall be a series of pulses with a period of 6673 μs ± 10 μs as shown in figure 61 (525/60 system) or 6667 μs ± 10 μs as shown in figure 62 (625/50 system).

10.1.3 Flux polarity

The polarities of the recorded flux shall be as shown in figure 3.

10.1.4 Flux level

The peak recorded flux level shall be greater than 500 nWb/m of the track width. The recording shall attenuate any previous recording by at least 25 dB.

10.1.5 Pulse width

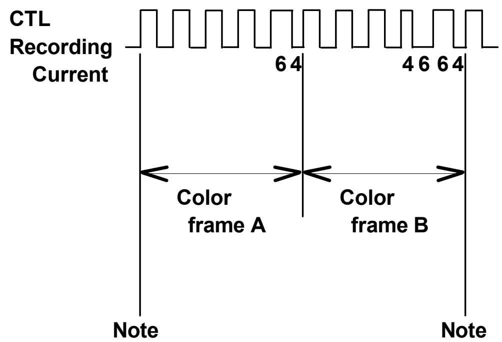
The recorded pulses shall have periods of 4T, 5T, or 6T where T equals 667.3 μs nominal (525/60 system) or 666.7 μs nominal (625/50 system). The rise and fall times of the record current (10 % to 90 % points) shall be less than 150 μs.

10.1.6 Servo reference pulse timing

As shown in figure 3, the servo reference pulse timing point and the helical track program reference point shall be time coincident.

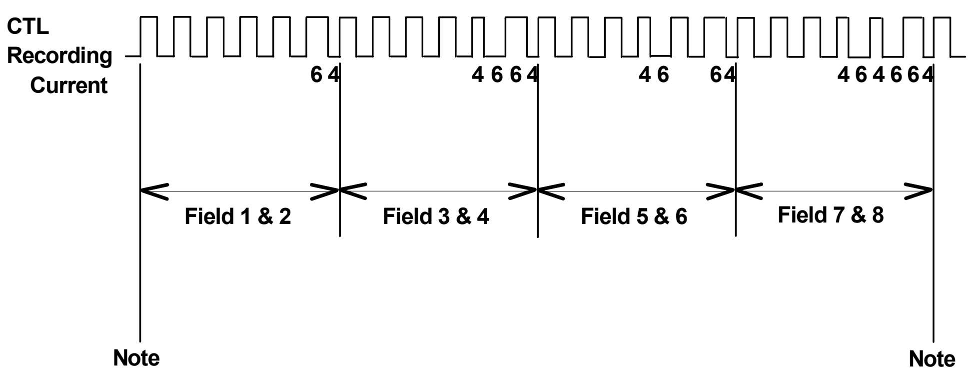
10.1.7 Color frame indication

Information on the color frame sequence, extracted from the input composite video signal, shall be encoded into the servo reference pulse as a pulse rise transmission point following the 6T or 4T duration pulse. Details are shown in figure 61.



NOTE – Control track reference pulse position for measurement of P1.

Figure 61 – Recorded control code waveform timing (525/60 system)



NOTE – Control track reference pulse position for measurement of P1.

Figure 62 – Recorded control code waveform timing (625/50 system)

10.2 Cue track

10.2.1 Method of recording

The signals shall be recorded using the anhysteresis (AC bias) method.

10.2.2 Flux level

The recorded reference audio level shall correspond to an rms magnetic short-circuit flux level of 23 nWb/m ± 3 nWb/m of track width at 1000 Hz.

10.2.3 Relative timing

Cue information shall be recorded on the tape at a point referenced to the associated video information as defined by dimension P2 of figure 3 and table 1 (525/60 system) or table 2 (625/50 system).

11 Interface

11.1 Introduction

As shown in figure 8, processed audio, video, and subcode data, prior to the addition of error correction code and modulation, may be routed out from the recording electronics for other application through a digital interface port.

11.2 Data structure

The data structure at the digital interface is shown in figures 63 and 64. The data in one video frame are divided into 10 DIF sequences for the 525/60 system and 12 DIF sequences for the 625/50 system of 25 Mb/s format, and 20 DIF sequences for the 525/60 system and 24 DIF sequences for the 625/50 system of 50 Mb/s format. Each DIF sequence consists of the header section, subcode section, VAUX section, and an audio and video section with a total of 150 DIF blocks as shown below:

– Header section: 1 DIF block;
– Subcode section: 2 DIF blocks;
– VAUX section: 3 DIF blocks;
– Audio and video section: 144 DIF blocks.

As shown in figures 63 and 64, each DIF block consists of a 3-byte ID and 77 bytes of data. DIF data bytes are numbered 0 to 79.

The MSB of each data byte in a subcode sync block and a data-sync block is mapped onto the MSB of every byte in a DIF block.

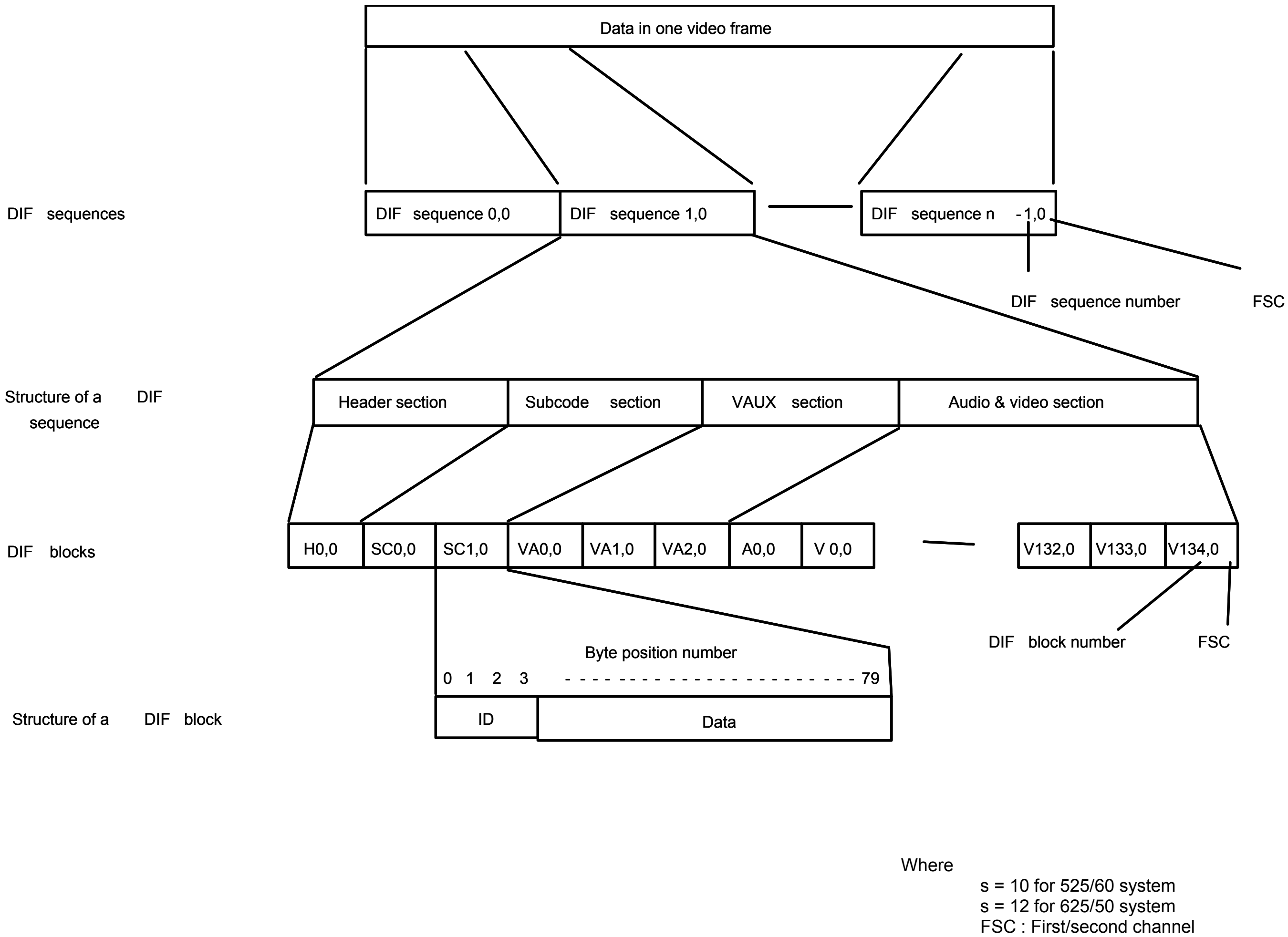
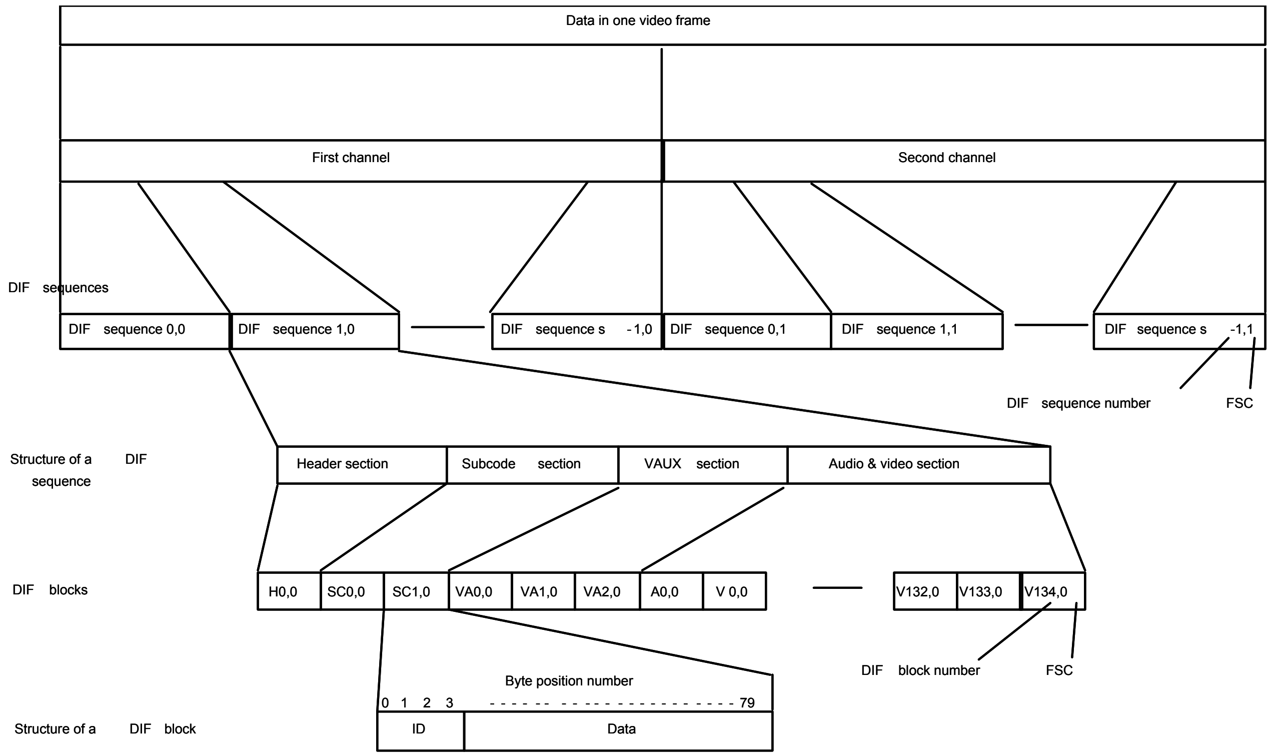
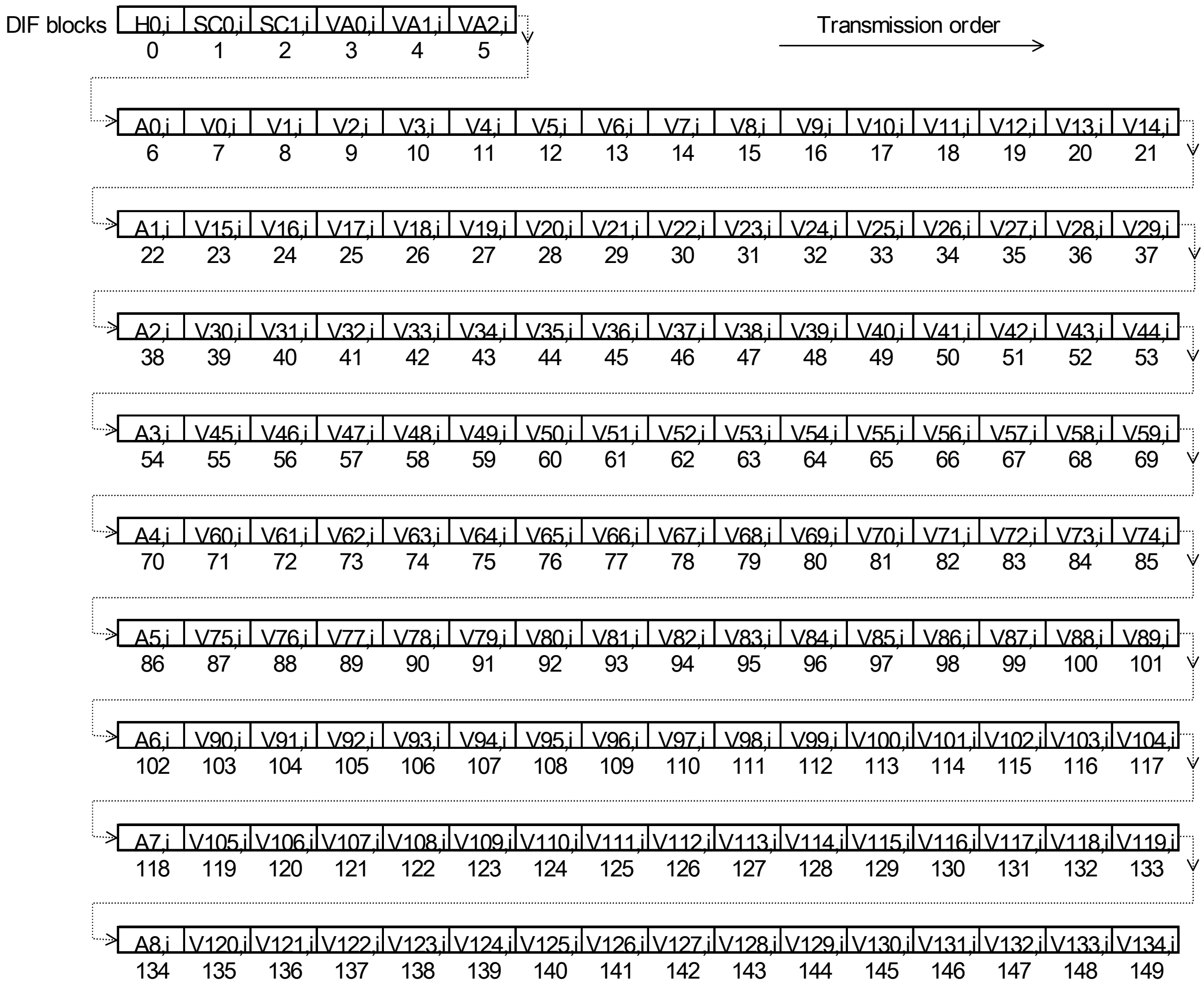


Figure 63 – Data structure of one video frame for 25 Mb/s format



Where
s = 10 for 525/60 system
s = 12 for 625/50 system
FSC : First/second channel

Figure 64 – Data structure of one video frame for 50 Mb/s format



NOTE-

i :	FSC
i = 0	for 25 Mb/s format
i = 0,1	for 50 Mb/s format
H0,i :	DIF block in header section
SC0,i , SC1,i :	DIF block in subcode section
VA0,i , VA1,i :	DIF block in VAUX section
A0,i to A8,i :	DIF block in audio section
V0,i to V134,i :	DIF block in video section

Figure 65 – Transmission order of DIF block in a DIF sequence

11.2.1 ID

The ID of the DIF block consists of 3-bytes (ID0, ID1, ID2) as shown in figures 63 and 64. Table 51 shows ID data in the DIF block.

ID contains the following:

- SCT : Section type (see table 52);
- Dseq: DIF sequence number (see tables 53 and 54);
- DBN : DIF block number (see table 55).

Table 51 – ID data in a DIF block

Byte position number		
0	1	2
ID0	ID1	ID2
SCT_2	$Dseq_3$	DBN_7
SCT_1	$Dseq_2$	DBN_6
SCT_0	$Dseq_1$	DBN_5
Reserved	$Dseq_0$	DBN_4
Arb	FSC	DBN_3
Arb	Reserved	DBN_2
Arb	Reserved	DBN_1
Arb	Reserved	DBN_0

- FSC : Identification of a DIF block in each channel
  50 Mb/s structure
    FSC = 0 : first channel
    FSC = 1 : second channel
  25 Mb/s structure
    FSC = 0

Table 52 – DIF block type

SCT_2	SCT_1	SCT_0	Section type
0	0	0	Header
0	0	1	Subcode
0	1	0	VAUX
0	1	1	Audio
1	0	0	Video
1	0	1	Reserved
1	1	0	
1	1	1	

Table 53 – DIF sequence number (525/60 system)

$Dseq_3$	$Dseq_2$	$Dseq_1$	$Dseq_0$	Meaning
0	0	0	0	DIF sequence 0
0	0	0	1	DIF sequence 1
0	0	1	0	DIF sequence 2
0	0	1	1	DIF sequence 3
0	1	0	0	DIF sequence 4
0	1	0	1	DIF sequence 5
0	1	1	0	DIF sequence 6
0	1	1	1	DIF sequence 7
1	0	0	0	DIF sequence 8
1	0	0	1	DIF sequence 9
1	0	1	0	Not used
1	0	1	1	Not used
1	1	0	0	Not used
1	1	0	1	Not used
1	1	1	0	Not used
1	1	1	1	Not used

Table 54 – DIF sequence number (625/50 system)

$Dseq_3$	$Dseq_2$	$Dseq_1$	$Dseq_0$	Meaning
0	0	0	0	DIF sequence 0
0	0	0	1	DIF sequence 1
0	0	1	0	DIF sequence 2
0	0	1	1	DIF sequence 3
0	1	0	0	DIF sequence 4
0	1	0	1	DIF sequence 5
0	1	1	0	DIF sequence 6
0	1	1	1	DIF sequence 7
1	0	0	0	DIF sequence 8
1	0	0	1	DIF sequence 9
1	0	1	0	DIF sequence 10
1	0	1	1	DIF sequence 11
1	1	0	0	Not used
1	1	0	1	Not used
1	1	1	0	Not used
1	1	1	1	Not used

Table 55 – DIF block number

DBN_7	DBN_6	DBN_5	DBN_4	DBN_3	DBN_2	DBN_1	DBN_0	Meaning
0	0	0	0	0	0	0	0	DIF blocks numbered 0
0	0	0	0	0	0	0	1	DIF blocks numbered 1
0	0	0	0	0	0	1	0	DIF blocks numbered 2
0	0	0	0	0	0	1	1	DIF blocks numbered 3
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
1	0	0	0	0	1	1	0	DIF blocks numbered 134
1	0	0	0	0	1	1	1	Not used
:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	1	Not used

11.2.2 Data

Data of the DIF block consist of 77 bytes as shown in figures 63 and 64.

11.2.2.1 Header section

The data portion of the header section is shown in table 56. Byte position numbers 3 to 7 are active and 8 to 79 are reserved.

DSF: DIF sequence flag

DSF = 0: 10 DIF sequences included in a video frame (525/60 system)
DSF = 1: 12 DIF sequences included in a video frame (625/50 system)

APT: Track application IDs (see 6.2.4)

AP1 (see 6.3.3.2)
AP2 (see 6.4.3.2)
AP3 (see 6.5.3.2)

TF: Transmitting flag

TF1: Transmitting flag of audio section
TF2: Transmitting flag of VAUX and video section
TF3: Transmitting flag of subcode section

TFn = 0: Data shall be valid
TFn = 1: Data shall be invalid.

11.2.2.2 Subcode section

The data portion of the subcode section is shown in figure 66. Subcode ID data and subcode data whose byte positions 2 through 9 in figure 28 are distributed in the subcode section as shown in figure 66. Correspondence between DIF blocks and subcode sync blocks is shown in tables 57 and 58. The mapping of the subcode data is exactly the same as described in 9.2.

Table 56 – Data in the header section

	Byte position number of H_0				
	3	4	5	6	7
MSB	DSF	Reserved	TF1	TF2	TF3
	0	Reserved	Reserved	Reserved	Reserved
	Reserved	Reserved	Reserved	Reserved	Reserved
	Reserved	Reserved	Reserved	Reserved	Reserved
	Reserved	Reserved	Reserved	Reserved	Reserved
	Reserved	APT_2	$AP1_2$	$AP2_2$	$AP3_2$
	Reserved	APT_1	$AP1_1$	$AP2_1$	$AP3_1$
LSB	Reserved	APT_0	$AP1_0$	$AP2_0$	$AP3_0$

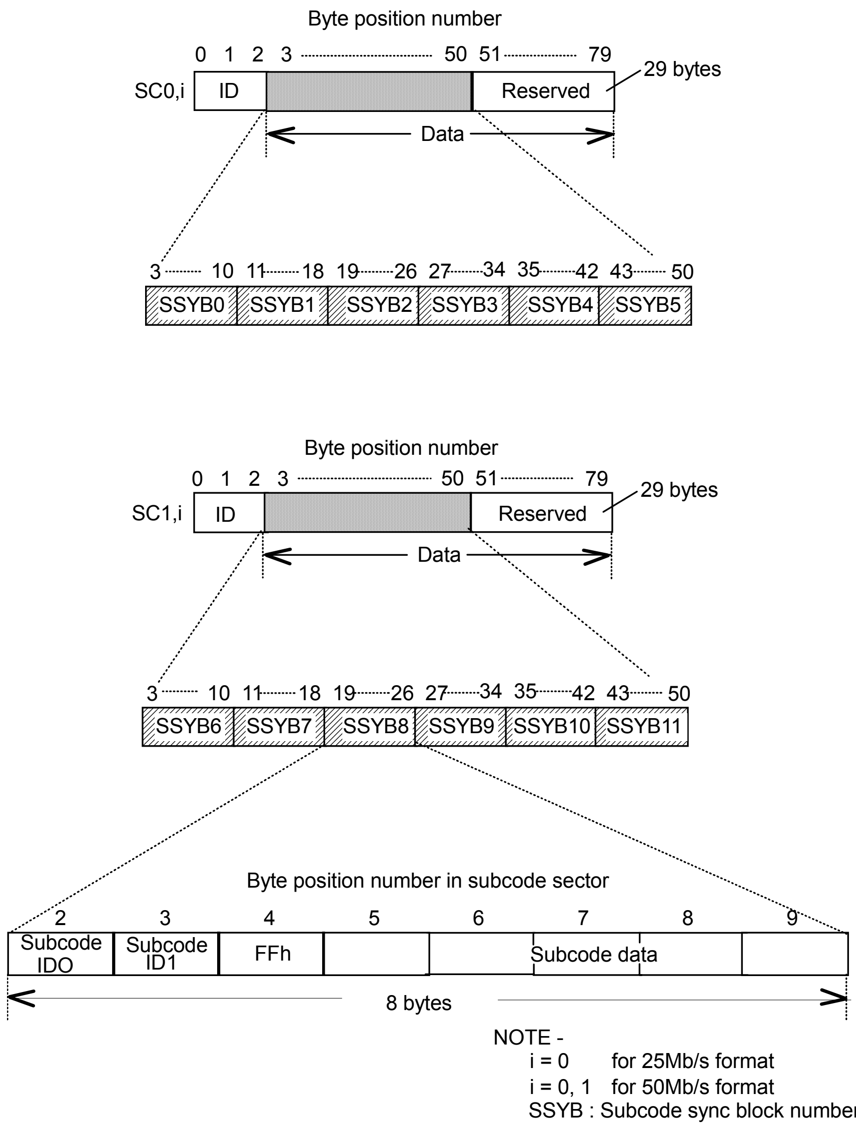


Figure 66 – Data in the subcode section

Table 57 – DIF blocks and subcode sync blocks for 25 Mb/s format

DIF sequence number	DIF block	Track number	SSYB
0	SC0,0	0	0 TO 5
	SC1,0		6 TO 11
1	SC0,0	1	0 TO 5
	SC1,0		6 TO 11
2	SC0,0	2	0 TO 5
	SC1,0		6 TO 11
:	:	:	:
s - 1	SC0,0	n – 1	0 TO 5
	SC1,0		6 TO 11
NOTE - SSYB: Subcode sync block number s = 10, n = 10 for 525 / 60 system s = 12, n = 12 for 625 / 50 system			

Table 58 – DIF blocks and subcode sync blocks for 50 Mb/s format

DIF sequence number	DIF block	Track number	SSYB
0	SC0,0	0	0 TO 5
	SC1,0		6 TO 11
	SC0,1	1	0 TO 5
	SC1,1		6 TO 11
1	SC0,0	2	0 TO 5
	SC1,0		6 TO 11
	SC0,1	3	0 TO 5
	SC1,1		6 TO 11
:	:	:	:
s –1	SC0,0	n – 2	0 TO 5
	SC1,0		6 TO 11
	SC0,1	n – 1	0 TO 5
	SC1,1		6 TO 11
NOTE - SSYB: Subcode sync block number s = 10, n = 20 for 525 / 60 system s = 12, n = 24 for 625 / 50 system			

11.2.2.3 VAUX section

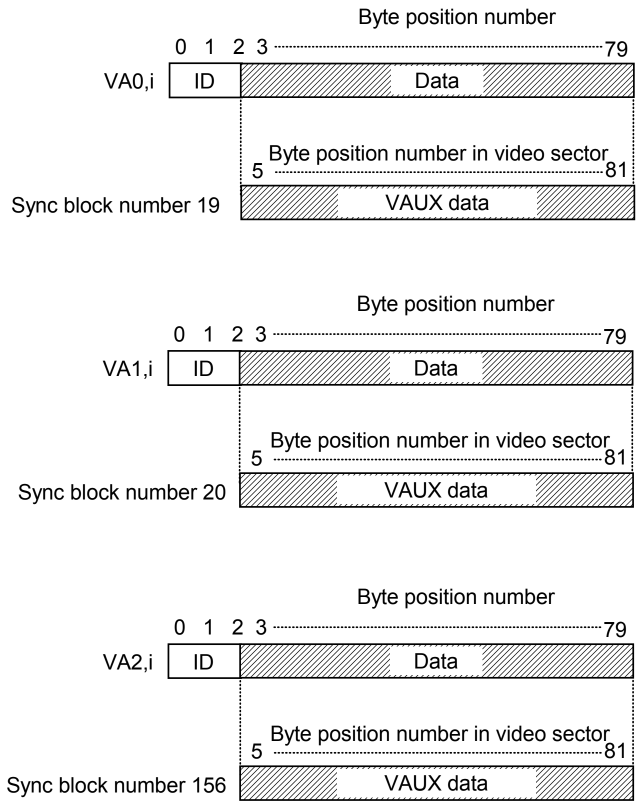
The data portion of the VAUX section is shown in figure 67. VAUX data whose byte positions 5 through 81 (77 bytes) in figure 26 are distributed among three VAUX DIF blocks (VA0, VA1, VA2).

If errors are detected in any pack of VAUX, NO INFO pack shall be transmitted. VAUX source and VAUX source control pack shall keep the same value in each video frame. Correspondence between blocks and VAUX data-sync blocks is shown in tables 59 and 60.

The mapping of the VAUX data shall be as defined below:

– VAUX source pack

The data of the VAUX source pack is the same as that in 8.9.1 except that table 46 shall be read as table 61.



NOTE - i = 0 for 25Mb/s format
i = 0, 1 for 50Mb/s format

Figure 67 – Data in the VAUX section

Table 59.– DIF blocks and VAUX data-sync blocks for 25 Mb/s format

DIF sequence number	DIF block	Track number	Syb
0	VA0,0	0	19
	VA1,0		20
	VA2,0		156
1	VA0,0	1	19
	VA1,0		20
	VA2,0		156
2	VA0,0	2	19
	VA1,0		20
	VA2,0		156
:	:	:	:
s – 1	VA0,0	n - 1	19
	VA1,0		20
	VA2,0		156
NOTE - Syb: Sync block number s = 10, n = 10 for 525 / 60 system s = 12, n = 12 for 625 / 50 system			

Table 60 – DIF blocks and VAUX data-sync blocks for 50 Mb/s format

DIF sequence number	DIF block	Track number	Syb
0	VA0,0	0	19
	VA1,0		20
	VA2,0		156
	VA0,1	1	19
	VA1,1		20
	VA2,1		156
1	VA0,0	3	19
	VA1,0		20
	VA2,0		156
	VA0,1	4	19
	VA1,1		20
	VA2,1		156
:	:	:	:
s –1	VA0,0	n - 2	19
	VA1,0		20
	VA2,0		156
	VA0,1	n - 1	19
	VA1,1		20
	VA2,1		156
NOTE – Syb: Sync block number s = 10, n = 20 for 525 / 60 system s = 12, n = 24 for 625 / 50 system			

Table 61 – Mapping of VAUX source pack for interface

	MSB							LSB
PC0	0	1	1	0	0	0	0	0
PC1	Res	Res	Res	Res	Res	Res	Res	Res
PC2	B / W	EN	CLF		Res	Res	Res	Res
PC3	Res	Res	50 / 60	STYPE				
PC4	0	Res	Res	Res	Res	Res	Res	Res

B /W: Black and White flag
0 = Black and White
1 = Color

EN: Color frames enable flag
0 = CLF is valid
1 = CLF is invalid

CLF: Color frames identification code (refer to ITU - R BT470)
For 525/60 system
00b = Color frame A
01b = Color frame B
Others = Reserved

For 625/50 system
00b = 1st, 2nd field
01b = 3rd, 4th field
10b = 5th, 6th field
11b = 7th, 8th field

– VAUX source control pack

The data of the VAUX source control pack are the same as in 8.9.2 except that table 47 shall be read as table 62.

Table 62 – Mapping of VAUX source control pack for interface

	MSB							LSB
PC0	0	1	1	0	0	0	0	1
PC1	CGMS		Res	Res	Res	Res	Res	Res
PC2	Res	Res	0	0	Res	DISP		
PC3	FF	FS	FC	IL	Res	Res	0	0
PC4	Res	Res	Res	Res	Res	Res	Res	Res

IL: Interlace flag
IL = 0: Noninterlaced
IL = 1: Interlaced

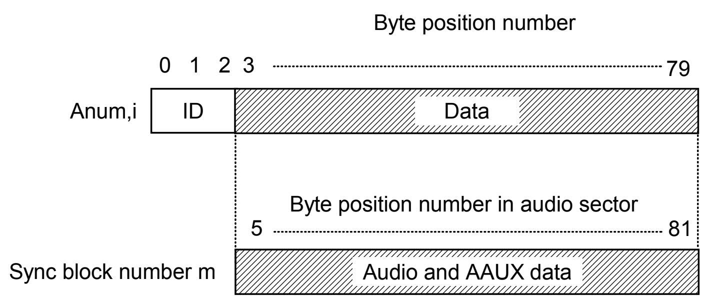
11.2.2.4 Audio section

The data portion of the audio section is shown in figure 68. Audio and AAUX data whose byte portions 5 through 81 (77 bytes) in figure 24 are distributed in the audio section. The audio and AAUX data contained in the 9 sync blocks of a track are transmitted as 9 DIF blocks, A0 though A8, in the audio section. If errors are detected in the audio data, error samples shall be replaced with audio error code, as described in 6.4.3. If no data are contained in AAUX blocks, FFh shall be transmitted. If errors are detected in any pack of AAUX, FFh shall be transmitted. AAUX source and AAUX source control pack shall keep the same value in each audio block. Correspondence between DIF blocks and audio data - sync blocks is shown in tables 63 and 64.

Mapping of the AAUX data is defined below:

– AAUX source pack

The data of the AAUX source pack is the same as that described in 7.4.1 except that table 35 shall be read as table 65.



NOTE - num = 0 to 8
i = 0 for 25Mb/s format
i = 0,1 for 50Mb/s format
m = 2 to 10 = num + 2

Figure 68 – Data in the audio section

Table 63 – DIF blocks and audio data-sync blocks for 25 Mb/s format

DIF sequence number	DIF block	Track number	Syb
0	A0,0	0	2
	A1,0		3
	:		:
	A8,0		10
1	A0,0	1	2
	A1,0		3
	:		:
	A8,0		10
2	A0,0	2	2
	A1,0		3
	:		:
	A8,0		10
: : :	: : :	: : :	: : :
s – 1	A0,0	n - 1	2
	A1,0		3
	:		:
	A8,0		10

NOTE – Syb: Sync block number
s = 10, n = 10 for 525/60 system
s = 12, n = 12 for 625/50 system

Table 64 – DIF blocks and audio data-sync blocks for 50 Mb/s format

DIF sequence number	DIF block	Track number	Syb
0	A0,0	0	2
	A1,0		3
	:		:
	A8,0		10
	A0,1	1	2
	A1,1		3
	:		:
	A8.1		10
1	A0.0	2	2
	A1.0		3
	:		:
	A8.0		10
	A0.1	3	2
	A1.1		3
	:		:
	A8.1		10
: : :	: : :	: : :	: : :
s –1	A0.0	n - 2	2
	A1.0		3
	:		:
	A8.0		10
	A0,1	n - 1	2
	A1,1		3
	:		:
	A8,1		10

NOTE - Syb: Sync block number
s = 10, n = 20 for 525/60 system
s = 12, n = 24 for 625/50 system

Table 65 – Mapping of AAUX source pack for interface

	MSB							LSB
PC0	0	1	0	1	0	0	0	0
PC1	LF	Res	AF SIZE					
PC2	0	CHN		Res	AUDIO MODE			
PC3	Res	Res	50/60	STYPE				
PC4	Res	Res	SMP			QU		

– AAUX source control pack

The data of the AAUX source control pack is the same as that described in 7.4.2 except that table 36 shall be read as table 66.

Table 66 – Mapping of AAUX source control pack for interface

	MSB							LSB
PC0	0	1	0	1	0	0	0	1
PC1	CGMS		Res	Res	Res	Res	EFC	
PC2	REC ST	REC END	FADE ST	FADE END	Res	Res	Res	Res
PC3	DRF	SPEED						
PC4	Res	Res	Res	Res	Res	Res	Res	Res

REC ST: Recording start point
0 = Recording start
1 = Not recording start point
The duration of the recording start point shall be one audio block period for each channel.

REC END: Recording end point
0 = Recording end point
1 = Not recording end point
The duration of the recording end point shall be one audio block period for each channel.

FADE ST: Fading of recording start point
0 = Fading off
1 = Fading on
The information of FADE ST shall be effective only at the recording start (REC ST) point.

FADE END: Fading of recording end point
0 = Fading off
1 = Fading on
The information of FADE END shall be effective only at the recording end (REC END) point.

DRF: Direction flag of tape travel
0 = Reverse direction
1 = Forward direction

SPEED: Shuttle speed of VTR

SPEED	Shuttle speed of VTR	
	525/60 system	625/50 system
0000000	0/120 (= 0)	0/100 (= 0)
0000001	1/120	1/100
:	:	:
1100100	100/120	100/100 (= 1)
:	:	Reserved
1111000	120/120 (= 1)	Reserved
:	Reserved	Reserved
1111110	Reserved	Reserved
1111111	Data invalid	Data invalid

– Audio data

The audio data are the same as the data in clause 7.

11.2.2.5 Video section

The data portion of the video section is shown in figure 69. Video data whose byte portions 5 through 81 (77 bytes) in figure 26 are distributed in the video section. The video data contained in the 135 sync blocks of a track are transmitted as 135 DIF blocks (V0 through V134) in the video section.

If a compressed macro block is replaced by another compressed macro block for error concealment or for fast playback mode, the STA data of the compressed macro block shall be changed. For example, STA of 4 bits at fast playback mode is changed to 1110b. Correspondence between DIF blocks and video compressed macro blocks is shown in table 67 and 68.

The corresponding value is shown as follows:

25 Mb/s structure - 4:1:1 compression

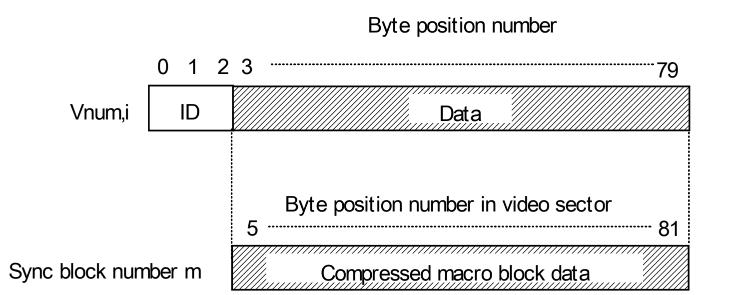
```
    If ( 525-60 system ) s = 10 else s = 12;
    for (i = 0; i < s; i ++ ) {
        a = i;
        b = ( i - 6 ) mod s;
        c = ( i - 2 ) mod s;
        d = ( i - 8 ) mod s;
        e = ( i - 4 ) mod s;
        p = a;
        q = 3;
        for ( j = 0; j<5; j++){
            for ( k = 0; k < 27; k ++){
                V ( 5 x k + q ),0 of DSNp = CM i, j, k;
            }

                If ( q = = 3 ; { p = b; q = 1; }
            else if ( q = = 1 ) { p = c; q = 0; }
            else if ( q = = 0 ) { p = d; q = 2; }
            else if ( q = = 2 ) { p = e; q = 4; }
        }
    }
```

50 Mb/s structure - 4:2:2 compression

```
if (525/60 system) s = 10 else s = 12;
for (i=0; i<s; i++){
    a = i;
    b = (i - 6) mod s;
    c = (i - 2) mod s;
    d = (i - 8) mod s;
    e = (i - 4) mod s;
    p = a;
    q = 3;
    for (j=0; j<5; j++){
        for (k=0; k<27; k++){
                V (5 × k + q),0 of DSNp = CM 2i,j,k;
                V (5 × k + q),1 of DSNp = CM 2i+1,j,k;
        }
            if (q == 3) {p = b; q = 1;}
        else if (q == 1) {p = c; q = 0;}
        else if (q == 0) {p = d; q = 2;}
        else if (q == 2) {p = e; q = 4;}
    }
}
```

Video data shall be the same as that in clause 8.



NOTE - num = 0 to 134;
i = 0 for 25 Mb/s format
i = 0,1 for 50 Mb/s format.

Figure 69 – Data in the video section

Table 67 – DIF blocks and compressed macro blocks for 25 Mb/s format

DIF sequence number	DIF block	Compressed macro block
0	V0,0	CM 2,2,0.
	V1,0	CM 6,1,0
	V2,0	CM 8,3,0
	V3,0	CM 0,0,0
	V4,0	CM 4,4,0
	:	:
	V133,0	CM 0,0,26
	V134,0	CM 4,4,26
1	V0,0	CM 3,2,0
	V1,0	CM 7,1,0
	V2,0	CM 9,3,0
	V3,0	CM 1,0,0
	V4,0	CM 5,4,0
	:	:
	V133,0	CM 1,0,26
	V134,0	CM 5,4,26
. . . .	: : : :	: : : :
s – 1	V0,0	CM 1,2,0
	V1,0	CM 5,1,0
	V2,0	CM 7,3,0
	V3,0	CM n - 1,0,0
	V4,0	CM 3,4,0
	:	:
	V133,0	CM n - 1,0,26
	V134,0	CM 3,4,26
NOTE - s = 10, n = 10 for 525/60 system s = 12, n = 12 for 625/50 system		

Table 68 – Video DIF blocks and compressed macro blocks for 50 Mb/s format

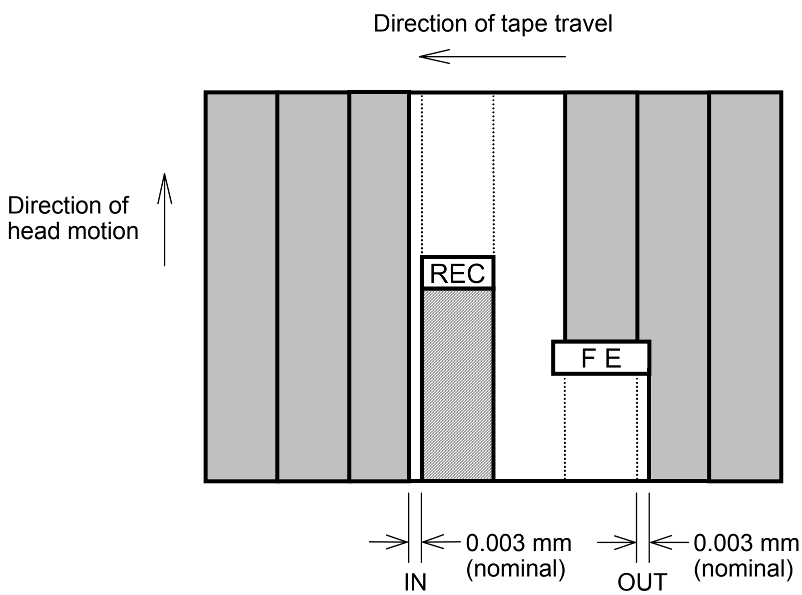
DIF sequence number	DIF block	Compressed macro block
0	V0,0 V1,0 V2,0 : V134,0	CM 4,2,0 CM 12,1,0 CM 16,3,0 : CM 8,4,26
	V0,1 V1,1 V2,1 : V134,1	CM 5,2,0 CM 13,1,0 CM 17,3,0 : CM 9,4,26
1	V0,0 V1,0 V2,0 : V134,0	CM 6,2,0 CM 14,1,0 CM 18,3,0 : CM 10,4,26
	V0,1 V1,1 V2,1 : V134,1	CM 7,2,0 CM 15,1,0 CM 19,3,0 : CM 11,4,26
. . . .	: : : :	: : : :
s –1	V0,0 V1,0 V2,0 : V134,0	CM 2,2,0 CM 10,1,0 CM 14,3,0 : CM 6,4,26
	V0,1 V1,1 V2,1 : V134,1	CM 3,2,0 CM 11,1,0 CM 15,3,0 : CM 7,4,26
NOTE - s = 10 for 525/60 system s = 12 for 625/50 system		

Annex A (normative)
Tape tension

The value measured with a tension monitor on the entrance side of the scanner may vary among manufacturers, but would typically be 0.09 N ± 0.02 N.

Annex B (normative)
Track pattern during insert editing

A guard band of 3 μm (nominal) at editing points only is shown in figures B.1 and B.2



NOTES
1 REC is a recording head.
2 FE is a flying erase head.

Figure B.1 – Typical track pattern during insert editing for 25 Mb/s format

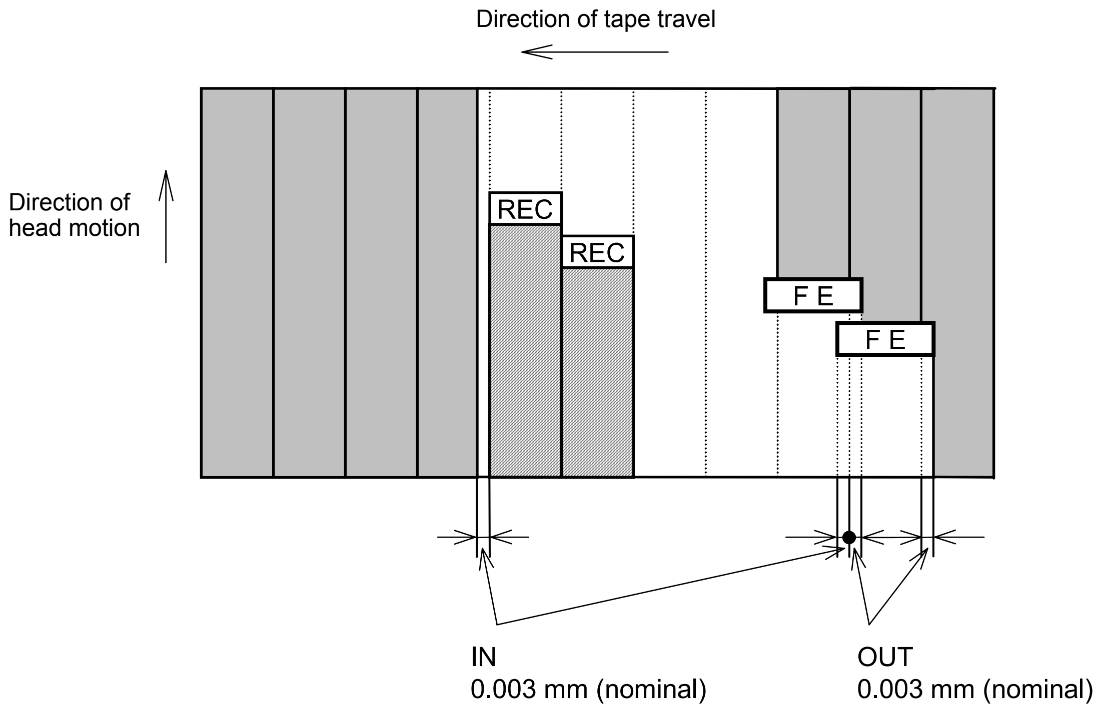


Figure B.2 – Typical track pattern during insert editing for 50 Mb/s format

Annex C (normative)
Cross-tape track measurement technique

The cross-tape track measuring technique utilizes the fact that all tracks of a helical-scan video recording, recorded by the same head at constant tape speed, have the same longitudinal track pitch, the same track angle, and the same track curvature.

From a ferrofluid development, measurements are made of the actual track positions and the distance between a minimum of 300 control track pitches. All measurements shall be made under the environmental conditions described in 3.1 except that the measurements are made without tape tension (see table C.1). The tape is then mathematically stretched to account for tape tension (see figure C.1). The theoretical track position is calculated from the corrected longitudinal track pitch and the theoretical track angle. The track location error is calculated as the difference between the theoretical track position and the actual track position (see table C.1 and figure C.2).

Track location error, which shall be expressed by the error for the center of the tracks, includes track angle errors, track straightness errors, and track pitch errors. The starting point for calculations and measurements is, for example, the cross point of the center of the track containing the program reference point and the line along the measurement path in figure C.4. The values for each eighth track are the errors for tolerance zone one. Shifting one track, the second tolerance zone can be measured. It is not necessary to measure all tracks; a suitable number can be 35 samples per zone. A plot of the track location error against the track number must be computed (see figures C.2 and C.3). The peak-to-peak value shall lie within the tolerance zones specified in 5.4.

Table C.1 – Nomenclature and calculation of track location error

Y_0	Program area reference (basic)	0.615
θ	Track angle (basic)	9.1784 °
T	Tension	0.09 N
E	Young's modulus	8000 N/mm^2 for 8.8 µm tape
A	Cross-sectional area	Thickness × Width
CTM	Distance of n control track pitches without tape tension	
CTM'	Distance of n control track pitches with tape tension	CTM' = CTM(1+ T/(A × E))
λ	Longitudinal track pitch	λ = CTM'/n
i	Track number, i = 0 for track containing reference point	
Y_i	Measured position of track i at the recorded pattern	
Δ Y	Cross-section track pitch	$\Delta Y = l \times \tan\theta$
Y_{it}	Theoretical position of track i at the recorded pattern	$Y_{it} = Y_0 + i \times \Delta Y$
l	Track pitch	$l = \lambda \times \sin\theta$
TLE	Track location error	$TLE = Y_i - Y_{it}$
Z	Tolerance zone for 25 Mb/s format Tolerance zone for 50 Mb/s format	Z1 = 0.003 mm Z2 = 0.005 mm Z1 = 0.005 mm Z2 = 0.003 mm Z3 = 0.005 mm Z4 = 0.005 mm
NOTE - For the tolerance zone of 25 Mb/s format, Z1: i = ... -2, 0, +2, +4, ... Z2: i = ... -1, +1, +3, +5, ... For the tolerance zone of 50 Mb/s format, Z1: i = ... –4, 0, +4, +8, ... Z2: i = ... –3, 1, +5, +9, ... Z3: i = ... –2, 2, +6, +10, ... Z4: i = ... –1, 3, +7, +11, ...		

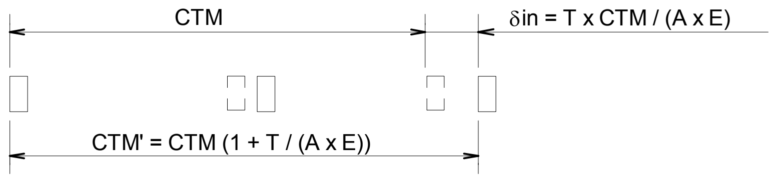


Figure C.1 – Correction factors (actual tape speed, tension)

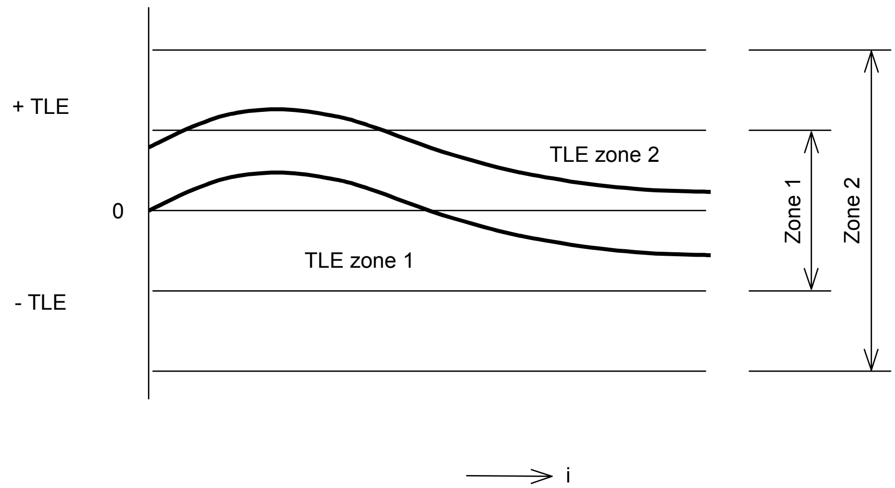


Figure C.2 – Track location error plot for 25 Mb/s format (example)

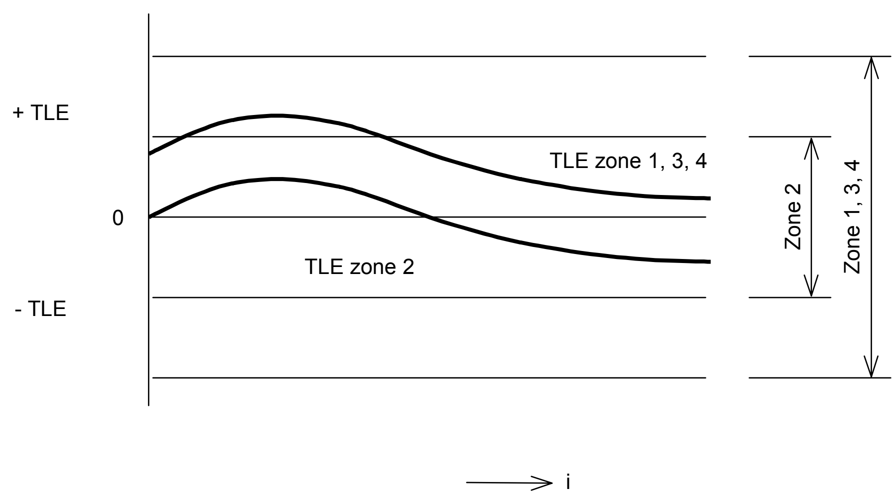
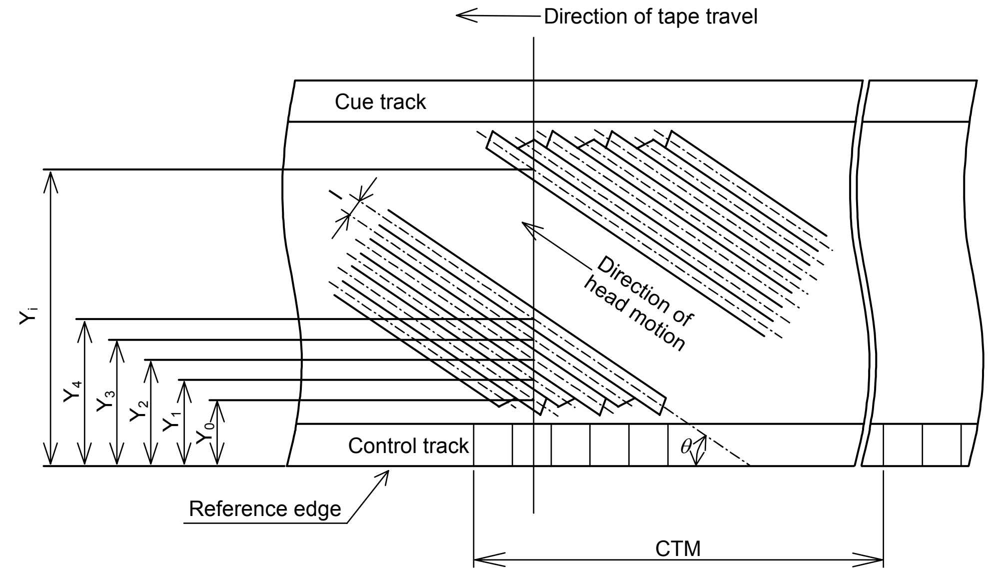


Figure C.3 – Track location error plot for 50 Mb/s format (example)



NOTE - The same head must be used for Yi measurement. (i.e. every 8th track)
CTM is the distance of n control track pitches. (n = 300 minimum)

Figure C.4 - Cross-tape measurement technique

Annex D (normative)
Frequency characteristics of F_0 track

The recommended frequency characteristics of the F_0 track shall be defined as follows:

[(N1+N2)/2] - [(NL+NH)/2] > 5 [dB]

fwL is defined as fc - fb/4000.
fwH is defined as fc + fb/4000.
NL is defined as amplitude at the fwL.
NH is defined as amplitude at the fwH.
fc means a notch frequency f1 or f2.

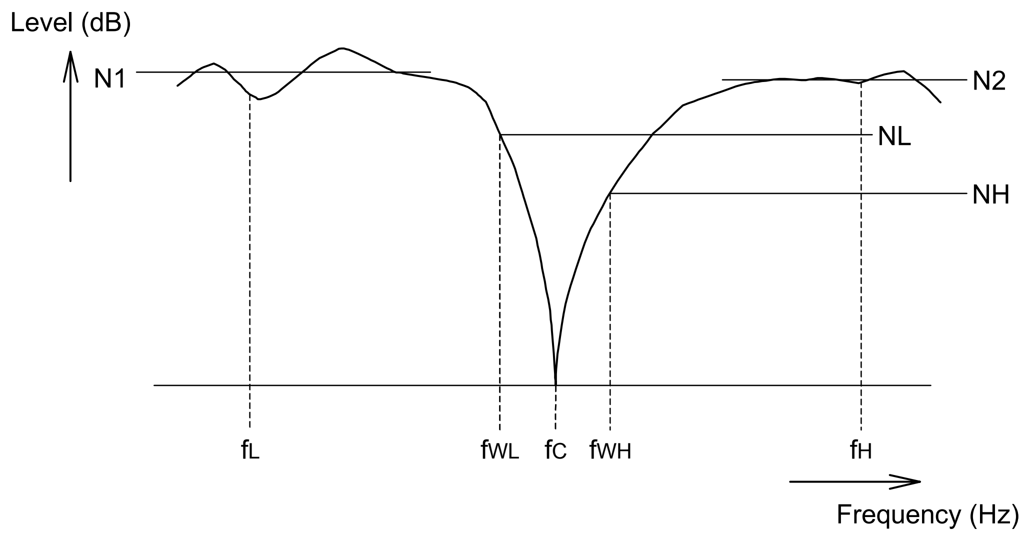


Figure D. 1 – Frequency characteristics of F0 track

Annex E (normative)
Digital filter for sampling-rate conversion from 4:2:2 to 4:1:1 color-difference signals

A template for insertion loss frequency characteristic is shown in figure E.1. Figure E.2 shows the passband ripple tolerance.

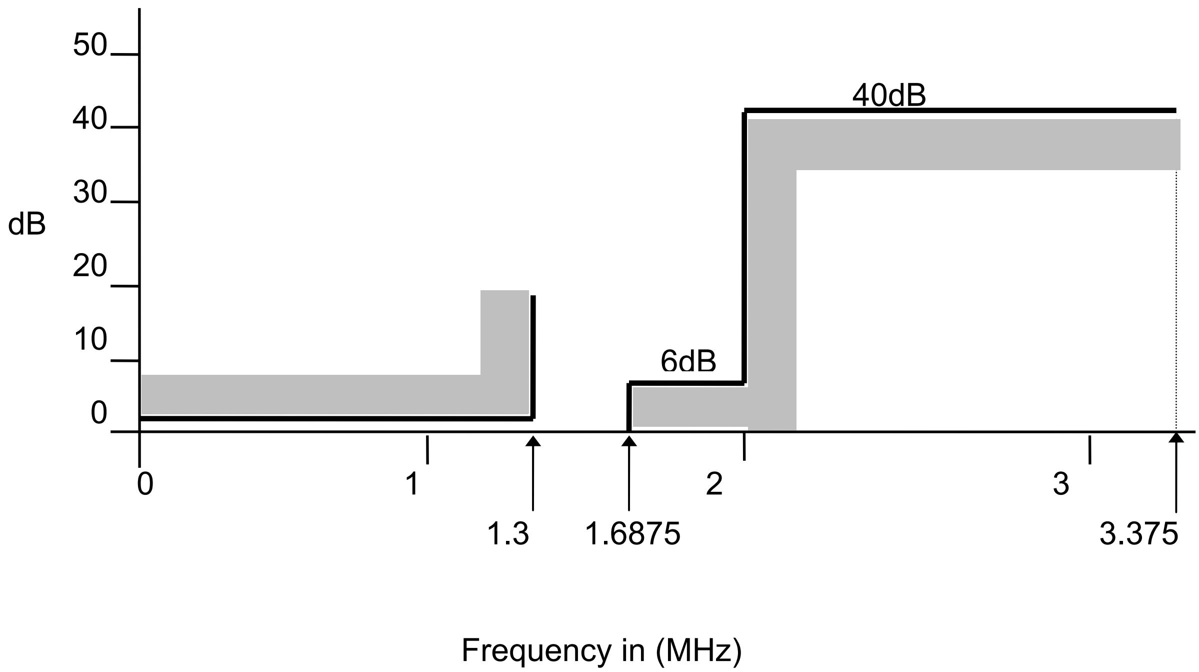


Figure E. 1 – Template for insertion loss frequency characteristic

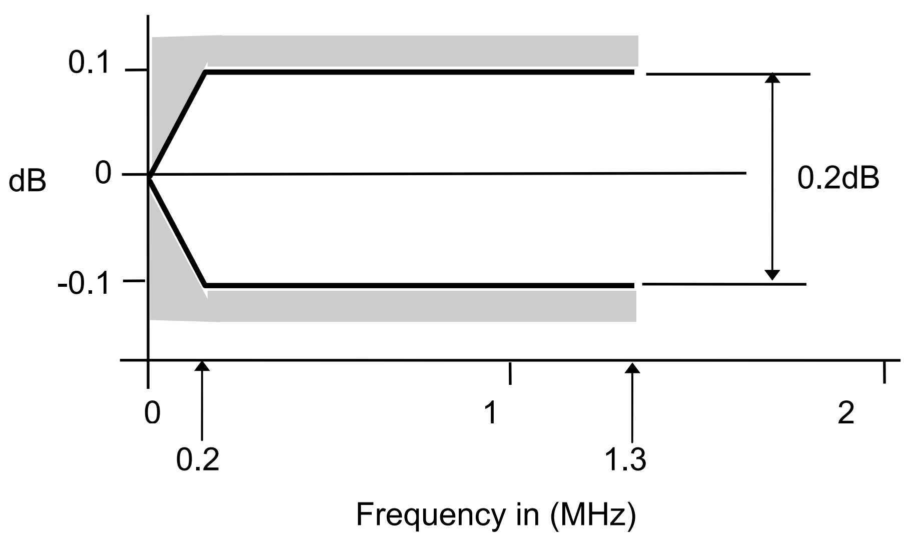


Figure – E. 2 Passband ripple tolerance

Annex F (informative)
Relationship between tape length and recording time

Table F.1 shows the relationship between tape length and recording time for M, L and EL cassette.

Table F.1 Tape length and recording time

Cassette size	Tape Thickness (μm)	Tape length (m)	Recording time (min.)	
			25 Mb/s	50 Mb/s
M	8.8	27	12	6
		51	24	12
		70	33	16
		96	46	23
		137	66	33
L	8.8	72	34	17
		137	66	33
		194	94	47
		259	126	63
EL	6.7	377	184	92

Annex G (informative)
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